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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	48 MIPS
Connectivity	I ² C, SPI, UART/USART, USB
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 21x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051t320-gqr

C8051T620/1/6/7 & C8051T320/1/2/3

5. QFN-32 Package Specifications

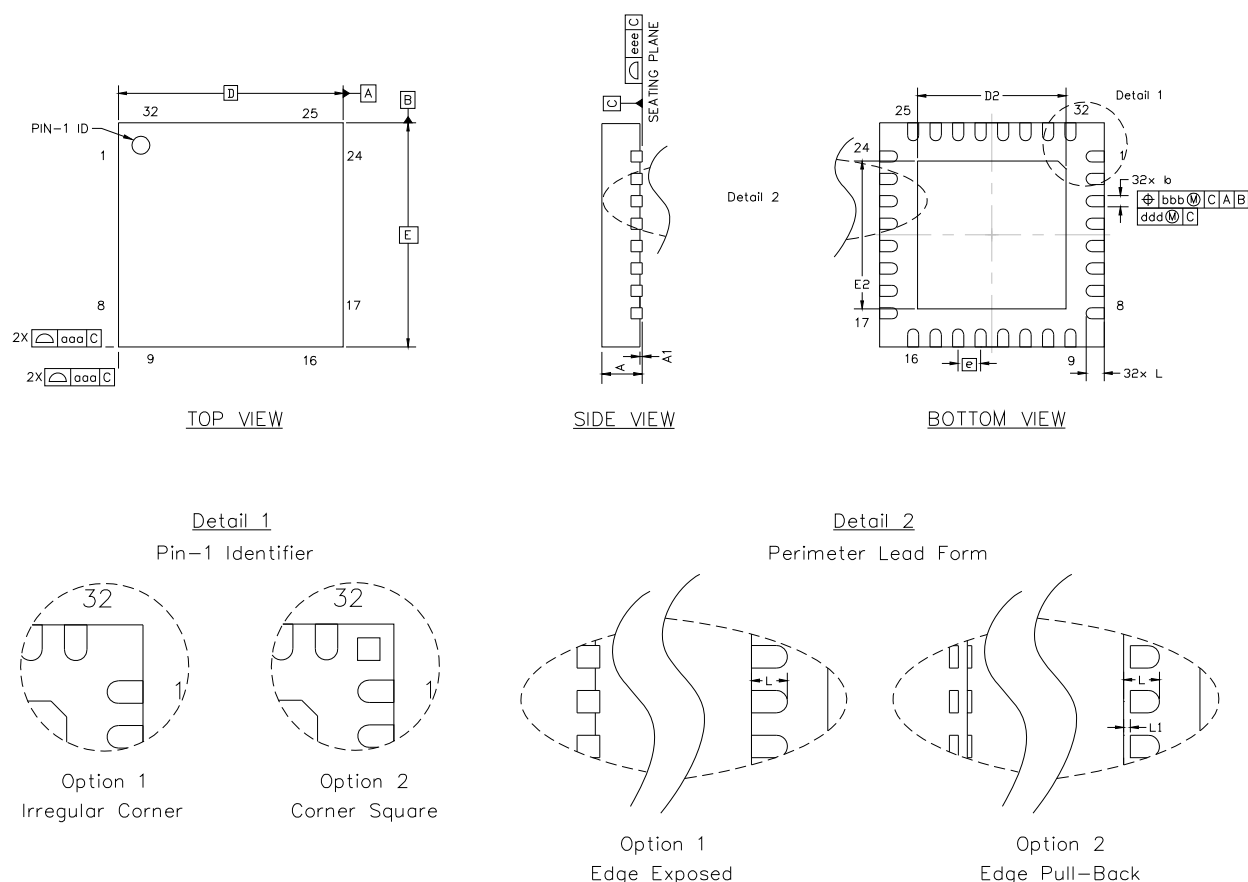


Figure 5.1. QFN-32 Package Drawing

Table 5.1. QFN-32 Package Dimensions

Dimension	Min	Typ	Max	Dimension	Min	Typ	Max
A	0.80	0.90	1.00	E2	3.20	3.30	3.40
A1	0.00	0.02	0.05	L	0.30	0.40	0.50
b	0.18	0.25	0.30	L1	0.00	—	0.15
D	5.00 BSC.			aaa	0.15		
D2	3.20	3.30	3.40	bbb	0.10		
e	0.50 BSC.			ddd	0.05		
E	5.00 BSC.			eee	0.08		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, variation VHHD except for custom features D2, E2, and L which are tolerated per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

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6. QFN-28 Package Specifications

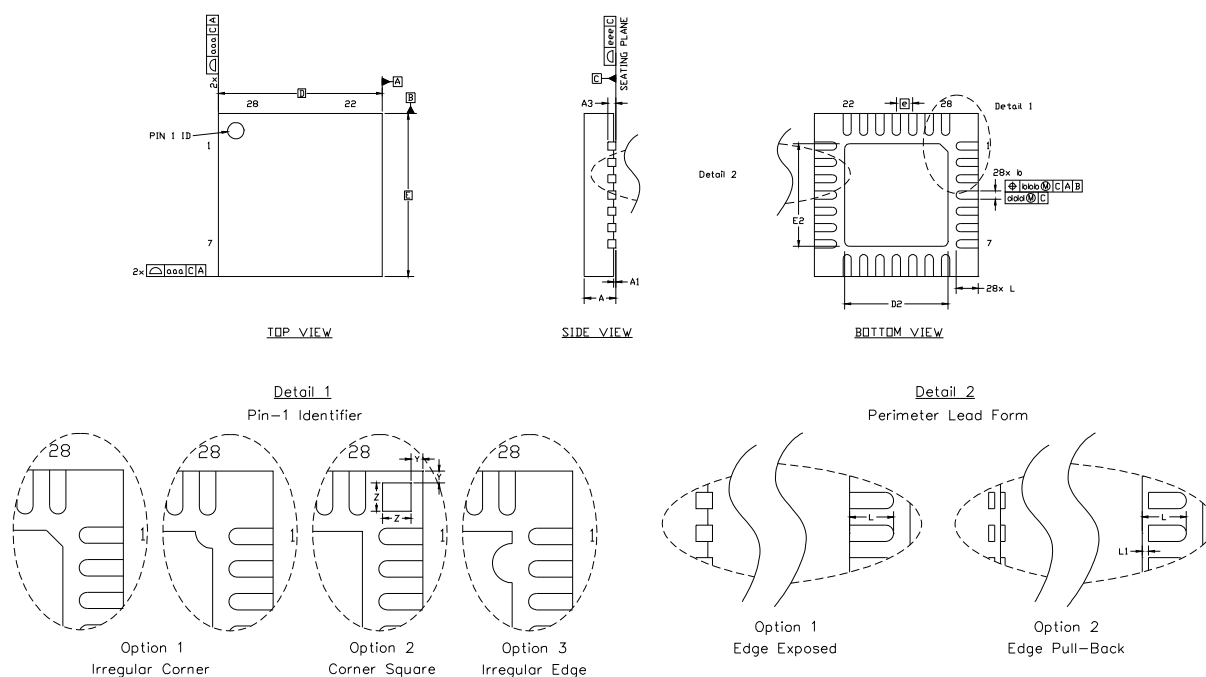


Figure 6.1. QFN-28 Package Drawing

Table 6.1. QFN-28 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	0.25 REF		
b	0.18	0.23	0.30
D	5.00 BSC.		
D2	2.90	3.15	3.35
e	0.50 BSC.		
E	5.00 BSC.		
E2	2.90	3.15	3.35
L	0.35	0.55	0.65
L1	0.00	—	0.15
aaa	0.15		
bbb	0.10		
ddd	0.05		
eee	0.08		
Z	0.44		
Y	0.18		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, variation VHHD except for custom features D2, E2, Z, Y, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

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Table 7.3. Port I/O DC Electrical Characteristics

$V_{DD} = 1.8$ to 3.6 V, $V_{IO} \leq V_{DD}$, -40 to $+85$ °C unless otherwise specified.

Parameters	Test Condition	Min	Typ	Max	Unit
Output High Voltage	$I_{OH} = -10$ μ A, Port I/O push-pull	$V_{IO} - 0.1$	—	—	V
	$I_{OH} = -3$ mA, Port I/O push-pull	$V_{IO} - 0.2$	—	—	
	$I_{OH} = -10$ mA, Port I/O push-pull	—	$V_{IO} - 0.4$	—	
Output Low Voltage	$I_{OL} = 10$ μ A	—	—	0.1	V
	$I_{OL} = 8.5$ mA	—	—	0.4	
	$I_{OL} = 25$ mA	—	0.6	—	
Input High Voltage		$0.7 \times V_{IO}$	—	—	V
Input Low Voltage		—	—	0.6	V
Input Leakage Current	Weak Pullup Off	-1	—	+1	μ A
	Weak Pullup On, $V_{IN} = 0$ V	—	25	50	μ A

Table 7.4. Reset Electrical Characteristics

-40 to $+85$ °C unless otherwise specified.

Parameters	Test Condition	Min	Typ	Max	Unit
RST Output Low Voltage	$I_{OL} = 8.5$ mA, $V_{DD} = 1.8$ V to 3.6 V	—	—	0.6	V
RST Input High Voltage		$0.75 \times V_{IO}$	—	—	V
RST Input Low Voltage		—	—	0.6	V
RST Input Pullup Current	RST = 0.0 V	—	25	50	μ A
V_{DD} POR Threshold (V_{RST})		1.7	1.75	1.8	V
Missing Clock Detector Time-out	Time from last system clock rising edge to reset initiation	500	625	750	μ s
Reset Time Delay	Delay between release of any reset source and code execution at location 0x0000	—	—	60	μ s
Minimum RST Low Time to Generate a System Reset		15	—	—	μ s
V_{DD} Monitor Turn-on Time	$V_{DD} = V_{RST} - 0.1$ V	—	50	—	μ s
V_{DD} Monitor Supply Current		—	20	30	μ A

11. Voltage Regulators (REG0 and REG1)

C8051T620/1/6/7 & C8051T320/1/2/3 devices include two internal voltage regulators: one regulates a voltage source on RGIN to 3.45 V (REG0), and the other regulates the internal core supply to 1.8 V from a V_{DD} supply of 1.8 to 3.6 V (REG1). When enabled, the REG0 output appears on the V_{DD} pin and can be used to power external devices. REG0 can be enabled/disabled by software using bit REG0DIS in register REG01CN (SFR Definition 11.1). REG1 has two power-saving modes built into the regulator to help reduce current consumption in low-power applications. These modes are accessed through the REG01CN register. Electrical characteristics for the on-chip regulators are specified in Table 7.5 on page 37.

Note that the VBUS signal must be connected to the VBUS pin when using the device in a USB network. The VBUS signal should only be connected to the RGIN pin when operating the device as a bus-powered function. REG0 configuration options are shown in Figure 11.1–Figure 11.4.

11.1. Voltage Regulator (REG0)

11.1.1. Regulator Mode Selection

REG0 offers a low power mode intended for use when the device is in suspend mode. In this low power mode, the REG0 output remains as specified; however the REG0 dynamic performance (response time) is degraded. See Table 7.5 for normal and low power mode supply current specifications. The REG0 mode selection is controlled via the REG0MD bit in register REG01CN.

11.1.2. VBUS Detection

When the USB Function Controller is used (see section Section “23. Universal Serial Bus Controller (USB0)” on page 160), the VBUS signal should be connected to the VBUS pin. The VBSTAT bit (register REG01CN) indicates the current logic level of the VBUS signal. If enabled, a VBUS interrupt will be generated when the VBUS signal has either a falling or rising edge. The VBUS interrupt is edge-sensitive, and has no associated interrupt pending flag. See Table 7.5 for VBUS input parameters.

Important Note: When USB is selected as a reset source, a system reset will be generated when a falling or rising edge occurs on the VBUS pin. See Section “20. Reset Sources” on page 121 for details on selecting USB as a reset source.

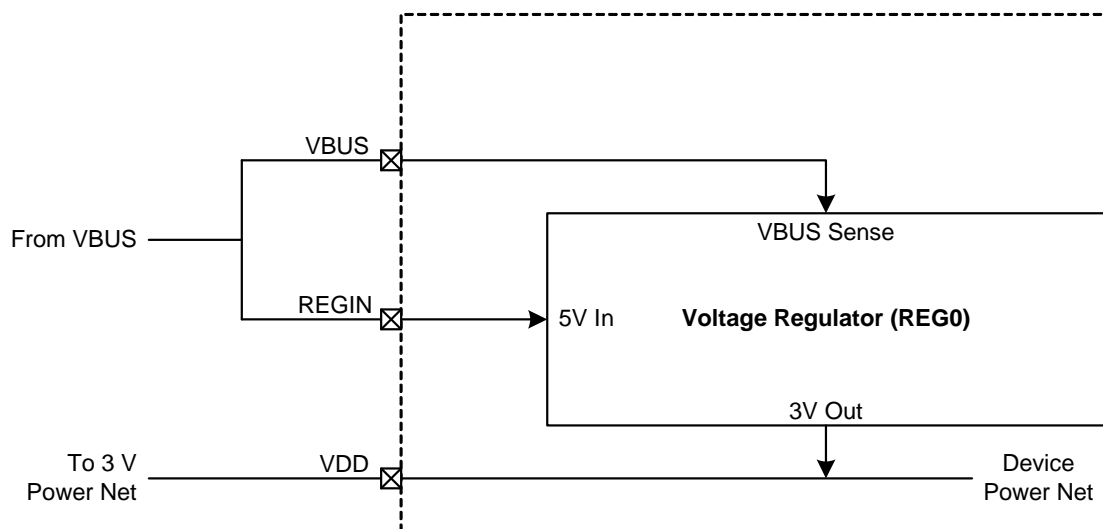


Figure 11.1. REG0 Configuration: USB Bus-Powered

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11.2. Voltage Regulator (REG1)

Under default conditions, the internal REG1 regulator will remain on when the device enters STOP mode. This allows any enabled reset source to generate a reset for the device and bring the device out of STOP mode. For additional power savings, the STOPCF bit can be used to shut down the regulator and the internal power network of the device when the part enters STOP mode. When STOPCF is set to 1, the $\overline{\text{RST}}$ pin and a full power cycle of the device are the only methods of generating a reset.

REG1 offers an additional low power mode intended for use when the device is in suspend mode. This low power mode should not be used during normal operation or if the REG0 Voltage Regulator is disabled. See Table 7.5 for normal and low power mode supply current specifications. The REG1 mode selection is controlled via the REG1MD bit in register REG01CN.

Important Note: At least 12 clock instructions must occur after placing REG1 in low power mode before the Internal High Frequency Oscillator is Suspended (OSCICN.5 = 1b).

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SFR Definition 14.6. CPT1MX: Comparator1 MUX Selection

Bit	7	6	5	4	3	2	1	0
Name		CMX1N[2:0]				CMX1P[2:0]		
Type	R	R/W			R	R/W		
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x9E

Bit	Name	Function
7	Unused	Read = 0b; Write = don't care.
6:4	CMX1N[2:0]	Comparator1 Negative Input MUX Selection. 000: P1.3 001: P1.7 010: P2.3 011: RESERVED 100: P0.5 101-111: RESERVED
3	Unused	Read = 0b; Write = don't care.
2:0	CMX1P[2:0]	Comparator1 Positive Input MUX Selection. 000: P1.2 001: P1.6 010: P2.2 011: RESERVED 100: P0.4 101-111: RESERVED

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SFR Definition 15.2. EMI0CF: External Memory Configuration

Bit	7	6	5	4	3	2	1	0
Name		USBFAE						
Type	R	R/W	R	R	R	R	R	R
Reset	0	0	0	0	0	0	1	1

SFR Address = 0x85

Bit	Name	Function
7	Unused	Read = 0b; Write = Don't Care.
6	USBFAE	USB FIFO Access Enable. 0: USB FIFO RAM not available through MOVX instructions. 1: USB FIFO RAM available using MOVX instructions. The 1k of USB RAM will be mapped in XRAM space at addresses 0x0400 to 0x07FF. The USB clock must be active and greater than or equal to twice the SYSCLK (USBCLK > 2 x SYSCLK) to access this area with MOVX instructions.
5:0	Unused	Read = 000011b; Write = Don't Care.

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SFR Definition 17.5. EIE2: Extended Interrupt Enable 2

Bit	7	6	5	4	3	2	1	0
Name				Reserved	EMAT	Reserved	ES1	EVBUS
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE7

Bit	Name	Function
7:3	Unused	Read = 0000b, Write = Don't Care.
4	Reserved	Must write 0b.
3	EMAT	Enable Port Match Interrupts. This bit sets the masking of the Port Match Event interrupt. 0: Disable all Port Match interrupts. 1: Enable interrupt requests generated by a Port Match.
2	Reserved	Must write 0b.
1	ES1	Enable UART1 Interrupt. This bit sets the masking of the UART1 interrupt. 0: Disable UART1 interrupt. 1: Enable UART1 interrupt.
0	EVBUS	Enable VBUS Level Interrupt. This bit sets the masking of the VBUS interrupt. 0: Disable all VBUS interrupts. 1: Enable interrupt requests generated by VBUS level sense.

Table 22.3. Port I/O Assignment for External Digital Event Capture Functions

Digital Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
External Interrupt 0	P0.0 - P0.7	IT01CF
External Interrupt 1	P0.0 - P0.7	IT01CF
Port Match	P0.0 - P1.7	P0MASK, P0MAT P1MASK, P1MAT

22.3. Priority Crossbar Decoder

The Priority Crossbar Decoder assigns a priority to each I/O function, starting at the top with UART0. When a digital resource is selected, the least-significant unassigned Port pin is assigned to that resource (excluding UART0, which is always at pins 4 and 5). If a Port pin is assigned, the Crossbar skips that pin when assigning the next selected resource. Additionally, the Crossbar will skip Port pins whose associated bits in the PnSKIP registers are set. The PnSKIP registers allow software to skip Port pins that are to be used for analog input, dedicated functions, or GPIO.

Because of the nature of the Priority Crossbar Decoder, not all peripherals can be located on all port pins. Figure 22.3 shows the possible pins on which peripheral I/O can appear.

Important Note on Crossbar Configuration: If a Port pin is claimed by a peripheral without use of the Crossbar, its corresponding PnSKIP bit should be set. The Crossbar skips selected pins as if they were already assigned, and moves to the next unassigned pin.

Registers XBR0, XBR1, and XBR2 are used to assign the digital I/O resources to the physical I/O Port pins. Note that when the SMBus is selected, the Crossbar assigns both pins associated with the SMBus (SDA and SCL); when a UART is selected, the Crossbar assigns both pins associated with the UART (TX and RX). UART0 pin assignments are fixed for bootloading purposes: UART TX0 is always assigned to P0.4; UART RX0 is always assigned to P0.5. Standard Port I/Os appear contiguously after the prioritized functions have been assigned. Figure 22.4 and Figure 22.5 show examples of how the crossbar assigns peripherals according to the XBRn and PnSKIP register settings.

Important Note: The SPI can be operated in either 3-wire or 4-wire modes, pending the state of the NSS-MD1–NSSMD0 bits in register SPI0CN. According to the SPI mode, the NSS signal may or may not be routed to a Port pin.

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SFR Definition 23.2. USB0ADR: USB0 Indirect Address

Bit	7	6	5	4	3	2	1	0
Name	BUSY	AUTORD	USBADDR[5:0]					
Type	R/W	R/W	R/W					
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x96

Bit	Name	Description	Write	Read
7	BUSY	USB0 Register Read Busy Flag. This bit is used during indirect USB0 register accesses.	0: No effect. 1: A USB0 indirect register read is initiated at the address specified by the USBADDR bits.	0: USB0DAT register data is valid. 1: USB0 is busy accessing an indirect register; USB0DAT register data is invalid.
6	AUTORD	USB0 Register Auto-read Flag. This bit is used for block FIFO reads. 0: BUSY must be written manually for each USB0 indirect register read. 1: The next indirect register read will automatically be initiated when software reads USB0DAT (USBADDR bits will not be changed).		
5:0	USBADDR[5:0]	USB0 Indirect Register Address Bits. These bits hold a 6-bit address used to indirectly access the USB0 core registers. Table 23.2 lists the USB0 core registers and their indirect addresses. Reads and writes to USB0DAT will target the register indicated by the USBADDR bits.		

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23.13.1. Endpoints1-3 OUT Interrupt or Bulk Mode

When the ISO bit (EOUTCSRH.6) = 0 the target endpoint operates in Bulk or Interrupt mode. Once an endpoint has been configured to operate in Bulk/Interrupt OUT mode (typically following an Endpoint0 SET_INTERFACE command), hardware will set the OPRDY bit (EOUTCSRL.0) to 1 and generate an interrupt upon reception of an OUT token and data packet. The number of bytes in the current OUT data packet (the packet ready to be unloaded from the FIFO) is given in the EOUTCNTH and EOUTCNTL registers. In response to this interrupt, firmware should unload the data packet from the OUT FIFO and reset the OPRDY bit to 0.

A Bulk or Interrupt pipe can be shut down (or Halted) by writing 1 to the SDSTL bit (EOUTCSRL.5). While SDSTL = 1, hardware will respond to all OUT requests with a STALL condition. Each time hardware generates a STALL condition, an interrupt will be generated and the STSTL bit (EOUTCSRL.6) set to 1. The STSTL bit must be reset to 0 by firmware.

Hardware will automatically set OPRDY when a packet is ready in the OUT FIFO. Note that if double buffering is enabled for the target endpoint, it is possible for two packets to be ready in the OUT FIFO at a time. In this case, hardware will set OPRDY to 1 immediately after firmware unloads the first packet and resets OPRDY to 0. A second interrupt will be generated in this case.

23.13.2. Endpoints1-3 OUT Isochronous Mode

When the ISO bit (EOUTCSRH.6) is set to 1, the target endpoint operates in Isochronous (ISO) mode. Once an endpoint has been configured for ISO OUT mode, the host will send exactly one data per USB frame; the location of the data packet within each frame may vary, however. Because of this, it is recommended that double buffering be enabled for ISO OUT endpoints.

Each time a data packet is received, hardware will load the received data packet into the endpoint FIFO, set the OPRDY bit (EOUTCSRL.0) to 1, and generate an interrupt (if enabled). Firmware would typically use this interrupt to unload the data packet from the endpoint FIFO and reset the OPRDY bit to 0.

If a data packet is received when there is no room in the endpoint FIFO, an interrupt will be generated and the OVRUN bit (EOUTCSRL.2) set to 1. If USB0 receives an ISO data packet with a CRC error, the data packet will be loaded into the endpoint FIFO, OPRDY will be set to 1, an interrupt (if enabled) will be generated, and the DATAERR bit (EOUTCSRL.3) will be set to 1. Software should check the DATAERR bit each time a data packet is unloaded from an ISO OUT endpoint FIFO.

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USB Register Definition 23.25. EOUTCNTH: USB0 OUT Endpoint Count High

Bit	7	6	5	4	3	2	1	0
Name							EOCH[1:0]	
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

USB Register Address = 0x17

Bit	Name	Function
7:2	Unused	Read = 000000b. Write = don't care.
1:0	EOCH[1:0]	OUT Endpoint Count High Byte. EOCH holds the upper 2-bits of the 10-bit number of data bytes in the last received packet in the current OUT endpoint FIFO. This number is only valid while OPRDY = 1.

27. Enhanced Serial Peripheral Interface (SPI0)

The Enhanced Serial Peripheral Interface (SPI0) provides access to a flexible, full-duplex synchronous serial bus. SPI0 can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select SPI0 in slave mode, or to disable Master Mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a chip-select output in master mode, or disabled for 3-wire operation. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

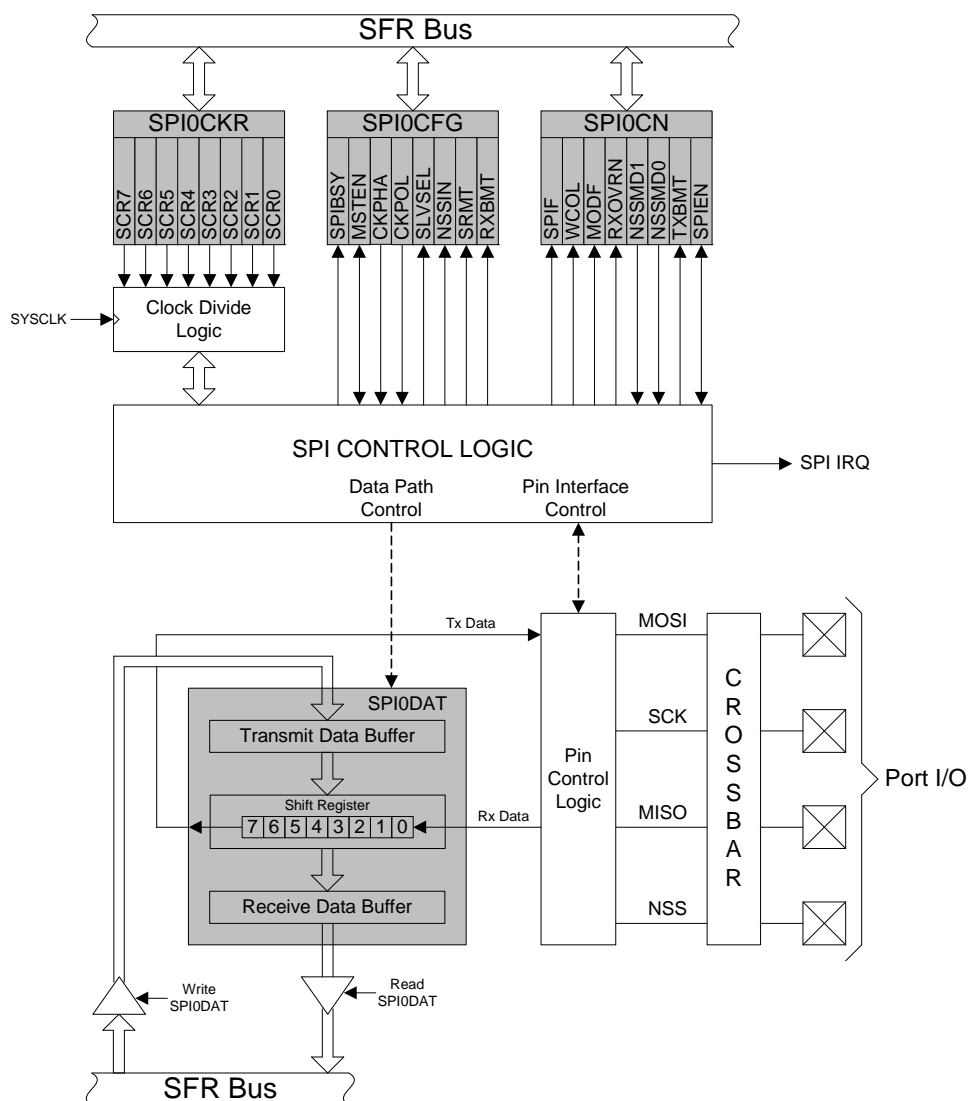


Figure 27.1. SPI Block Diagram

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SFR Definition 28.13. TMR3CN: Timer 3 Control

Bit	7	6	5	4	3	2	1	0
Name	TF3H	TF3L	TF3LEN	TF3CEN	T3SPLIT	TR3	T3XCLK[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x91

Bit	Name	Function
7	TF3H	Timer 3 High Byte Overflow Flag. Set by hardware when the Timer 3 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 3 overflows from 0xFFFF to 0x0000. When the Timer 3 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 3 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF3L	Timer 3 Low Byte Overflow Flag. Set by hardware when the Timer 3 low byte overflows from 0xFF to 0x00. TF3L will be set when the low byte overflows regardless of the Timer 3 mode. This bit is not automatically cleared by hardware.
5	TF3LEN	Timer 3 Low Byte Interrupt Enable. When set to 1, this bit enables Timer 3 Low Byte interrupts. If Timer 3 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 3 overflows.
4	TF3CEN	Timer 3 Low-Frequency Oscillator Capture Enable. When set to 1, this bit enables Timer 3 Low-Frequency Oscillator Capture Mode. If TF3CEN is set and Timer 3 interrupts are enabled, an interrupt will be generated on a falling edge of the low-frequency oscillator output, and the current 16-bit timer value in TMR3H:TMR3L will be copied to TMR3RLH:TMR3RLL.
3	T3SPLIT	Timer 3 Split Mode Enable. When this bit is set, Timer 3 operates as two 8-bit timers with auto-reload. 0: Timer 3 operates in 16-bit auto-reload mode. 1: Timer 3 operates as two 8-bit auto-reload timers.
2	TR3	Timer 3 Run Control. Timer 3 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR3H only; TMR3L is always enabled in split mode.
1:0	T3XCLK[1:0]	Timer 3 External Clock Select. This bit selects the “external” clock source for Timer 3. If Timer 3 is in 8-bit mode, this bit selects the external oscillator clock source for both timer bytes. However, the Timer 3 Clock Select bits (T3MH and T3ML in register CKCON) may still be used to select between the external clock and the system clock for either timer. 00: System clock divided by 12. 01: External clock divided by 8 (synchronized with SYSCLK when not in suspend). 10: Reserved. 11: Internal LFO/8 (synchronized with SYSCLK when not in suspend).

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29.1. PCA Counter/Timer

The 16-bit PCA counter/timer consists of two 8-bit SFRs: PCA0L and PCA0H. PCA0H is the high byte (MSB) of the 16-bit counter/timer and PCA0L is the low byte (LSB). Reading PCA0L automatically latches the value of PCA0H into a “snapshot” register; the following PCA0H read accesses this “snapshot” register. **Reading the PCA0L Register first guarantees an accurate reading of the entire 16-bit PCA0 counter.** Reading PCA0H or PCA0L does not disturb the counter operation. The CPS2–CPS0 bits in the PCA0MD register select the timebase for the counter/timer as shown in Table 29.1.

When the counter/timer overflows from 0xFFFF to 0x0000, the Counter Overflow Flag (CF) in PCA0MD is set to logic 1 and an interrupt request is generated if CF interrupts are enabled. Setting the ECF bit in PCA0MD to logic 1 enables the CF flag to generate an interrupt request. The CF bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Clearing the CIDL bit in the PCA0MD register allows the PCA to continue normal operation while the CPU is in Idle mode.

Table 29.1. PCA Timebase Input Options

CPS2	CPS1	CPS0	Timebase
0	0	0	System clock divided by 12
0	0	1	System clock divided by 4
0	1	0	Timer 0 overflow
0	1	1	High-to-low transitions on ECI (max rate = system clock divided by 4)
1	0	0	System clock
1	0	1	External oscillator source divided by 8*
1	1	x	Reserved.
Note: External oscillator source divided by 8 is synchronized with the system clock.			

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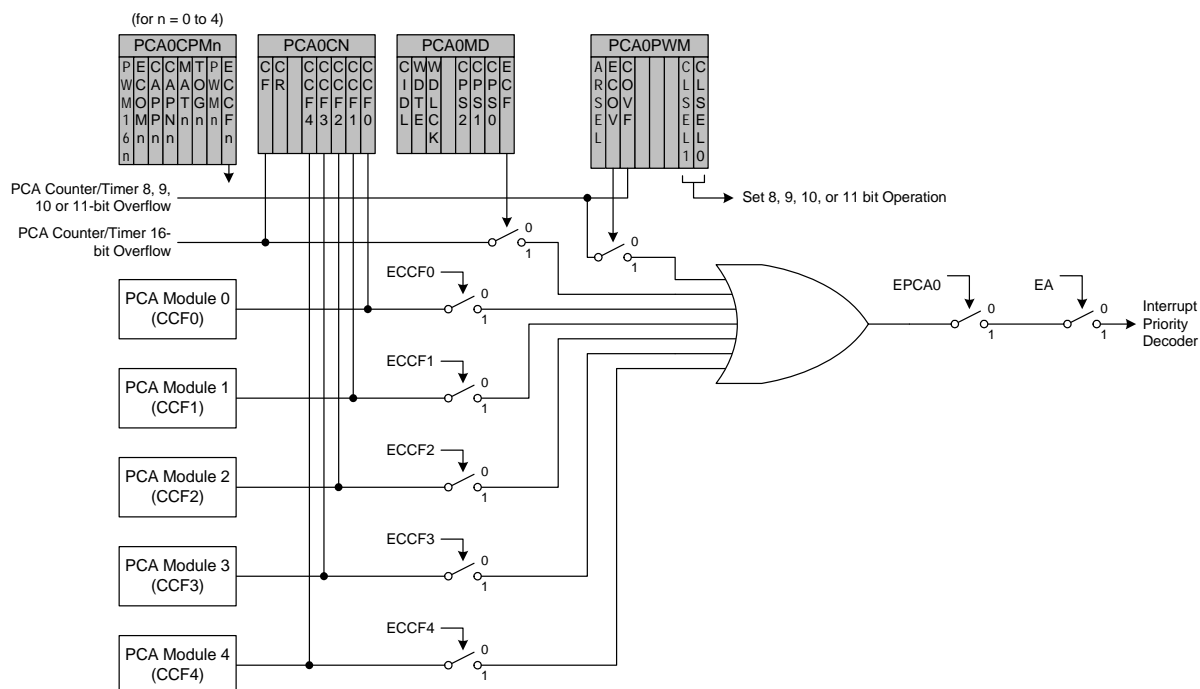


Figure 29.3. PCA Interrupt Block Diagram

29.3. Capture/Compare Modules

Each module can be configured to operate independently in one of six operation modes: Edge-triggered Capture, Software Timer, High Speed Output, Frequency Output, 8 to 11-Bit Pulse Width Modulator, or 16-Bit Pulse Width Modulator. Each module has Special Function Registers (SFRs) associated with it in the CIP-51 system controller. These registers are used to exchange data with a module and configure the module's mode of operation. Table 29.2 summarizes the bit settings in the PCA0CPMn and PCA0PWM registers used to select the PCA capture/compare module's operating mode. Note that all modules set to use 8, 9, 10, or 11-bit PWM mode must use the same cycle length (8-11 bits). Setting the ECCFn bit in a PCA0CPMn register enables the module's CCFn interrupt.

A 0% duty cycle may be generated by clearing the ECOMn bit to 0.

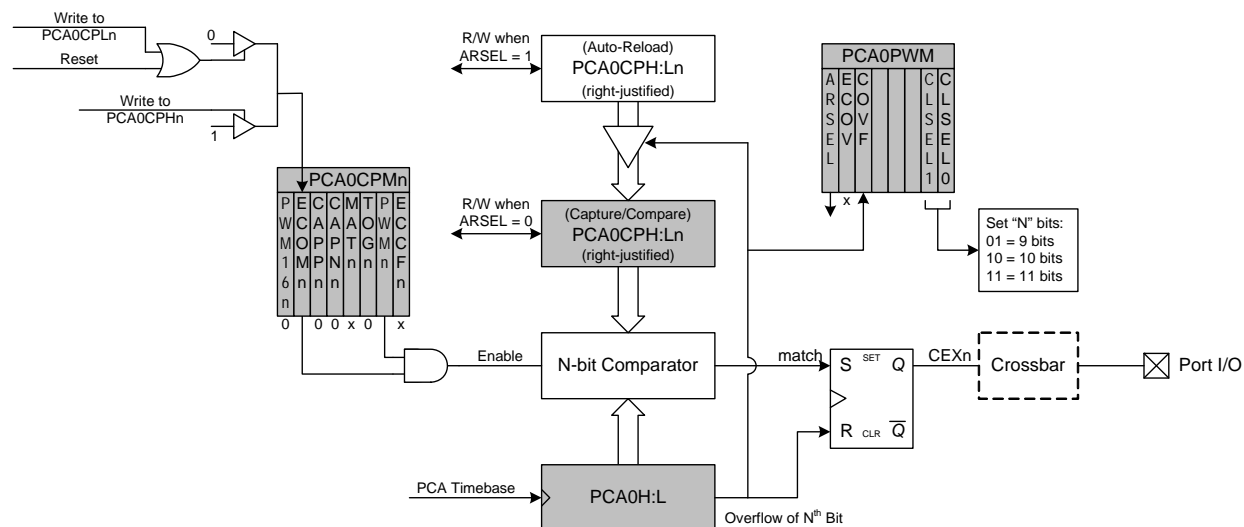


Figure 29.9. PCA 9, 10 and 11-Bit PWM Mode Diagram

29.3.6. 16-Bit Pulse Width Modulator Mode

A PCA module may also be operated in 16-Bit PWM mode. 16-bit PWM mode is independent of the other (8/9/10/11-bit) PWM modes. In this mode, the 16-bit capture/compare module defines the number of PCA clocks for the low time of the PWM signal. When the PCA counter matches the module contents, the output on CEXn is asserted high; when the 16-bit counter overflows, CEXn is asserted low. To output a varying duty cycle, new value writes should be synchronized with PCA CCFn match interrupts. 16-Bit PWM Mode is enabled by setting the ECOMn, PWMn, and PWM16n bits in the PCA0CPMn register. For a varying duty cycle, match interrupts should be enabled (ECCFn = 1 AND MATn = 1) to help synchronize the capture/compare register writes. If the MATn bit is set to 1, the CCFn flag for the module will be set each time a 16-bit comparator match (rising edge) occurs. The CF flag in PCA0CN can be used to detect the overflow (falling edge). The duty cycle for 16-Bit PWM Mode is given by Equation 29.4.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

$$\text{Duty Cycle} = \frac{(65536 - \text{PCA0CPn})}{65536}$$

Equation 29.4. 16-Bit PWM Duty Cycle

Using Equation 29.4, the largest duty cycle is 100% (PCA0CPn = 0), and the smallest duty cycle is 0.0015% (PCA0CPn = 0xFFFF). A 0% duty cycle may be generated by clearing the ECOMn bit to 0.

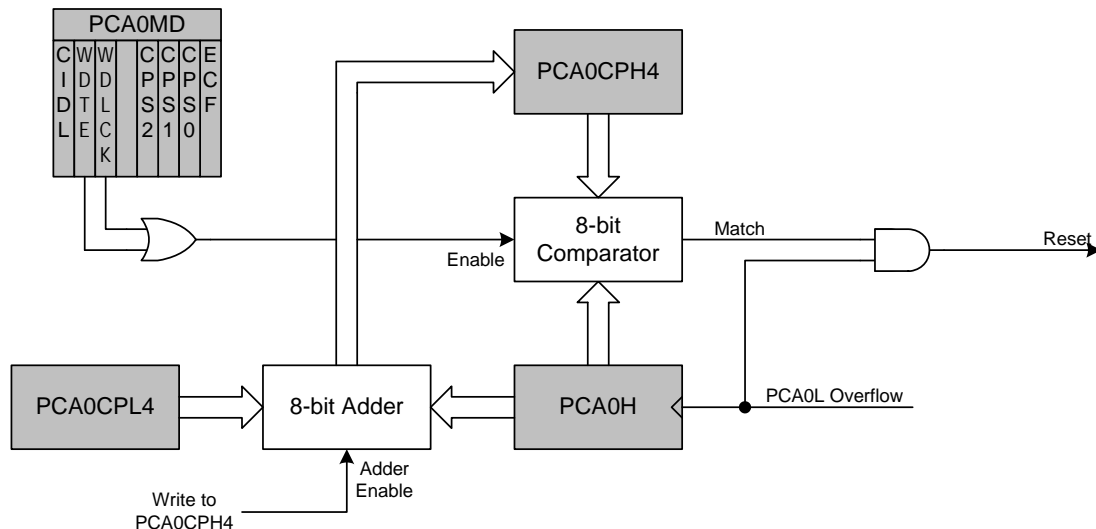


Figure 29.11. PCA Module 2 with Watchdog Timer Enabled

Note that the 8-bit offset held in PCA0CPH4 is compared to the upper byte of the 16-bit PCA counter. This offset value is the number of PCA0L overflows before a reset. Up to 256 PCA clocks may pass before the first PCA0L overflow occurs, depending on the value of the PCA0L when the update is performed. The total offset is then given (in PCA clocks) by Equation 29.5, where PCA0L is the value of the PCA0L register at the time of the update.

$$\text{Offset} = (256 \times \text{PCA0CPL4}) + (256 - \text{PCA0L})$$

Equation 29.5. Watchdog Timer Offset in PCA Clocks

The WDT reset is generated when PCA0L overflows while there is a match between PCA0CPH4 and PCA0H. Software may force a WDT reset by writing a 1 to the CCF4 flag (PCA0CN.4) while the WDT is enabled.

29.4.2. Watchdog Timer Usage

To configure the WDT, perform the following tasks:

- Disable the WDT by writing a 0 to the WDTE bit.
- Select the desired PCA clock source (with the CPS2–CPS0 bits).
- Load PCA0CPL4 with the desired WDT update offset value.
- Configure the PCA Idle mode (set CIDL if the WDT should be suspended while the CPU is in Idle mode).
- Enable the WDT by setting the WDTE bit to 1.
- Reset the WDT timer by writing to PCA0CPH4.

The PCA clock source and Idle mode select cannot be changed while the WDT is enabled. The watchdog timer is enabled by setting the WDTE or WDLCK bits in the PCA0MD register. When WDLCK is set, the WDT cannot be disabled until the next system reset. If WDLCK is not set, the WDT is disabled by clearing the WDTE bit.

The WDT is enabled following any reset. The PCA0 counter clock defaults to the system clock divided by 12, PCA0L defaults to 0x00, and PCA0CPL4 defaults to 0x00. Using Equation 29.5, this results in a WDT timeout interval of 256 PCA clock cycles, or 3072 system clock cycles. Table 29.3 lists some example tim-

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SFR Definition 29.2. PCA0MD: PCA Mode

Bit	7	6	5	4	3	2	1	0
Name	CIDL	WDTE	WDLCK		CPS2	CPS1	CPS0	ECF
Type	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

SFR Address = 0xD9

Bit	Name	Function
7	CIDL	PCA Counter/Timer Idle Control. Specifies PCA behavior when CPU is in Idle Mode. 0: PCA continues to function normally while the system controller is in Idle Mode. 1: PCA operation is suspended while the system controller is in Idle Mode.
6	WDTE	Watchdog Timer Enable. If this bit is set, PCA Module 4 is used as the watchdog timer. 0: Watchdog Timer disabled. 1: PCA Module 4 enabled as Watchdog Timer.
5	WDLCK	Watchdog Timer Lock. This bit locks/unlocks the Watchdog Timer Enable. When WDLCK is set, the Watchdog Timer may not be disabled until the next system reset. 0: Watchdog Timer Enable unlocked. 1: Watchdog Timer Enable locked.
4	Unused	Read = 0b, Write = Don't care.
3:1	CPS[2:0]	PCA Counter/Timer Pulse Select. These bits select the timebase source for the PCA counter 000: System clock divided by 12 001: System clock divided by 4 010: Timer 0 overflow 011: High-to-low transitions on ECI (max rate = system clock divided by 4) 100: System clock 101: External clock divided by 8 (synchronized with the system clock) 11x: Reserved
0	ECF	PCA Counter/Timer Overflow Interrupt Enable. This bit sets the masking of the PCA Counter/Timer Overflow (CF) interrupt. 0: Disable the CF interrupt. 1: Enable a PCA Counter/Timer Overflow interrupt request when CF (PCA0CN.7) is set.
Note: When the WDTE bit is set to 1, the other bits in the PCA0MD register cannot be modified. To change the contents of the PCA0MD register, the Watchdog Timer must first be disabled.		

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C2 Register Definition 30.2. DEVICEID: C2 Device ID

Bit	7	6	5	4	3	2	1	0
Name	DEVICEID[7:0]							
Type	R/W							
Reset	Varies	Varies	Varies	Varies	Varies	Varies	Varies	Varies

C2 Address: 0x00

Bit	Name	Function
7:0	DEVICEID[7:0]	Device ID. This read-only register returns the 8-bit device ID: 0x18 (C8051T620/621/320/321/322/323). 0x2C (C8051T626/627).

C2 Register Definition 30.3. REVID: C2 Revision ID

Bit	7	6	5	4	3	2	1	0
Name	REVID[7:0]							
Type	R/W							
Reset	Varies	Varies	Varies	Varies	Varies	Varies	Varies	Varies

C2 Address: 0x01

Bit	Name	Function
7:0	REVID[7:0]	Revision ID. This read-only register returns the 8-bit revision ID. For example: 0x00 = Revision A.