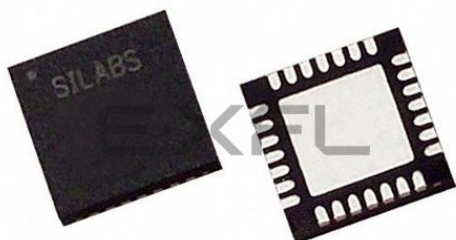


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Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	48 MIPS
Connectivity	I ² C, SPI, UART/USART, USB
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 21x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VFQFN Exposed Pad
Supplier Device Package	28-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051t321-gmr

C8051T620/1/6/7 & C8051T320/1/2/3

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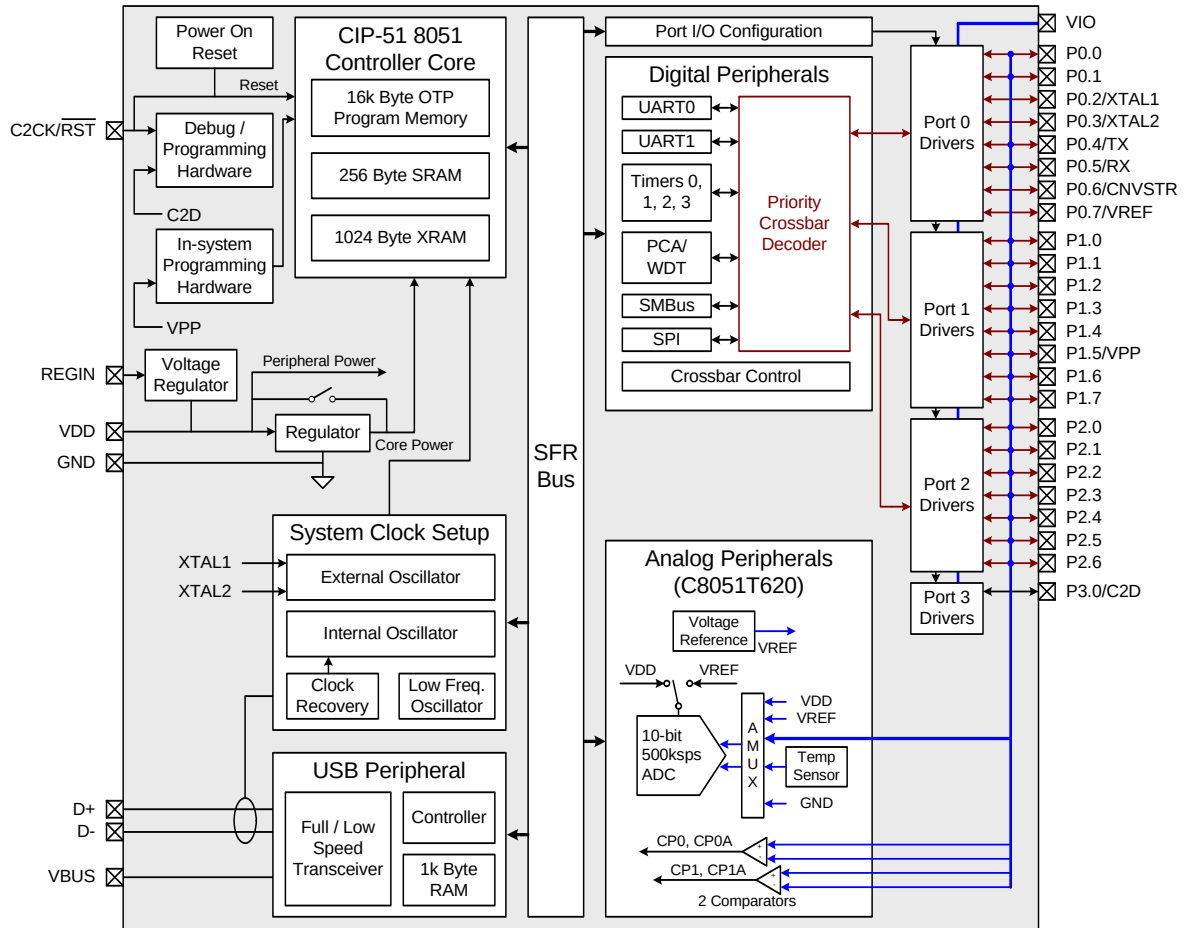


Figure 1.1. C8051T620/1 Block Diagram

C8051T620/1/6/7 & C8051T320/1/2/3

8.4.1. Window Detector Example

Figure 8.4 shows two example window comparisons for right-justified data, with $ADC0LTH:ADC0LTL = 0x0080$ (128d) and $ADC0GTH:ADC0GTL = 0x0040$ (64d). The input voltage can range from 0 to $VREF \times (1023/1024)$ with respect to GND, and is represented by a 10-bit unsigned integer value. In the left example, an $AD0WINT$ interrupt will be generated if the $ADC0$ conversion word ($ADC0H:ADC0L$) is within the range defined by $ADC0GTH:ADC0GTL$ and $ADC0LTH:ADC0LTL$ (if $0x0040 < ADC0H:ADC0L < 0x0080$). In the right example, an $AD0WINT$ interrupt will be generated if the $ADC0$ conversion word is outside of the range defined by the $ADC0GT$ and $ADC0LT$ registers (if $ADC0H:ADC0L < 0x0040$ or $ADC0H:ADC0L > 0x0080$). Figure 8.5 shows an example using left-justified data with the same comparison values.

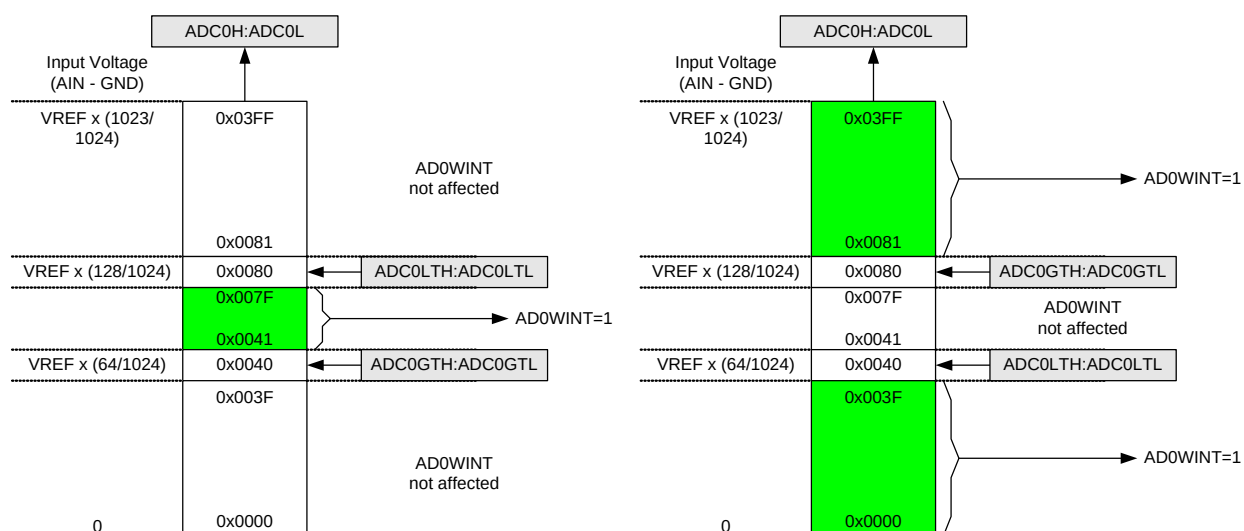


Figure 8.4. ADC Window Compare Example: Right-Justified Data

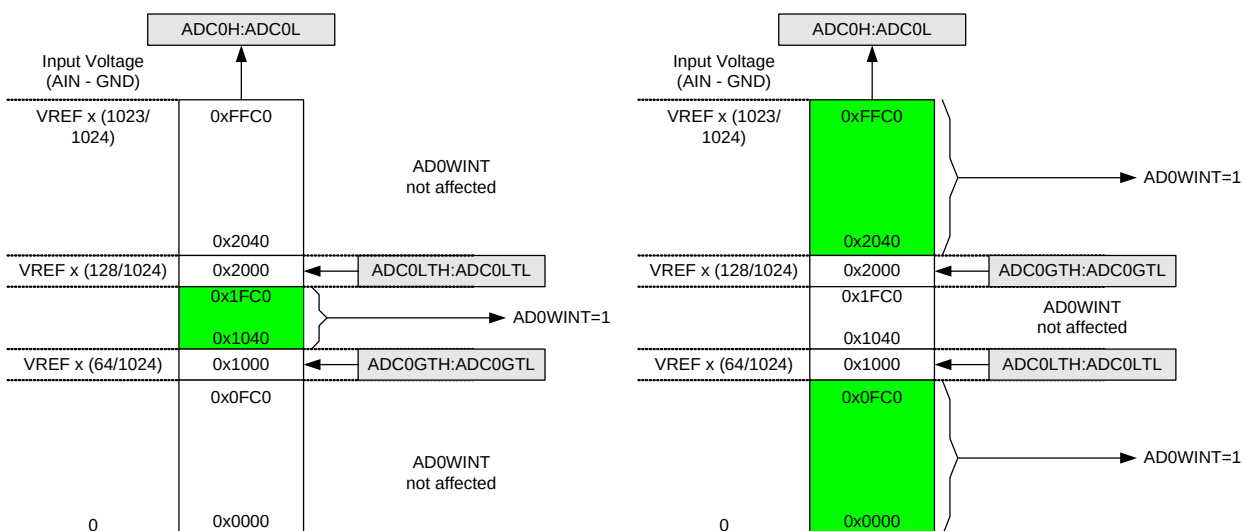


Figure 8.5. ADC Window Compare Example: Left-Justified Data

C8051T620/1/6/7 & C8051T320/1/2/3

SFR Definition 10.1. REF0CN: Reference Control

Bit	7	6	5	4	3	2	1	0
Name	REFBGS			REGOVR	REFSL	TEMPE	BIASE	REFBE
Type	R/W	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD1

Bit	Name	Function
7	REFBGS	Reference Buffer Gain Select. This bit selects between 1x and 2x gain for the on-chip voltage reference buffer. 0: 2x Gain 1: 1x Gain
6:5	Unused	Read = 00b; Write = don't care.
4	REGOVR	Regulator Reference Override. This bit "overrides" the REFSL bit, and allows the internal regulator to be used as a reference source. 0: The voltage reference source is selected by the REFSL bit. 1: The internal regulator is used as the voltage reference.
3	REFSL	Voltage Reference Select. This bit selects the ADCs voltage reference. 0: V_{REF} pin used as voltage reference. 1: V_{DD} used as voltage reference.
2	TEMPE	Temperature Sensor Enable Bit. 0: Internal Temperature Sensor off. 1: Internal Temperature Sensor on.
1	BIASE	Internal Analog Bias Generator Enable Bit. 0: Internal Bias Generator off. 1: Internal Bias Generator on.
0	REFBE	On-chip Reference Buffer Enable Bit. 0: On-chip Reference Buffer off. 1: On-chip Reference Buffer on. Internal voltage reference driven on the V_{REF} pin.

C8051T620/1/6/7 & C8051T320/1/2/3

15. Memory Organization

The memory organization of the CIP-51 System Controller is similar to that of a standard 8051. There are two separate memory spaces: program memory and data memory. Program and data memory share the same address space but are accessed via different instruction types. The memory organization of the C8051T620/1/6/7 & C8051T320/1/2/3 device family is shown in Figure 15.1

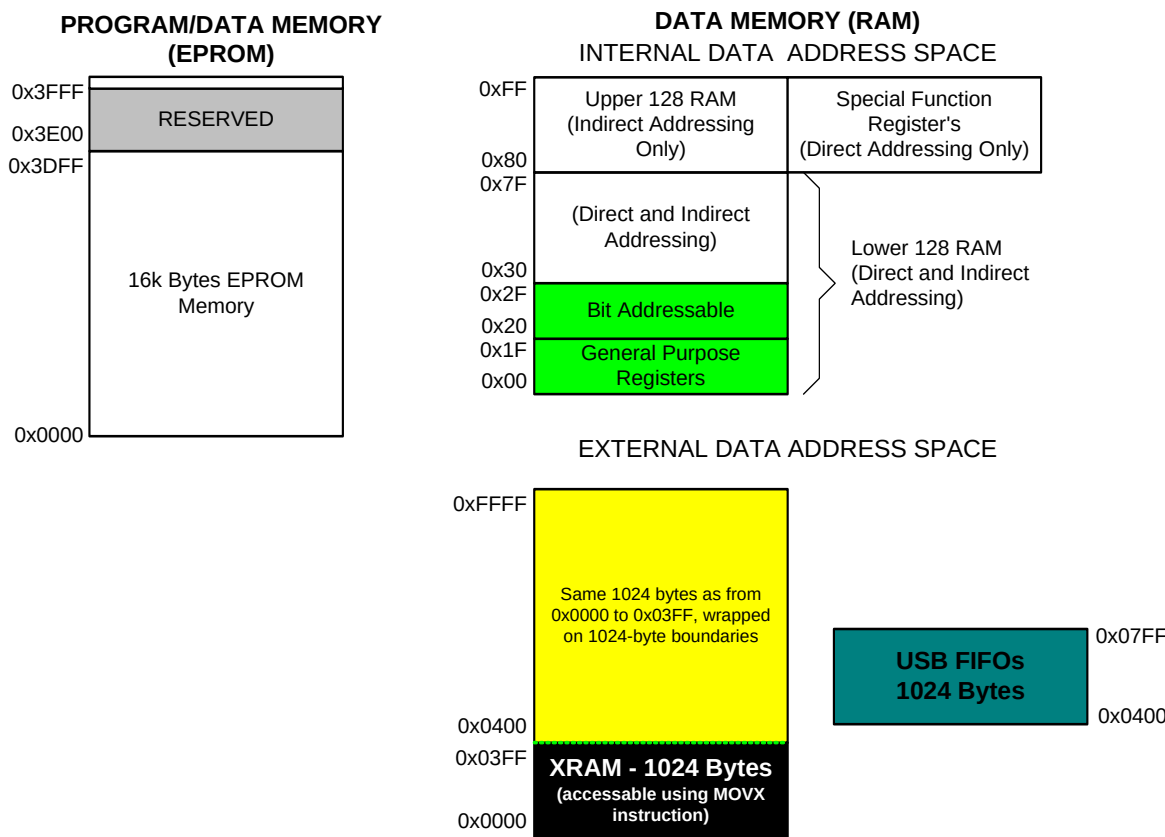


Figure 15.1. C8051T620/1 and C8051T320/1/2/3 Memory Map

C8051T620/1/6/7 & C8051T320/1/2/3

16. Special Function Registers

The direct-access data memory locations from 0x80 to 0xFF constitute the special function registers (SFRs). The SFRs provide control and data exchange with the C8051T620/1/6/7 & C8051T320/1/2/3's resources and peripherals. The CIP-51 controller core duplicates the SFRs found in a typical 8051 implementation as well as implementing additional SFRs used to configure and access the sub-systems unique to the C8051T620/1/6/7 & C8051T320/1/2/3. This allows the addition of new functionality while retaining compatibility with the MCS-51™ instruction set. Table 16.1 lists the SFRs implemented in the C8051T620/1/6/7 & C8051T320/1/2/3 device family.

The SFR registers are accessed anytime the direct addressing mode is used to access memory locations from 0x80 to 0xFF. SFRs with addresses ending in 0x0 or 0x8 (e.g., P0, TCON, SCON0, IE, etc.) are bit-addressable as well as byte-addressable. All other SFRs are byte-addressable only. Unoccupied addresses in the SFR space are reserved for future use. Accessing these areas will have an indeterminate effect and should be avoided. Refer to the corresponding pages of the data sheet, as indicated in Table 16.2, for a detailed description of each register.

Table 16.1. Special Function Register (SFR) Memory Map

F8	SPI0CN	PCA0L	PCA0H	PCA0CPL0	PCA0CPH0	PCA0CPL4	PCA0CPH4	VDM0CN
F0	B	P0MDIN	P1MDIN	P2MDIN	PCA0PWM	IAPCN	EIP1	EIP2
E8	ADC0CN	PCA0CPL1	PCA0CPH1	PCA0CPL2	PCA0CPH2	PCA0CPL3	PCA0CPH3	RSTSRC
E0	ACC	XBR0	XBR1	XBR2	IT01CF	SMOD1	EIE1	EIE2
D8	PCA0CN	PCA0MD	PCA0CPM0	PCA0CPM1	PCA0CPM2	PCA0CPM3	PCA0CPM4	-
D0	PSW	REF0CN	SCON1	SBUF1	P0SKIP	P1SKIP	P2SKIP	USB0XCN
C8	TMR2CN	REG01CN	TMR2RLL	TMR2RLH	TMR2L	TMR2H	-	SMB0ADM
C0	SMB0CN	SMB0CF	SMB0DAT	ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH	SMB0ADR
B8	IP	CLKMUL	P1MASK	AMX0P	ADC0CF	ADC0L	ADC0H	-
B0	P3	OSCXCN	OSCI CN	OSCI CL	SBRL1	SBRLH1	P1MAT	MEMKEY
A8	IE	CLKSEL	EMI0CN	-	SB CON1	-	P0MASK	PFE0CN
A0	P2	SPI0CFG	SPI0CKR	SPI0DAT	P0MDOUT	P1MDOUT	P2MDOUT	P3MDOUT
98	SCON0	SBUF0	CPT1CN	CPT0CN	CPT1MD	CPT0MD	CPT1MX	CPT0MX
90	P1	TMR3CN	TMR3RLL	TMR3RLH	TMR3L	TMR3H	USB0ADR	USB0DAT
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	PSCTL
80	P0	SP	DPL	DPH	P0MAT	EMI0CF	OSCLCN	PCON
	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

Note: SFR Addresses ending in 0x0 or 0x8 are bit-addressable locations and can be used with bitwise instructions.

C8051T620/1/6/7 & C8051T320/1/2/3

SFR Definition 17.3. EIE1: Extended Interrupt Enable 1

Bit	7	6	5	4	3	2	1	0
Name	ET3	ECP1	ECP0	EPCA0	EADC0	EWADC0	EUSB0	ESMB0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE6

Bit	Name	Function
7	ET3	Enable Timer 3 Interrupt. This bit sets the masking of the Timer 3 interrupt. 0: Disable Timer 3 interrupts. 1: Enable interrupt requests generated by the TF3L or TF3H flags.
6	ECP1	Enable Comparator1 (CP1) Interrupt. This bit sets the masking of the CP1 interrupt. 0: Disable CP1 interrupts. 1: Enable interrupt requests generated by the CP1RIF or CP1FIF flags.
5	ECP0	Enable Comparator0 (CP0) Interrupt. This bit sets the masking of the CP0 interrupt. 0: Disable CP0 interrupts. 1: Enable interrupt requests generated by the CP0RIF or CP0FIF flags.
4	EPCA0	Enable Programmable Counter Array (PCA0) Interrupt. This bit sets the masking of the PCA0 interrupts. 0: Disable all PCA0 interrupts. 1: Enable interrupt requests generated by PCA0.
3	EADC0	Enable ADC0 Conversion Complete Interrupt. This bit sets the masking of the ADC0 Conversion Complete interrupt. 0: Disable ADC0 Conversion Complete interrupt. 1: Enable interrupt requests generated by the AD0INT flag.
2	EWADC0	Enable Window Comparison ADC0 Interrupt. This bit sets the masking of ADC0 Window Comparison interrupt. 0: Disable ADC0 Window Comparison interrupt. 1: Enable interrupt requests generated by ADC0 Window Compare flag (AD0WINT).
1	EUSB0	Enable USB (USB0) Interrupt. This bit sets the masking of the USB0 interrupt. 0: Disable all USB0 interrupts. 1: Enable interrupt requests generated by USB0.
0	ESMB0	Enable SMBus (SMB0) Interrupt. This bit sets the masking of the SMB0 interrupt. 0: Disable all SMB0 interrupts. 1: Enable interrupt requests generated by SMB0.

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USB Register Definition 23.16. CMIE: USB0 Common Interrupt Enable

Bit	7	6	5	4	3	2	1	0
Name					SOFE	RSTINTE	RSUINTE	SUSINTE
Type	R	R	R	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	1	0

USB Register Address = 0x0B

Bit	Name	Function
7:4	Unused	Read = 0000b. Write = don't care.
3	SOFE	Start of Frame Interrupt Enable. 0: SOF interrupt disabled. 1: SOF interrupt enabled.
2	RSTINTE	Reset Interrupt Enable. 0: Reset interrupt disabled. 1: Reset interrupt enabled.
1	RSUINTE	Resume Interrupt Enable. 0: Resume interrupt disabled. 1: Resume interrupt enabled.
0	SUSINTE	Suspend Interrupt Enable. 0: Suspend interrupt disabled. 1: Suspend interrupt enabled.

23.9. The Serial Interface Engine

The Serial Interface Engine (SIE) performs all low level USB protocol tasks, interrupting the processor when data has successfully been transmitted or received. When receiving data, the SIE will interrupt the processor when a complete data packet has been received; appropriate handshaking signals are automatically generated by the SIE. When transmitting data, the SIE will interrupt the processor when a complete data packet has been transmitted and the appropriate handshake signal has been received.

The SIE will not interrupt the processor when corrupted/erroneous packets are received.

23.10. Endpoint0

Endpoint0 is managed through the USB register E0CSR (USB Register Definition 23.18). The INDEX register must be loaded with 0x00 to access the E0CSR register.

An Endpoint0 interrupt is generated when:

1. A data packet (OUT or SETUP) has been received and loaded into the Endpoint0 FIFO. The OPRDY bit (E0CSR.0) is set to 1 by hardware.
2. An IN data packet has successfully been unloaded from the Endpoint0 FIFO and transmitted to the host; INPRDY is reset to 0 by hardware.
3. An IN transaction is completed (this interrupt generated during the status stage of the transaction).
4. Hardware sets the STSTL bit (E0CSR.2) after a control transaction ended due to a protocol violation.

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5. Hardware sets the SUEND bit (E0CSR.4) because a control transfer ended before firmware sets the DATAEND bit (E0CSR.3).

The E0CNT register (USB Register Definition 23.11) holds the number of received data bytes in the Endpoint0 FIFO.

Hardware will automatically detect protocol errors and send a STALL condition in response. Firmware may force a STALL condition to abort the current transfer. When a STALL condition is generated, the STSTL bit will be set to 1 and an interrupt generated. The following conditions will cause hardware to generate a STALL condition:

1. The host sends an OUT token during a OUT data phase after the DATAEND bit has been set to 1.
2. The host sends an IN token during an IN data phase after the DATAEND bit has been set to 1.
3. The host sends a packet that exceeds the maximum packet size for Endpoint0.
4. The host sends a non-zero length DATA1 packet during the status phase of an IN transaction.

Firmware sets the SDSTL bit (E0CSR.5) to 1.

23.10.1. Endpoint0 SETUP Transactions

All control transfers must begin with a SETUP packet. SETUP packets are similar to OUT packets, containing an 8-byte data field sent by the host. Any SETUP packet containing a command field of anything other than 8 bytes will be automatically rejected by USB0. An Endpoint0 interrupt is generated when the data from a SETUP packet is loaded into the Endpoint0 FIFO. Software should unload the command from the Endpoint0 FIFO, decode the command, perform any necessary tasks, and set the SOPRDY bit to indicate that it has serviced the OUT packet.

23.10.2. Endpoint0 IN Transactions

When a SETUP request is received that requires USB0 to transmit data to the host, one or more IN requests will be sent by the host. For the first IN transaction, firmware should load an IN packet into the Endpoint0 FIFO, and set the INPRDY bit (E0CSR.1). An interrupt will be generated when an IN packet is transmitted successfully. Note that no interrupt will be generated if an IN request is received before firmware has loaded a packet into the Endpoint0 FIFO. If the requested data exceeds the maximum packet size for Endpoint0 (as reported to the host), the data should be split into multiple packets; each packet should be of the maximum packet size excluding the last (residual) packet. If the requested data is an integer multiple of the maximum packet size for Endpoint0, the last data packet should be a zero-length packet signaling the end of the transfer. Firmware should set the DATAEND bit to 1 after loading into the Endpoint0 FIFO the last data packet for a transfer.

Upon reception of the first IN token for a particular control transfer, Endpoint0 is said to be in Transmit Mode. In this mode, only IN tokens should be sent by the host to Endpoint0. The SUEND bit (E0CSR.4) is set to 1 if a SETUP or OUT token is received while Endpoint0 is in Transmit Mode.

Endpoint0 will remain in Transmit Mode until any of the following occur:

1. USB0 receives an Endpoint0 SETUP or OUT token.
2. Firmware sends a packet less than the maximum Endpoint0 packet size.
3. Firmware sends a zero-length packet.

Firmware should set the DATAEND bit (E0CSR.3) to 1 when performing (2) and (3) above.

The SIE will transmit a NAK in response to an IN token if there is no packet ready in the IN FIFO (INPRDY = 0).

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25.2. Operational Modes

UART0 provides standard asynchronous, full duplex communication. The UART mode (8-bit or 9-bit) is selected by the S0MODE bit (SCON0.7). Typical UART connection options are shown in Figure 25.3.

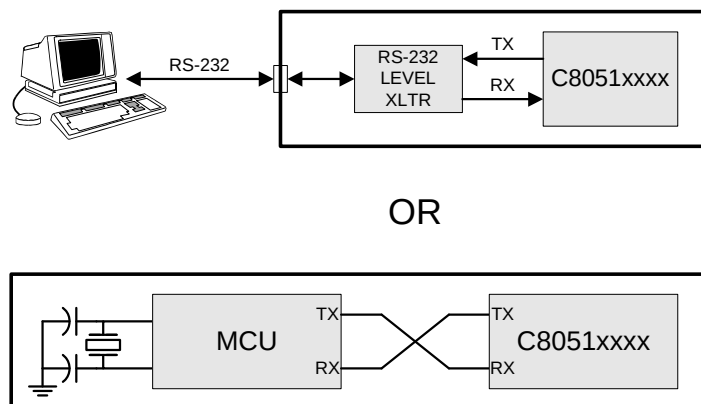


Figure 25.3. UART Interconnect Diagram

25.2.1. 8-Bit UART

8-Bit UART mode uses a total of 10 bits per data byte: one start bit, eight data bits (LSB first), and one stop bit. Data are transmitted LSB first from the TX0 pin and received at the RX0 pin. On receive, the eight data bits are stored in SBUF0 and the stop bit goes into RB80 (SCON0.2).

Data transmission begins when software writes a data byte to the SBUF0 register. The TIO Transmit Interrupt Flag (SCON0.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN0 Receive Enable bit (SCON0.4) is set to logic 1. After the stop bit is received, the data byte will be loaded into the SBUF0 receive register if the following conditions are met: RI0 must be logic 0, and if MCE0 is logic 1, the stop bit must be logic 1. In the event of a receive data overrun, the first received 8 bits are latched into the SBUF0 receive register and the following overrun data bits are lost.

If these conditions are met, the eight bits of data is stored in SBUF0, the stop bit is stored in RB80 and the RI0 flag is set. If these conditions are not met, SBUF0 and RB80 will not be loaded and the RI0 flag will not be set. An interrupt will occur if enabled when either TIO or RI0 is set.

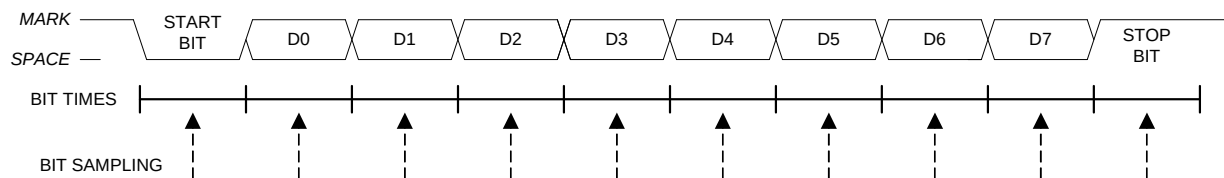


Figure 25.4. 8-Bit UART Timing Diagram

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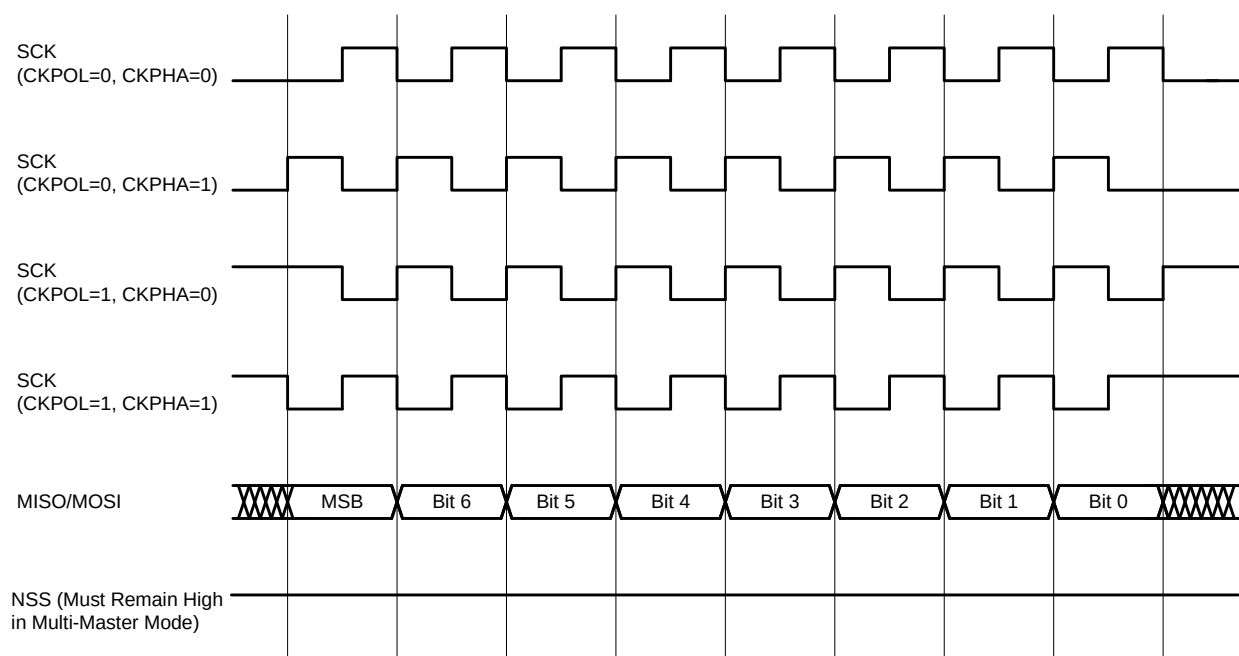


Figure 27.5. Master Mode Data/Clock Timing

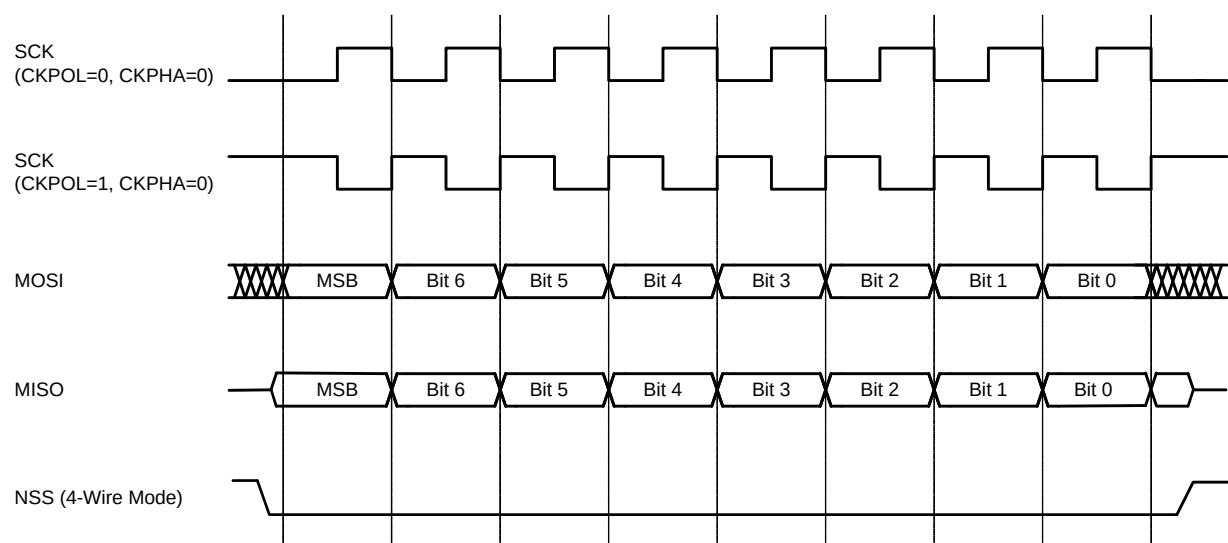
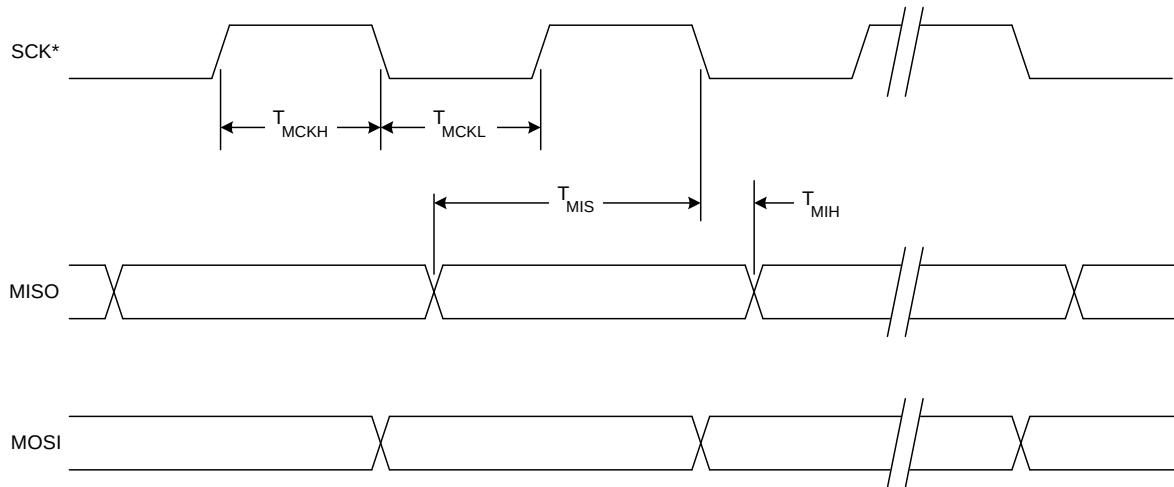


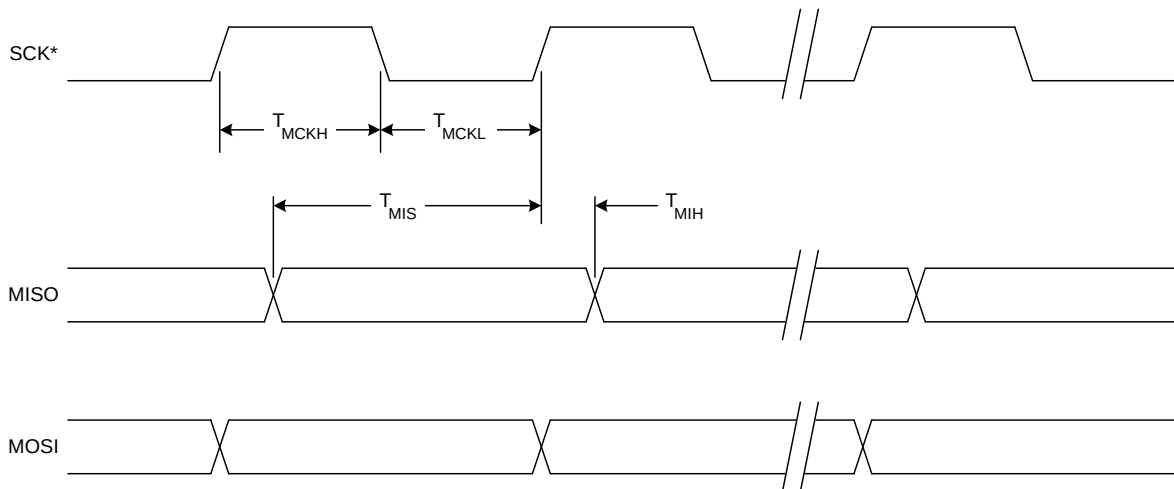
Figure 27.6. Slave Mode Data/Clock Timing (CKPHA = 0)

C8051T620/1/6/7 & C8051T320/1/2/3



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 27.8. SPI Master Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 27.9. SPI Master Timing (CKPHA = 1)

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SFR Definition 28.2. TCON: Timer Control

Bit	7	6	5	4	3	2	1	0
Name	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x88; Bit-Addressable

Bit	Name	Function
7	TF1	Timer 1 Overflow Flag. Set to 1 by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.
6	TR1	Timer 1 Run Control. Timer 1 is enabled by setting this bit to 1.
5	TF0	Timer 0 Overflow Flag. Set to 1 by hardware when Timer 0 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.
4	TR0	Timer 0 Run Control. Timer 0 is enabled by setting this bit to 1.
3	IE1	External Interrupt 1. This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine in edge-triggered mode.
2	IT1	Interrupt 1 Type Select. This bit selects whether the configured $\overline{\text{INT1}}$ interrupt will be edge or level sensitive. $\overline{\text{INT1}}$ is configured active low or high by the IN1PL bit in the IT01CF register (see SFR Definition 17.7). 0: $\overline{\text{INT1}}$ is level triggered. 1: $\overline{\text{INT1}}$ is edge triggered.
1	IE0	External Interrupt 0. This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine in edge-triggered mode.
0	IT0	Interrupt 0 Type Select. This bit selects whether the configured $\overline{\text{INT0}}$ interrupt will be edge or level sensitive. $\overline{\text{INT0}}$ is configured active low or high by the IN0PL bit in register IT01CF (see SFR Definition 17.7). 0: $\overline{\text{INT0}}$ is level triggered. 1: $\overline{\text{INT0}}$ is edge triggered.

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28.2.3. Low-Frequency Oscillator (LFO) Capture Mode

The Low-Frequency Oscillator Capture Mode allows the LFO clock to be measured against the system clock or an external oscillator source. Timer 2 can be clocked from the system clock, the system clock divided by 12, or the external oscillator divided by 8, depending on the T2ML (CKCON.4), and T2XCLK settings.

Setting TF2CEN to 1 enables the LFO Capture Mode for Timer 2. In this mode, T2SPLIT should be set to 0, as the full 16-bit timer is used. Upon a falling edge of the low-frequency oscillator, the contents of Timer 2 (TMR2H:TMR2L) are loaded into the Timer 2 reload registers (TMR2RLH:TMR2RLL) and the TF2H flag is set. By recording the difference between two successive timer capture values, the LFO clock frequency can be determined with respect to the Timer 2 clock. The Timer 2 clock should be much faster than the LFO to achieve an accurate reading.

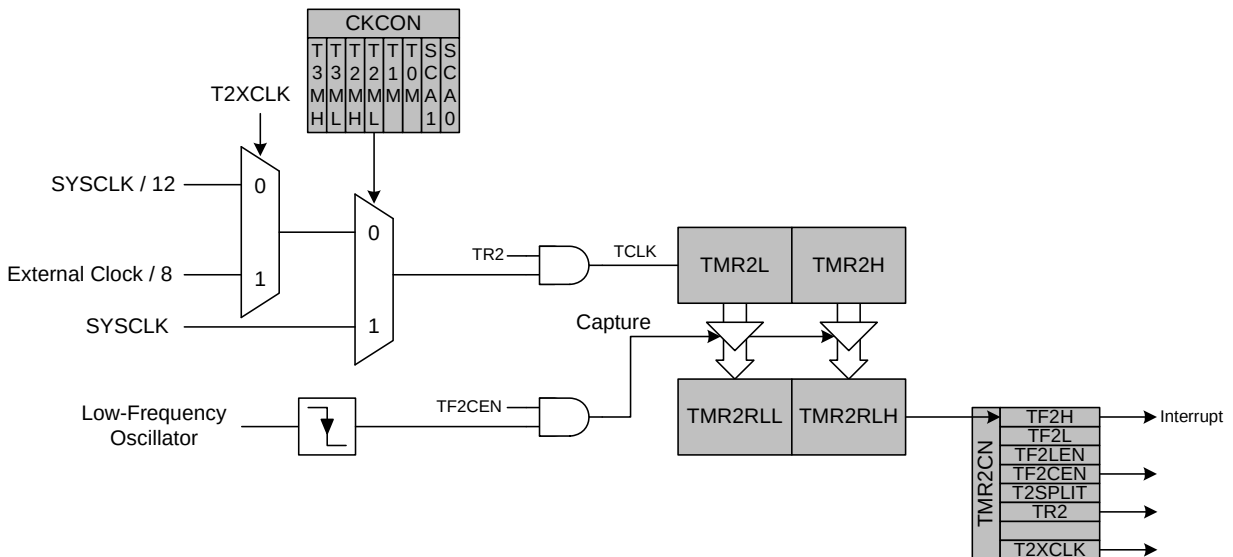


Figure 28.6. Timer 2 Low-Frequency Oscillation Capture Mode Block Diagram

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28.3.3. Low-Frequency Oscillator (LFO) Capture Mode

The Low-Frequency Oscillator Capture Mode allows the LFO clock to be measured against the system clock or an external oscillator source. Timer 3 can be clocked from the system clock, the system clock divided by 12, or the external oscillator divided by 8, depending on the T3ML (CKCON.6), and T3XCLK[1:0] settings.

Setting TF3CEN to 1 enables the LFO Capture Mode for Timer 3. In this mode, T3SPLIT should be set to 0, as the full 16-bit timer is used. Upon a falling edge of the low-frequency oscillator, the contents of Timer 3 (TMR3H:TMR3L) are loaded into the Timer 3 reload registers (TMR3RLH:TMR3RLL) and the TF3H flag is set. By recording the difference between two successive timer capture values, the LFO clock frequency can be determined with respect to the Timer 3 clock. The Timer 3 clock should be much faster than the LFO to achieve an accurate reading. This means that the LFO/8 should not be selected as the timer clock source in this mode.

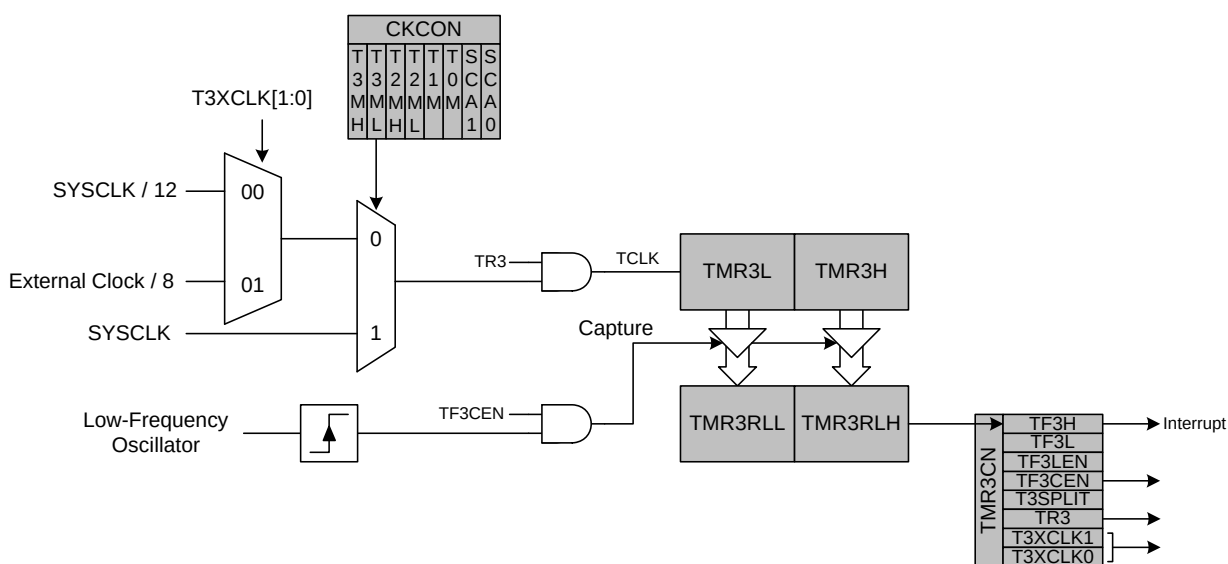


Figure 28.9. Timer 3 Low-Frequency Oscillation Capture Mode Block Diagram

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SFR Definition 28.13. TMR3CN: Timer 3 Control

Bit	7	6	5	4	3	2	1	0
Name	TF3H	TF3L	TF3LEN	TF3CEN	T3SPLIT	TR3	T3XCLK[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x91

Bit	Name	Function
7	TF3H	Timer 3 High Byte Overflow Flag. Set by hardware when the Timer 3 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 3 overflows from 0xFFFF to 0x0000. When the Timer 3 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 3 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF3L	Timer 3 Low Byte Overflow Flag. Set by hardware when the Timer 3 low byte overflows from 0xFF to 0x00. TF3L will be set when the low byte overflows regardless of the Timer 3 mode. This bit is not automatically cleared by hardware.
5	TF3LEN	Timer 3 Low Byte Interrupt Enable. When set to 1, this bit enables Timer 3 Low Byte interrupts. If Timer 3 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 3 overflows.
4	TF3CEN	Timer 3 Low-Frequency Oscillator Capture Enable. When set to 1, this bit enables Timer 3 Low-Frequency Oscillator Capture Mode. If TF3CEN is set and Timer 3 interrupts are enabled, an interrupt will be generated on a falling edge of the low-frequency oscillator output, and the current 16-bit timer value in TMR3H:TMR3L will be copied to TMR3RLH:TMR3RLL.
3	T3SPLIT	Timer 3 Split Mode Enable. When this bit is set, Timer 3 operates as two 8-bit timers with auto-reload. 0: Timer 3 operates in 16-bit auto-reload mode. 1: Timer 3 operates as two 8-bit auto-reload timers.
2	TR3	Timer 3 Run Control. Timer 3 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR3H only; TMR3L is always enabled in split mode.
1:0	T3XCLK[1:0]	Timer 3 External Clock Select. This bit selects the “external” clock source for Timer 3. If Timer 3 is in 8-bit mode, this bit selects the external oscillator clock source for both timer bytes. However, the Timer 3 Clock Select bits (T3MH and T3ML in register CKCON) may still be used to select between the external clock and the system clock for either timer. 00: System clock divided by 12. 01: External clock divided by 8 (synchronized with SYSCLK when not in suspend). 10: Reserved. 11: Internal LFO/8 (synchronized with SYSCLK when not in suspend).

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SFR Definition 29.4. PCA0CPMn: PCA Capture/Compare Mode

Bit	7	6	5	4	3	2	1	0
Name	PWM16n	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Addresses: 0xDA (n = 0), 0xDB (n = 1), 0xDC (n = 2), 0xDD (n = 3), 0xDE (n = 4)

Bit	Name	Function
7	PWM16n	16-bit Pulse Width Modulation Enable. This bit enables 16-bit mode when Pulse Width Modulation mode is enabled. 0: 8 to 11-bit PWM selected. 1: 16-bit PWM selected.
6	ECOMn	Comparator Function Enable. This bit enables the comparator function for PCA module n when set to 1.
5	CAPPn	Capture Positive Function Enable. This bit enables the positive edge capture for PCA module n when set to 1.
4	CAPNn	Capture Negative Function Enable. This bit enables the negative edge capture for PCA module n when set to 1.
3	MATn	Match Function Enable. This bit enables the match function for PCA module n when set to 1. When enabled, matches of the PCA counter with a module's capture/compare register cause the CCFn bit in PCA0MD register to be set to logic 1.
2	TOGn	Toggle Function Enable. This bit enables the toggle function for PCA module n when set to 1. When enabled, matches of the PCA counter with a module's capture/compare register cause the logic level on the CEXn pin to toggle. If the PWMn bit is also set to logic 1, the module operates in Frequency Output Mode.
1	PWMn	Pulse Width Modulation Mode Enable. This bit enables the PWM function for PCA module n when set to 1. When enabled, a pulse width modulated signal is output on the CEXn pin. 8 to 11-bit PWM is used if PWM16n is cleared; 16-bit mode is used if PWM16n is set to logic 1. If the TOGn bit is also set, the module operates in Frequency Output Mode.
0	ECCFn	Capture/Compare Flag Interrupt Enable. This bit sets the masking of the Capture/Compare Flag (CCFn) interrupt. 0: Disable CCFn interrupts. 1: Enable a Capture/Compare Flag interrupt request when CCFn is set.
Note: When the WDTE bit is set to 1, the PCA0CPM4 register cannot be modified, and module 4 acts as the watchdog timer. To change the contents of the PCA0CPM4 register or the function of module 4, the Watchdog Timer must be disabled.		

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30. C2 Interface

C8051T620/1/6/7 & C8051T320/1/2/3 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow EPROM programming and in-system debugging with the production part installed in the end application. The C2 interface operates using only two pins: a bi-directional data signal (C2D), and a clock input (C2CK). See the C2 Interface Specification for details on the C2 protocol.

30.1. C2 Interface Registers

The following describes the C2 registers necessary to perform EPROM programming functions through the C2 interface. All C2 registers are accessed through the C2 interface as described in the C2 Interface Specification.

C2 Register Definition 30.1. C2ADD: C2 Address

Bit	7	6	5	4	3	2	1	0
Name	C2ADD[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function																																							
7:0	C2ADD[7:0]	Write: C2 Address. Selects the target Data register for C2 Data Read and Data Write commands according to the following list. <table><tr><th>Address</th><th>Name</th><th>Description</th></tr><tr><td>0x00</td><td>DEVICEID</td><td>Selects the Device ID Register (read only)</td></tr><tr><td>0x01</td><td>REVID</td><td>Selects the Revision ID Register (read only)</td></tr><tr><td>0x02</td><td>DEVCTL</td><td>Selects the C2 Device Control Register</td></tr><tr><td>0xDF</td><td>EPCTL</td><td>Selects the C2 EPROM Programming Control Register</td></tr><tr><td>0xBF</td><td>EPDAT</td><td>Selects the C2 EPROM Data Register</td></tr><tr><td>0xB7</td><td>EPSTAT</td><td>Selects the C2 EPROM Status Register</td></tr><tr><td>0xAF</td><td>EPADDRH</td><td>Selects the C2 EPROM Address High Byte Register</td></tr><tr><td>0xAE</td><td>EPADDRL</td><td>Selects the C2 EPROM Address Low Byte Register</td></tr><tr><td>0xA9</td><td>CRC0</td><td>Selects the CRC0 Register</td></tr><tr><td>0xAA</td><td>CRC1</td><td>Selects the CRC1 Register</td></tr><tr><td>0xAB</td><td>CRC2</td><td>Selects the CRC2 Register</td></tr><tr><td>0xAC</td><td>CRC3</td><td>Selects the CRC3 Register</td></tr></table> Read: C2 Status Returns status information on the current programming operation. When the MSB (bit 7) is set to 1, a read or write operation is in progress. All other bits can be ignored by the programming tools.	Address	Name	Description	0x00	DEVICEID	Selects the Device ID Register (read only)	0x01	REVID	Selects the Revision ID Register (read only)	0x02	DEVCTL	Selects the C2 Device Control Register	0xDF	EPCTL	Selects the C2 EPROM Programming Control Register	0xBF	EPDAT	Selects the C2 EPROM Data Register	0xB7	EPSTAT	Selects the C2 EPROM Status Register	0xAF	EPADDRH	Selects the C2 EPROM Address High Byte Register	0xAE	EPADDRL	Selects the C2 EPROM Address Low Byte Register	0xA9	CRC0	Selects the CRC0 Register	0xAA	CRC1	Selects the CRC1 Register	0xAB	CRC2	Selects the CRC2 Register	0xAC	CRC3	Selects the CRC3 Register
Address	Name	Description																																							
0x00	DEVICEID	Selects the Device ID Register (read only)																																							
0x01	REVID	Selects the Revision ID Register (read only)																																							
0x02	DEVCTL	Selects the C2 Device Control Register																																							
0xDF	EPCTL	Selects the C2 EPROM Programming Control Register																																							
0xBF	EPDAT	Selects the C2 EPROM Data Register																																							
0xB7	EPSTAT	Selects the C2 EPROM Status Register																																							
0xAF	EPADDRH	Selects the C2 EPROM Address High Byte Register																																							
0xAE	EPADDRL	Selects the C2 EPROM Address Low Byte Register																																							
0xA9	CRC0	Selects the CRC0 Register																																							
0xAA	CRC1	Selects the CRC1 Register																																							
0xAB	CRC2	Selects the CRC2 Register																																							
0xAC	CRC3	Selects the CRC3 Register																																							

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C2 Register Definition 30.8. EPADDRH: C2 EPROM Address High Byte

Bit	7	6	5	4	3	2	1	0
Name	EPADDR[15:8]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0xAF

Bit	Name	Function
7:0	EPADDR[15:8]	C2 EPROM Address High Byte. This register is used to set the EPROM address location during C2 EPROM operations.

C2 Register Definition 30.9. EPADDRL: C2 EPROM Address Low Byte

Bit	7	6	5	4	3	2	1	0
Name	EPADDR[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0xAE

Bit	Name	Function
7:0	EPADDR[15:8]	C2 EPROM Address Low Byte. This register is used to set the EPROM address location during C2 EPROM operations.