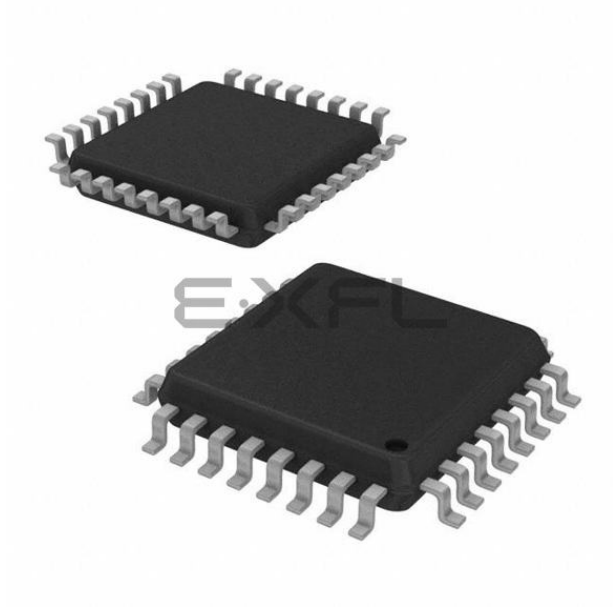

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	48 MIPS
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051t322-gq

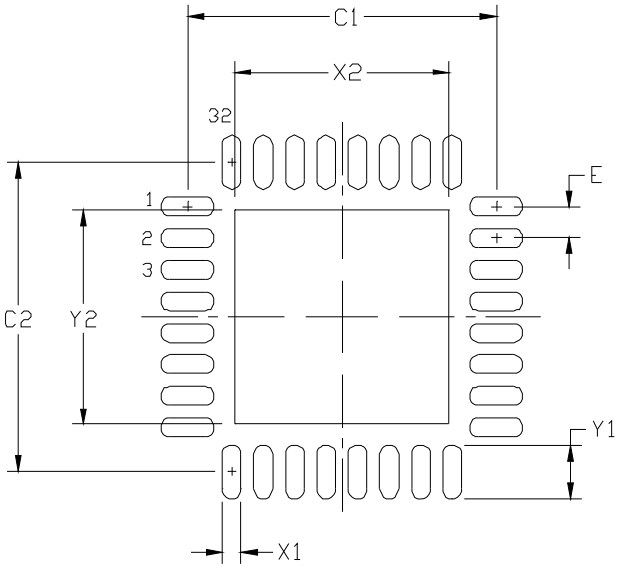


Figure 5.2. QFN-32 Recommended PCB Land Pattern

Table 5.2. QFN-32 PCB Land Pattern Dimensions

Dimension	Min	Max	Dimension	Min	Max
C1	4.80	4.90	X2	3.20	3.40
C2	4.80	4.90	Y1	0.75	0.85
E	0.50 BSC		Y2	3.20	3.40
X1	0.20	0.30			

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
7. A 3x3 array of 1.0 mm openings on a 1.2 mm pitch should be used for the center pad to assure the proper paste volume.

Card Assembly

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Table 7.10. ADC0 Electrical Characteristics

V_{DD} = 3.0 V, VREF = 2.40 V (REFSL=0), PGA Gain = 1, –40 to +85 °C unless otherwise specified.

Parameters	Test Condition	Min	Typ	Max	Unit
DC Accuracy					
Resolution			10		bits
Integral Nonlinearity		—	±0.5	±1	LSB
Differential Nonlinearity	Guaranteed Monotonic	—	±0.5	±1	LSB
Offset Error		–2	0	+2	LSB
Full Scale Error		–2	0	+2	LSB
Offset Temperature Coefficient		—	45	—	ppm/°C
Dynamic performance (10 kHz sine-wave single-ended input, 1 dB below Full Scale, 500 ksps)					
Signal-to-Noise Plus Distortion		56	60	—	dB
Total Harmonic Distortion	Up to the 5th harmonic	—	70	—	dB
Spurious-Free Dynamic Range		—	93	—	dB
Conversion Rate					
SAR Conversion Clock		—	—	8.00	MHz
Conversion Time in SAR Clocks	10-bit Mode 8-bit Mode	13 11	— —	— —	clocks clocks
Track/Hold Acquisition Time	VDD ≥ 2.0 V VDD < 2.0 V	300 2.0	— —	— —	ns µs
Throughput Rate		—	—	500	ksps
Analog Inputs					
ADC Input Voltage Range	Single Ended (AIN+ – GND)	0	—	VREF	V
Absolute Pin Voltage with respect to GND		0	—	V_{IO}	V
Sampling Capacitance	Gain = 1x (AMP0GN0 = 1) Gain = 0.5x (AMP0GN0 = 0)	— —	5 3	— —	pF pF
Input Multiplexer Impedance		—	5	—	kΩ
Power Specifications					
Power Supply Current (V_{DD} supplied to ADC0)	Operating Mode, 500 ksps C8051T626/7/T320/1/2/3 C8051T626/7	 — —	 600 640	 900 900	 µA µA
Power Supply Rejection		—	–70	—	dB

Note: Represents one standard deviation from the mean.

8.1. Output Code Formatting

The ADC measures the input voltage with reference to GND. The registers ADC0H and ADC0L contain the high and low bytes of the output conversion code from the ADC at the completion of each conversion. Data can be right-justified or left-justified, depending on the setting of the AD0LJST bit. Conversion codes are represented as 10-bit unsigned integers. Inputs are measured from 0 to VREF x 1023/1024. Example codes are shown below for both right-justified and left-justified data. Unused bits in the ADC0H and ADC0L registers are set to 0.

Input Voltage	Right-Justified ADC0H:ADC0L (AD0LJST = 0)	Left-Justified ADC0H:ADC0L (AD0LJST = 1)
VREF x 1023/1024	0x03FF	0xFFC0
VREF x 512/1024	0x0200	0x8000
VREF x 256/1024	0x0100	0x4000
0	0x0000	0x0000

8.2. 8-Bit Mode

Setting the ADC08BE bit in register ADC0CF to 1 will put the ADC in 8-bit mode. In 8-bit mode, only the 8 MSBs of data are converted, and the ADC0H register holds the results. The AD0LJST bit is ignored for 8-bit mode. 8-bit conversions take two fewer SAR clock cycles than 10-bit conversions, so the conversion is completed faster, and a 500 ksps sampling rate can be achieved with a slower SAR clock.

8.3. Modes of Operation

ADC0 has a maximum conversion speed of 500 ksps. The ADC0 conversion clock is a divided version of the system clock, determined by the AD0SC bits in the ADC0CF register.

8.3.1. Starting a Conversion

A conversion can be initiated in one of six ways, depending on the programmed states of the ADC0 Start of Conversion Mode bits (AD0CM2–0) in register ADC0CN. Conversions may be initiated by one of the following:

1. Writing a 1 to the AD0BUSY bit of register ADC0CN
2. A Timer 0 overflow (i.e., timed continuous conversions)
3. A Timer 2 overflow
4. A Timer 1 overflow
5. A rising edge on the CNVSTR input signal
6. A Timer 3 overflow

Writing a 1 to AD0BUSY provides software control of ADC0 whereby conversions are performed "on-demand". During conversion, the AD0BUSY bit is set to logic 1 and reset to logic 0 when the conversion is complete. The falling edge of AD0BUSY triggers an interrupt (when enabled) and sets the ADC0 interrupt flag (AD0INT). Note: When polling for ADC conversion completions, the ADC0 interrupt flag (AD0INT) should be used. Converted data is available in the ADC0 data registers, ADC0H:ADC0L, when bit AD0INT is logic 1. Note that when Timer 2 or Timer 3 overflows are used as the conversion source, Low Byte overflows are used if Timer 2/3 is in 8-bit mode; High byte overflows are used if Timer 2/3 is in 16-bit mode. See Section “28. Timers” on page 246 for timer configuration.

Important Note About Using CNVSTR: The CNVSTR input pin also functions as a Port I/O pin. When the CNVSTR input is used as the ADC0 conversion source, the associated pin should be skipped by the Digital Crossbar. See Section “22. Port Input/Output” on page 138 for details on Port I/O configuration.

8.4.1. Window Detector Example

Figure 8.4 shows two example window comparisons for right-justified data, with ADC0LTH:ADC0LTL = 0x0080 (128d) and ADC0GTH:ADC0GTL = 0x0040 (64d). The input voltage can range from 0 to VREF x (1023/1024) with respect to GND, and is represented by a 10-bit unsigned integer value. In the left example, an AD0WINT interrupt will be generated if the ADC0 conversion word (ADC0H:ADC0L) is within the range defined by ADC0GTH:ADC0GTL and ADC0LTH:ADC0LTL (if 0x0040 < ADC0H:ADC0L < 0x0080). In the right example, and AD0WINT interrupt will be generated if the ADC0 conversion word is outside of the range defined by the ADC0GT and ADC0LT registers (if ADC0H:ADC0L < 0x0040 or ADC0H:ADC0L > 0x0080). Figure 8.5 shows an example using left-justified data with the same comparison values.

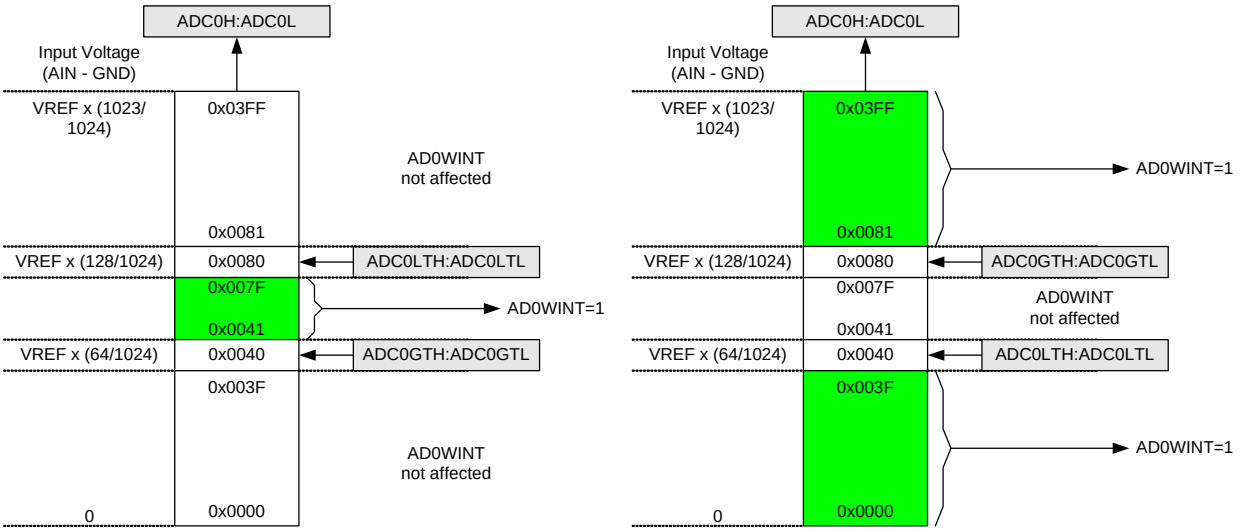


Figure 8.4. ADC Window Compare Example: Right-Justified Data

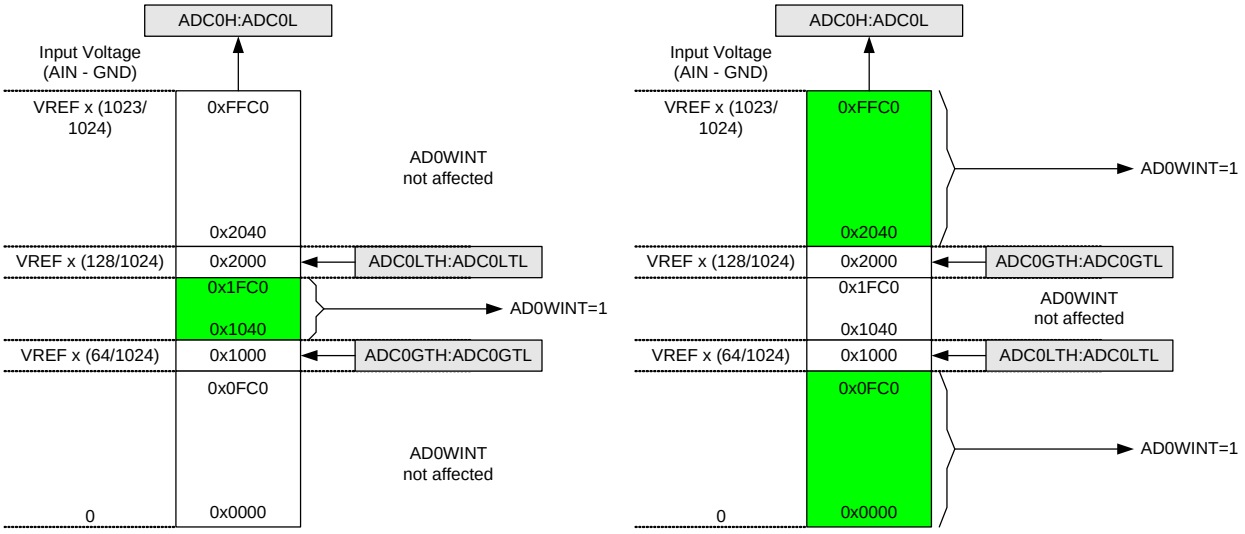


Figure 8.5. ADC Window Compare Example: Left-Justified Data

16. Special Function Registers

The direct-access data memory locations from 0x80 to 0xFF constitute the special function registers (SFRs). The SFRs provide control and data exchange with the C8051T620/1/6/7 & C8051T320/1/2/3's resources and peripherals. The CIP-51 controller core duplicates the SFRs found in a typical 8051 implementation as well as implementing additional SFRs used to configure and access the sub-systems unique to the C8051T620/1/6/7 & C8051T320/1/2/3. This allows the addition of new functionality while retaining compatibility with the MCS-51™ instruction set. Table 16.1 lists the SFRs implemented in the C8051T620/1/6/7 & C8051T320/1/2/3 device family.

The SFR registers are accessed anytime the direct addressing mode is used to access memory locations from 0x80 to 0xFF. SFRs with addresses ending in 0x0 or 0x8 (e.g., P0, TCON, SCON0, IE, etc.) are bit-addressable as well as byte-addressable. All other SFRs are byte-addressable only. Unoccupied addresses in the SFR space are reserved for future use. Accessing these areas will have an indeterminate effect and should be avoided. Refer to the corresponding pages of the data sheet, as indicated in Table 16.2, for a detailed description of each register.

Table 16.1. Special Function Register (SFR) Memory Map

F8	SPI0CN	PCA0L	PCA0H	PCA0CPL0	PCA0CPH0	PCA0CPL4	PCA0CPH4	VDM0CN
F0	B	P0MDIN	P1MDIN	P2MDIN	PCA0PWM	IAPCN	EIP1	EIP2
E8	ADC0CN	PCA0CPL1	PCA0CPH1	PCA0CPL2	PCA0CPH2	PCA0CPL3	PCA0CPH3	RSTSRC
E0	ACC	XBR0	XBR1	XBR2	IT01CF	SMOD1	EIE1	EIE2
D8	PCA0CN	PCA0MD	PCA0CPM0	PCA0CPM1	PCA0CPM2	PCA0CPM3	PCA0CPM4	-
D0	PSW	REF0CN	SCON1	SBUF1	P0SKIP	P1SKIP	P2SKIP	USB0XCN
C8	TMR2CN	REG01CN	TMR2RLL	TMR2RLH	TMR2L	TMR2H	-	SMB0ADM
C0	SMB0CN	SMB0CF	SMB0DAT	ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH	SMB0ADR
B8	IP	CLKMUL	P1MASK	AMX0P	ADC0CF	ADC0L	ADC0H	-
B0	P3	OSCXCN	OSCICN	OSCICL	SBRLL1	SBRLH1	P1MAT	MEMKEY
A8	IE	CLKSEL	EMI0CN	-	SBCON1	-	P0MASK	PFE0CN
A0	P2	SPI0CFG	SPI0CKR	SPI0DAT	P0MDOUT	P1MDOUT	P2MDOUT	P3MDOUT
98	SCON0	SBUF0	CPT1CN	CPT0CN	CPT1MD	CPT0MD	CPT1MX	CPT0MX
90	P1	TMR3CN	TMR3RLL	TMR3RLH	TMR3L	TMR3H	USB0ADR	USB0DAT
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	PSCTL
80	P0	SP	DPL	DPH	P0MAT	EMI0CF	OSCLCN	PCON
	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

Note: SFR Addresses ending in 0x0 or 0x8 are bit-addressable locations and can be used with bitwise instructions.

Table 16.2. Special Function Registers

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
ACC	0xE0	Accumulator	74
ADC0CF	0xBC	ADC0 Configuration	49
ADC0CN	0xE8	ADC0 Control	51
ADC0GTH	0xC4	ADC0 Greater-Than Compare High	52
ADC0GTL	0xC3	ADC0 Greater-Than Compare Low	52
ADC0H	0xBE	ADC0 High	50
ADC0L	0xBD	ADC0 Low	50
ADC0LTH	0xC6	ADC0 Less-Than Compare Word High	53
ADC0LTL	0xC5	ADC0 Less-Than Compare Word Low	53
AMX0P	0xBB	AMUX0 Positive Channel Select	56
B	0xF0	B Register	74
CKCON	0x8E	Clock Control	247
CLKMUL	0xB9	Clock Multiplier Control	132
CLKSEL	0xA9	Clock Select	129
CPT0CN	0x9B	Comparator0 Control	80
CPT0MD	0x9D	Comparator0 Mode Selection	81
CPT0MX	0x9F	Comparator0 MUX Selection	85
CPT1CN	0x9B	Comparator1 Control	82
CPT1MD	0x9D	Comparator1 Mode Selection	83
CPT1MX	0x9F	Comparator1 MUX Selection	86
DPH	0x83	Data Pointer High	73
DPL	0x82	Data Pointer Low	73
EIE1	0xE6	Extended Interrupt Enable 1	106
EIE2	0xE7	Extended Interrupt Enable 2	108
EIP1	0xF6	Extended Interrupt Priority 1	107
EIP2	0xF7	Extended Interrupt Priority 2	109
EMI0CF	0x85	External Memory Configuration	94
EMI0CN	0xAA	External Memory Interface Control	91

18.1.2. EPROM In-Application Programming

The EPROM of the C8051T620/1/6/7 & C8051T320/1/2/3 devices has an In-Application Programming option. In-Application Programming will be much slower than normal programming where the V_{PP} programming voltage is applied to the V_{PP} pin, but it allows a small number of bytes to be programmed anywhere in the non-reserved areas of the EPROM. In order to use this option, V_{IO} must be within a specific range and a capacitor must be connected externally to the V_{PP} pin. Refer to Section "7. Electrical Characteristics" on page 34 for the acceptable range of values for V_{IO} and the capacitor on the V_{PP} pin.

Bytes in the EPROM memory must be written one byte at a time. An EPROM write will be performed after each MOVX write instruction. The recommended procedure for writing to the EPROM is as follows:

1. **Disable interrupts**.
2. **Change the core clock to 25 MHz or less.**
3. Enable the VDD Monitor. **Write 0x80 to VDM0CN.**
4. Enable the VDD Monitor as a reset source. **Write 0x02 to RSTSRC.**
5. Disable the Prefetch engine. **Write 0x00 to the PFE0CN register.**
6. **Set the VPP Pin to an open-drain configuration, with a '1' in the port latch.**
7. **Set the PSWE bit (register PSCTL).**
8. **Write the first key code to MEMKEY: 0xA5**.
9. **Write the second key code to MEMKEY: 0xF1**.
10. Enable in-application programming. **Write 0x80 to the IAPCN register.**
11. Using a MOVX write instruction, **write a single data byte to the desired location.**
12. Disable in-application EPROM programming. **Write 0x00 to the IAPCN register.**
13. **Clear the PSWE bit**.
14. Re-enable the Prefetch engine. **Write 0x20 to the PFE0CN register.**
15. **Delay for at least 1 us.**
16. Disable the programming hardware. **Write 0x40 to the IAPCN register.**
17. **Restore the core clock** (if changed in Step 2)
18. **Re-enable interrupts**.

Steps 8–11 must be repeated for each byte to be written.

When an application uses the In-Application Programming feature, the V_{PP} pin must be set to open-drain mode, with a '1' in the port latch. The pin can still be used a as a general-purpose I/O pin if the programming circuitry of the pin is disabled after all writes are completed by using the IAPHWD bit in the IAPCN register (IAPCN.6). It is not necessary to disable the programming hardware if the In-Application Programming feature has not been used.

Important Note: Software should delay for at least 1 µs after the last EPROM write before setting the IAPHWD bit.

6. Make certain that all writes to the RSTSRC register explicitly set the PORSF bit to a 1. Areas to check are initialization code which enables other reset sources, such as the Missing Clock Detector, for example, and instructions which force a Software Reset. A global search on "RSTSRC" can quickly verify this.

18.3.2. PSWE Maintenance

7. Reduce the number of places in code where the PSWE bit (PSCTL.0) is set to a 1. There should be exactly one routine in code that sets PSWE to a 1 to write EPROM bytes.
8. Minimize the number of variable accesses while PSWE is set to a 1. Handle pointer address updates and loop variable maintenance outside the "PSWE = 1;... PSWE = 0;" area.
9. Disable interrupts prior to setting PSWE to a '1' and leave them disabled until after PSWE has been reset to '0'. Any interrupts posted during the EPROM write operation will be serviced in priority order after the EPROM operation has been completed and interrupts have been re-enabled by software.
10. Make certain that the EPROM write pointer variables are not located in XRAM. See your compiler documentation for instructions regarding how to explicitly locate variables in different memory areas.
11. Add address bounds checking to the routines that write EPROM memory to ensure that a routine called with an illegal address does not result in modification of the EPROM.

18.3.3. System Clock

12. If operating from an external crystal, be advised that crystal performance is susceptible to electrical interference and is sensitive to layout and to changes in temperature. If the system is operating in an electrically noisy environment, use the internal oscillator or an external CMOS clock.
13. If operating from the external oscillator, switch to the internal oscillator during EPROM write operations. The external oscillator can continue to run, and the CPU can switch back to the external oscillator after the EPROM operation has completed.

18.4. Program Memory CRC

A CRC engine is included on-chip which provides a means of verifying EPROM contents once the device has been programmed. The CRC engine is available for EPROM verification even if the device is fully read and write locked, allowing for verification of code contents at any time.

The CRC engine is operated through the C2 debug and programming interface, and performs 16-bit CRCs on individual 256-Byte blocks of program memory, or a 32-bit CRC on the entire memory space. To prevent hacking and extrapolation of security-locked source code, the CRC engine will only allow CRCs to be performed on contiguous 256-Byte blocks beginning on 256-Byte boundaries (lowest 8-bits of address are 0x00). For example, the CRC engine can perform a CRC for locations 0x0400 through 0x04FF, but it cannot perform a CRC for locations 0x0401 through 0x0500, or on block sizes smaller or larger than 256 Bytes.

18.4.1. Performing 32-bit CRCs on Full EPROM Content

A 32-bit CRC on the entire EPROM space is initiated by writing to the CRC1 byte over the C2 interface. The CRC calculation begins at address 0x0000, and ends at the end of user EPROM space. The EPBusy bit in register C2ADD will be set during the CRC operation, and cleared once the operation is complete. The 32-bit results will be available in the CRC3-0 registers. CRC3 is the MSB, and CRC0 is the LSB. The polynomial used for the 32-bit CRC calculation is 0x04C11DB7. Note: If a 16-bit CRC has been performed since the last device reset, a device reset should be initiated before performing a 32-bit CRC operation.

18.4.2. Performing 16-bit CRCs on 256-Byte EPROM Blocks

A 16-bit CRC of individual 256-byte blocks of EPROM can be initiated by writing to the CRC0 byte over the C2 interface. The value written to CRC0 is the high byte of the beginning address for the CRC. For example, if CRC0 is written to 0x02, the CRC will be performed on the 256-bytes beginning at address 0x0200, and ending at address 0x2FF. The EPBusy bit in register C2ADD will be set during the CRC operation, and cleared once the operation is complete. The 16-bit results will be available in the CRC1-0 registers. CRC1 is the MSB, and CRC0 is the LSB. The polynomial for the 16-bit CRC calculation is 0x1021.

21. Oscillators and Clock Selection

C8051T620/1/6/7 & C8051T320/1/2/3 devices include a programmable internal high-frequency oscillator, a programmable internal low-frequency oscillator, and an external oscillator drive circuit. The internal high-frequency oscillator can be enabled/disabled and calibrated using the OSCICN and OSCICL registers, as shown in Figure 21.1. The internal low-frequency oscillator can be enabled/disabled and calibrated using the OSCLCN register. The system clock can be sourced by the external oscillator circuit or either internal oscillator. Both internal oscillators offer a selectable post-scaling feature. The USB clock (USBCLK) can be derived from the internal oscillators or external oscillator.

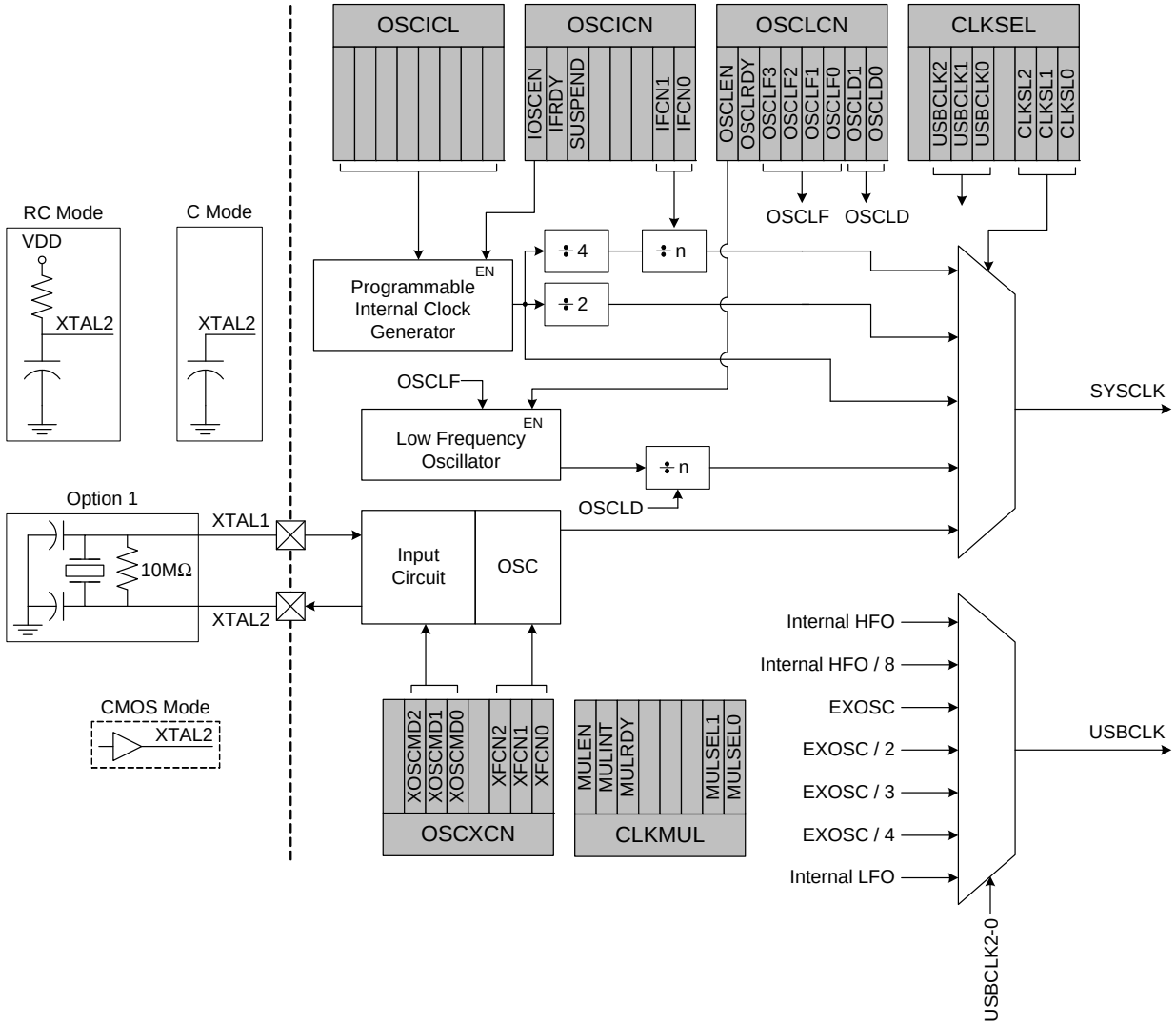


Figure 21.1. Oscillator Options

21.1. System Clock Selection

The CLKSL[2:0] bits in register CLKSEL select which oscillator source is used as the system clock. CLKSL[2:0] must be set to 001b for the system clock to run from the external oscillator; however the external oscillator may still clock certain peripherals (timers, PCA) when the internal oscillator is selected as the system clock. The system clock may be switched on-the-fly between the internal oscillators and external oscillator so long as the selected clock source is enabled and running.

The internal high-frequency and low-frequency oscillators require little start-up time and may be selected as the system clock immediately following the register write which enables the oscillator. The external RC and C modes also typically require no startup time.

21.2. USB Clock Selection

The USBCLK[2:0] bits in register CLKSEL select which oscillator source is used as the USB clock. The USB clock may be derived from the internal oscillators, a divided version of the internal High-Frequency oscillator, or a divided version of the external oscillator. Note that the USB clock must be 48 MHz when operating USB0 as a Full Speed Function; the USB clock must be 6 MHz when operating USB0 as a Low Speed Function. See SFR Definition 21.1 for USB clock selection options.

Some example USB clock configurations for Full and Low Speed mode are given below:

USB Full Speed (48 MHz)		
Internal Oscillator		
Clock Signal	**Input Source Selection**	**Register Bit Settings**
USB Clock	Internal Oscillator*	USBCLK = 000b
Internal Oscillator	Divide by 1	IFCN = 11b
External Oscillator		
Clock Signal	**Input Source Selection**	**Register Bit Settings**
USB Clock	External Oscillator	USBCLK = 010b
External Oscillator	CMOS Oscillator Mode 48 MHz Oscillator	XOSCMD = 010b

Note: Clock Recovery must be enabled for this configuration.

USB Low Speed (6 MHz)		
Internal Oscillator		
Clock Signal	**Input Source Selection**	**Register Bit Settings**
USB Clock	Internal Oscillator / 8	USBCLK = 001b
Internal Oscillator	Divide by 1	IFCN = 11b
External Oscillator		
Clock Signal	**Input Source Selection**	**Register Bit Settings**
USB Clock	External Oscillator / 4	USBCLK = 101b
External Oscillator	CMOS Oscillator Mode 24 MHz Oscillator	XOSCMD = 010b
	Crystal Oscillator Mode 24 MHz Oscillator	XOSCMD = 110b XFCN = 111b

21.5. Programmable Internal Low-Frequency (L-F) Oscillator

All C8051T620/1/6/7 & C8051T320/1/2/3 devices include a programmable low-frequency internal oscillator, which is calibrated to a nominal frequency of 80 kHz. The low-frequency oscillator circuit includes a divider that can be changed to divide the clock by 1, 2, 4, or 8, using the OSCLD bits in the OSCLCN register (see SFR Definition 21.5). Additionally, the OSCLF[3:0] bits can be used to adjust the oscillator's output frequency.

21.5.1. Calibrating the Internal L-F Oscillator

Timers 2 and 3 include capture functions that can be used to capture the oscillator frequency, when running from a known time base. When either Timer 2 or Timer 3 is configured for L-F Oscillator Capture Mode, a falling edge (Timer 2) or rising edge (Timer 3) of the low-frequency oscillator's output will cause a capture event on the corresponding timer. As a capture event occurs, the current timer value (TMRnH:TMRnL) is copied into the timer reload registers (TMRnRLH:TMRnRLL). By recording the difference between two successive timer capture values, the low-frequency oscillator's period can be calculated. The OSCLF bits can then be adjusted to produce the desired oscillator frequency.

SFR Definition 21.5. OSCLCN: Internal L-F Oscillator Control

Bit	7	6	5	4	3	2	1	0
Name	OSCLEN	OSCLRDY	OSCLF[3:0]				OSCLD[1:0]	
Type	R/W	R	R.W				R/W	
Reset	0	0	Varies	Varies	Varies	Varies	0	0

SFR Address = 0x86

Bit	Name	Function
7	OSCLEN	**Internal L-F Oscillator Enable.** 0: Internal L-F Oscillator Disabled. 1: Internal L-F Oscillator Enabled.
6	OSCLRDY	**Internal L-F Oscillator Ready.** 0: Internal L-F Oscillator frequency not stabilized. 1: Internal L-F Oscillator frequency stabilized. **Note:** OSCLRDY is only set back to 0 in the event of a device reset or a change to the OSCLD[1:0] bits.
5:2	OSCLF[3:0]	**Internal L-F Oscillator Frequency Control Bits.** Fine-tune control bits for the Internal L-F oscillator frequency. When set to 0000b, the L-F oscillator operates at its fastest setting. When set to 1111b, the L-F oscillator operates at its slowest setting.
1:0	OSCLD[1:0]	**Internal L-F Oscillator Divider Select.** 00: Divide by 8 selected. 01: Divide by 4 selected. 10: Divide by 2 selected. 11: Divide by 1 selected.

22.1. Port I/O Modes of Operation

Port pins use the Port I/O cell shown in Figure 22.2. Each Port I/O cell can be configured by software for analog I/O or digital I/O using the PnMDIN registers. On reset, all Port I/O cells default to a high impedance state with weak pull-ups enabled until the Crossbar is enabled (XBARE = 1).

22.1.1. Port Pins Configured for Analog I/O

Any pins to be used as Comparator or ADC input, external oscillator input/output, or VREF should be configured for analog I/O (PnMDIN.n = 1). When a pin is configured for analog I/O, its weak pullup, digital driver, and digital receiver are disabled. Port pins configured for analog I/O will always read back a value of 0.

Configuring pins as analog I/O saves power and isolates the Port pin from digital interference. Port pins configured as digital inputs may still be used by analog peripherals; however, this practice is not recommended and may result in measurement errors.

22.1.2. Port Pins Configured For Digital I/O

Any pins to be used by digital peripherals (UART, SPI, SMBus, etc.), external digital event capture functions, or as GPIO should be configured as digital I/O (PnMDIN.n = 1). For digital I/O pins, one of two output modes (push-pull or open-drain) must be selected using the PnMDOUT registers.

Push-pull outputs (PnMDOUT.n = 1) drive the Port pad to the V_{IO} or GND supply rails based on the output logic value of the Port pin. Open-drain outputs have the high side driver disabled; therefore, they only drive the Port pad to GND when the output logic value is 0 and become high impedance inputs (both high and low drivers turned off) when the output logic value is 1.

When a digital I/O cell is placed in the high impedance state, a weak pull-up transistor pulls the Port pad to the V_{DD} supply voltage to ensure the digital input is at a defined logic state. Weak pull-ups are disabled when the I/O cell is driven to GND to minimize power consumption and may be globally disabled by setting WEAKPUD to 1. The user should ensure that digital I/O are always internally or externally pulled or driven to a valid logic state to minimize power consumption. Port pins configured for digital I/O always read back the logic state of the Port pad, regardless of the output logic value of the Port pin.

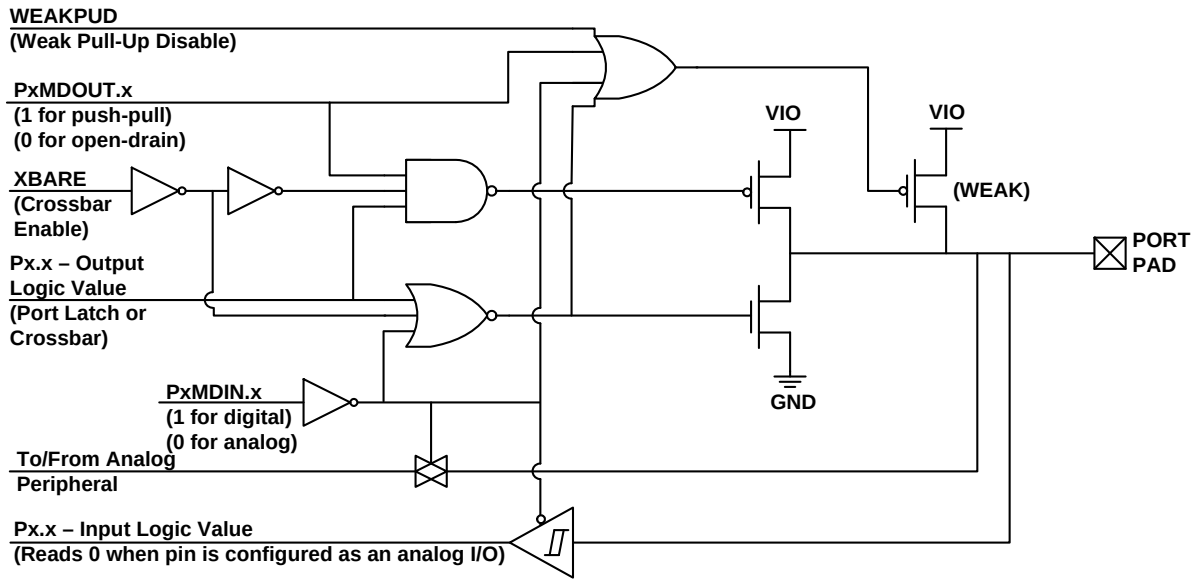
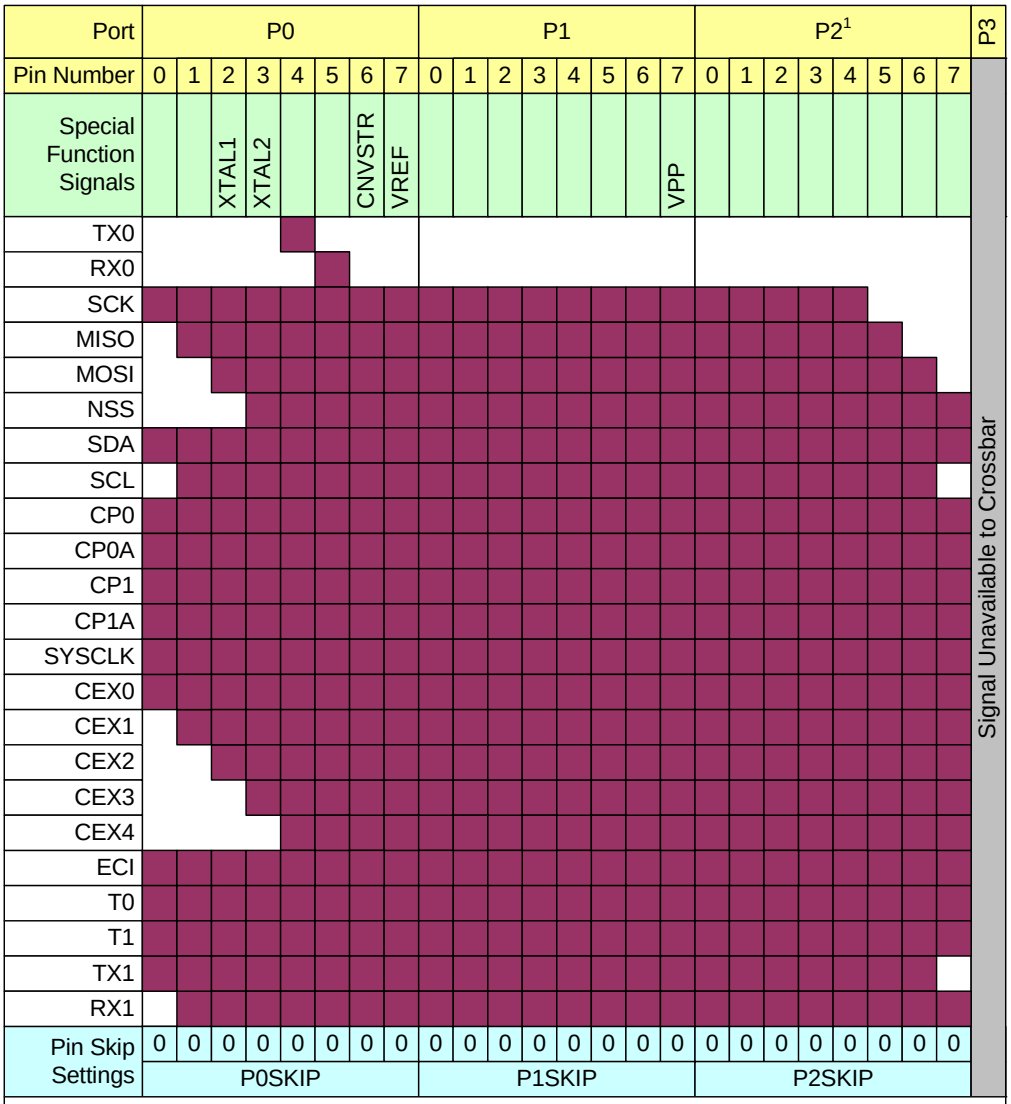


Figure 22.2. Port I/O Cell Block Diagram



Pins P0.0-P2.7[1] are capable of being assigned to crossbar peripherals.

The crossbar peripherals are assigned in priority order from top to bottom, according to this diagram.

■ These boxes represent Port pins which can potentially be assigned to a peripheral.

□ Special Function Signals are not assigned by the crossbar. When these signals are enabled, the Crossbar should be manually configured to skip the corresponding port pins.

□ Pins can be “skipped” by setting the corresponding bit in PnSKIP to ‘1’.

Notes:
1. P2.4-P2.7 are only available in certain packages.
2. NSS is only pinned out when the SPI is in 4-wire mode.

Figure 22.3. Priority Crossbar Decoder Potential Pin Assignments

USB Register Definition 23.19. EENABLE: USB0 Endpoint Enable

Bit	7	6	5	4	3	2	1	0
Name					EEN3	EEN2	EEN1	Reserved
Type	R	R	R	R	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

USB Register Address = 0x1E

Bit	Name	Function
7:4	Unused	Read = 1111b. Write = don't care.
3	EEN3	**Endpoint 3 Enable.** This bit enables/disables Endpoint 3. 0: Endpoint 3 is disabled (no NACK, ACK, or STALL on the USB network). 1: Endpoint 3 is enabled (normal).
2	EEN2	**Endpoint 2 Enable.** This bit enables/disables Endpoint 2. 0: Endpoint 2 is disabled (no NACK, ACK, or STALL on the USB network). 1: Endpoint 2 is enabled (normal).
1	EEN1	**Endpoint 1 Enable.** This bit enables/disables Endpoint 1. 0: Endpoint 1 is disabled (no NACK, ACK, or STALL on the USB network). 1: Endpoint 1 is enabled (normal).
0	Reserved	Read = 1b. Must Write 1b.

23.12. Controlling Endpoints1-3 IN

Endpoints1-3 IN are managed via USB registers EINCSRL and EINCSRH. All IN endpoints can be used for Interrupt, Bulk, or Isochronous transfers. Isochronous (ISO) mode is enabled by writing 1 to the ISO bit in register EINCSRH. Bulk and Interrupt transfers are handled identically by hardware.

An Endpoint1-3 IN interrupt is generated by any of the following conditions:

1. An IN packet is successfully transferred to the host.
2. Software writes 1 to the FLUSH bit (EINCSRL.3) when the target FIFO is not empty.
3. Hardware generates a STALL condition.

23.12.1. Endpoints1-3 IN Interrupt or Bulk Mode

When the ISO bit (EINCSRH.6) = 0 the target endpoint operates in Bulk or Interrupt Mode. Once an endpoint has been configured to operate in Bulk/Interrupt IN mode (typically following an Endpoint0 SET_INTERFACE command), firmware should load an IN packet into the endpoint IN FIFO and set the INPRDY bit (EINCSRL.0). Upon reception of an IN token, hardware will transmit the data, clear the INPRDY bit, and generate an interrupt.

Writing 1 to INPRDY without writing any data to the endpoint FIFO will cause a zero-length packet to be transmitted upon reception of the next IN token.

A Bulk or Interrupt pipe can be shut down (or Halted) by writing 1 to the SDSTL bit (EINCSRL.4). While SDSTL = 1, hardware will respond to all IN requests with a STALL condition. Each time hardware gener-

24. SMBus

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I^2C serial bus. Reads and writes to the interface by the system controller are byte oriented with the SMBus interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/20th of the system clock as a master or slave (this can be faster than allowed by the SMBus specification, depending on the system clock used). A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The SMBus interface may operate as a master and/or slave, and may function on a bus with multiple masters. The SMBus provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and START/STOP control and generation. The SMBus peripheral can be fully driven by software (i.e., software accepts/rejects slave addresses, and generates ACKs), or hardware slave address recognition and automatic ACK generation can be enabled to minimize software overhead. A block diagram of the SMBus peripheral and the associated SFRs is shown in Figure 24.1.

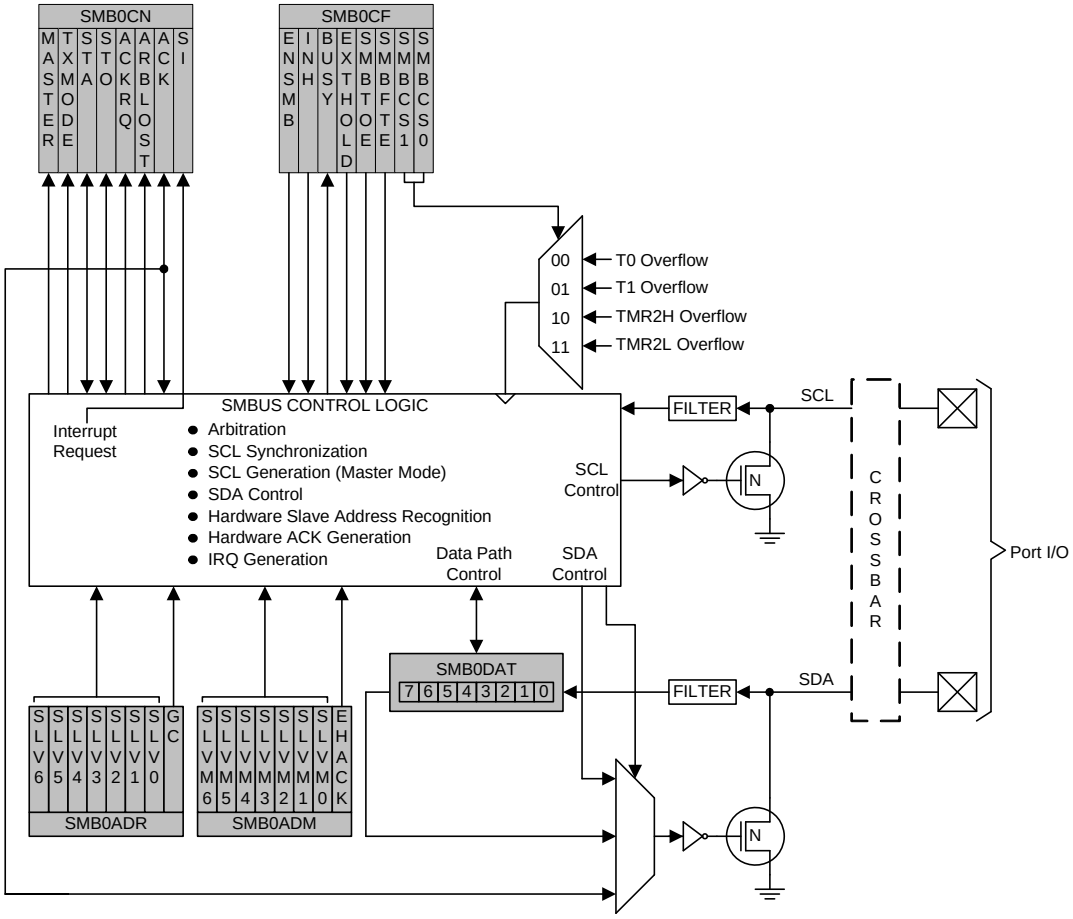


Figure 24.1. SMBus Block Diagram

Table 24.3. Sources for Hardware Changes to SMB0CN

Bit	Set by Hardware When:	Cleared by Hardware When:
MASTER	■ A START is generated.	■ A STOP is generated. ■ Arbitration is lost.
TXMODE	■ START is generated. ■ SMB0DAT is written before the start of an SMBus frame.	■ A START is detected. ■ Arbitration is lost. ■ SMB0DAT is not written before the start of an SMBus frame.
STA	■ A START followed by an address byte is received.	■ Must be cleared by software.
STO	■ A STOP is detected while addressed as a slave. ■ Arbitration is lost due to a detected STOP.	■ A pending STOP is generated.
ACKRQ	■ A byte has been received and an ACK response value is needed (only when hardware ACK is not enabled).	■ After each ACK cycle.
ARBLOST	■ A repeated START is detected as a MASTER when STA is low (unwanted repeated START). ■ SCL is sensed low while attempting to generate a STOP or repeated START condition. ■ SDA is sensed low while transmitting a 1 (excluding ACK bits).	■ Each time SI is cleared.
ACK	■ The incoming ACK value is low (ACKNOWLEDGE).	■ The incoming ACK value is high (NOT ACKNOWLEDGE).
SI	■ A START has been generated. ■ Lost arbitration. ■ A byte has been transmitted and an ACK/NACK received. ■ A byte has been received. ■ A START or repeated START followed by a slave address + R/W has been received. ■ A STOP has been received.	■ Must be cleared by software.

24.4.3. Hardware Slave Address Recognition

The SMBus hardware has the capability to automatically recognize incoming slave addresses and send an ACK without software intervention. Automatic slave address recognition is enabled by setting the EHACK bit in register SMB0ADM to 1. This will enable both automatic slave address recognition and automatic hardware ACK generation for received bytes (as a master or slave). More detail on automatic hardware ACK generation can be found in Section 24.4.2.2.

The registers used to define which address(es) are recognized by the hardware are the SMBus Slave Address register (SFR Definition 24.3) and the SMBus Slave Address Mask register (SFR Definition 24.4). A single address or range of addresses (including the General Call Address 0x00) can be specified using these two registers. The most-significant seven bits of the two registers are used to define which addresses will be ACKed. A 1 in bit positions of the slave address mask SLVM[6:0] enable a comparison between the received slave address and the hardware's slave address SLV[6:0] for those bits. A 0 in a bit of the slave address mask means that bit will be treated as a "don't care" for comparison purposes.

SFR Definition 24.4. SMB0ADM: SMBus Slave Address Mask

Bit	7	6	5	4	3	2	1	0
Name	SLVM[6:0]							EHACK
Type	R/W							R/W
Reset	1	1	1	1	1	1	1	0

SFR Address = 0xCF

Bit	Name	Function
7:1	SLVM[6:0]	**SMBus Slave Address Mask.** Defines which bits of register SMB0ADR are compared with an incoming address byte, and which bits are ignored. Any bit set to 1 in SLVM[6:0] enables comparisons with the corresponding bit in SLV[6:0]. Bits set to 0 are ignored (can be either 0 or 1 in the incoming address).
0	EHACK	**Hardware Acknowledge Enable.** Enables hardware acknowledgement of slave address and received data bytes. 0: Firmware must manually acknowledge all incoming address and data bytes. 1: Automatic Slave Address Recognition and Hardware Acknowledge is Enabled.

SFR Definition 25.1. SCON0: Serial Port 0 Control

Bit	7	6	5	4	3	2	1	0
Name	S0MODE		MCE0	REN0	TB80	RB80	TI0	RI0
Type	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

SFR Address = 0x98; Bit-Addressable

Bit	Name	Function
7	S0MODE	**Serial Port 0 Operation Mode.** Selects the UART0 Operation Mode. 0: 8-bit UART with Variable Baud Rate. 1: 9-bit UART with Variable Baud Rate.
6	Unused	Read = 1b, Write = Don't Care.
5	MCE0	**Multiprocessor Communication Enable.** The function of this bit is dependent on the Serial Port 0 Operation Mode: **Mode 0: Checks for valid stop bit.** 0: Logic level of stop bit is ignored. 1: RI0 will only be activated if stop bit is logic level 1. **Mode 1: Multiprocessor Communications Enable.** 0: Logic level of ninth bit is ignored. 1: RI0 is set and an interrupt is generated only when the ninth bit is logic 1.
4	REN0	**Receive Enable.** 0: UART0 reception disabled. 1: UART0 reception enabled.
3	TB80	**Ninth Transmission Bit.** The logic level of this bit will be sent as the ninth transmission bit in 9-bit UART Mode (Mode 1). Unused in 8-bit mode (Mode 0).
2	RB80	**Ninth Receive Bit.** RB80 is assigned the value of the STOP bit in Mode 0; it is assigned the value of the 9th data bit in Mode 1.
1	TI0	**Transmit Interrupt Flag.** Set by hardware when a byte of data has been transmitted by UART0 (after the 8th bit in 8-bit UART Mode, or at the beginning of the STOP bit in 9-bit UART Mode). When the UART0 interrupt is enabled, setting this bit causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software.
0	RI0	**Receive Interrupt Flag.** Set to 1 by hardware when a byte of data has been received by UART0 (set at the STOP bit sampling time). When the UART0 interrupt is enabled, setting this bit to 1 causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software.

SFR Definition 26.6. SBRLL1: UART1 Baud Rate Generator Low Byte

Bit	7	6	5	4	3	2	1	0
Name	SBRLL1[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xB4

Bit	Name	Function
7:0	SBRLL1[7:0]	**UART1 Baud Rate Reload Low Bits.** Low Byte of reload value for UART1 Baud Rate Generator.

Table 29.2. PCA0CPM and PCA0PWM Bit Settings for PCA Capture/Compare Modules

Operational Mode	PCA0CPMn								PCA0PWM				
Bit Number	7	6	5	4	3	2	1	0	7	6	5	4-2	1-0
Capture triggered by positive edge on CEXn	X	X	1	0	0	0	0	A	0	X	B	XXX	XX
Capture triggered by negative edge on CEXn	X	X	0	1	0	0	0	A	0	X	B	XXX	XX
Capture triggered by any transition on CEXn	X	X	1	1	0	0	0	A	0	X	B	XXX	XX
Software Timer	X	C	0	0	1	0	0	A	0	X	B	XXX	XX
High Speed Output	X	C	0	0	1	1	0	A	0	X	B	XXX	XX
Frequency Output	X	C	0	0	0	1	1	A	0	X	B	XXX	XX
8-Bit Pulse Width Modulator (Note 7)	0	C	0	0	E	0	1	A	0	X	B	XXX	00
9-Bit Pulse Width Modulator (Note 7)	0	C	0	0	E	0	1	A	D	X	B	XXX	01
10-Bit Pulse Width Modulator (Note 7)	0	C	0	0	E	0	1	A	D	X	B	XXX	10
11-Bit Pulse Width Modulator (Note 7)	0	C	0	0	E	0	1	A	D	X	B	XXX	11
16-Bit Pulse Width Modulator	1	C	0	0	E	0	1	A	0	X	B	XXX	XX

1. X = Don't Care (no functional difference for individual module if 1 or 0).
2. A = Enable interrupts for this module (PCA interrupt triggered on CCFn set to 1).
3. B = Enable 8th, 9th, 10th or 11th bit overflow interrupt (Depends on setting of CLSEL[1:0]).
4. C = When set to 0, the digital comparator is off. For high speed and frequency output modes, the associated pin will not toggle. In any of the PWM modes, this generates a 0% duty cycle (output = 0).
5. D = Selects whether the Capture/Compare register (0) or the Auto-Reload register (1) for the associated channel is accessed via addresses PCA0CPHn and PCA0CPLn.
6. E = When set, a match event will cause the CCFn flag for the associated channel to be set.
7. All modules set to 8, 9, 10 or 11-bit PWM mode use the same cycle length setting.

29.3.1. Edge-triggered Capture Mode

In this mode, a valid transition on the CEXn pin causes the PCA to capture the value of the PCA counter/timer and load it into the corresponding module's 16-bit capture/compare register (PCA0CPLn and PCA0CPHn). The CAPPn and CAPNn bits in the PCA0CPMn register are used to select the type of transition that triggers the capture: low-to-high transition (positive edge), high-to-low transition (negative edge), or either transition (positive or negative edge). When a capture occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. If both CAPPn and CAPNn bits are set to logic 1, then the state of the Port pin associated with CEXn can be read directly to determine whether a rising-edge or falling-edge caused the capture.