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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-R5F |
| Core Size | 32-Bit Single-Core |
| Speed | 240MHz |
| Connectivity | CANbus, CSIO, Ethernet, I²C, LINbus, SPI, UART/USART |
| Peripherals | DMA, I²S, LVD, POR, PWM, WDT |
| Number of I/O | 120 |
| Program Memory Size | 2.112MB (2.112M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.15V ~ 5.5V |
| Data Converters | A/D 50x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 208-LQFP Exposed Pad |
| Supplier Device Package | 208-TQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/s6j324cksmse2000a |

**Table 2-3: Function Digit Table**

| Part Number | S6J32X (X = Function Digit) |
|---|---|
| **Function Digit** | **B** |
| CPU Clock Maximum | 160 MHz |
| Graphics Clock Maximum | 160 MHz |
| Display Output Support | ch.0 |
| Video Capture Support | N/A |
| Graphic Engine Type | 2D |
| HyperBus Interface | ch.0, 1 |
| Sound System | YES |
| FPD-Link | N/A |
| Media System | N/A |
| Chip Select Output of MFS | N/A |
| $I^2C$ | MFS ch.16, 17 |

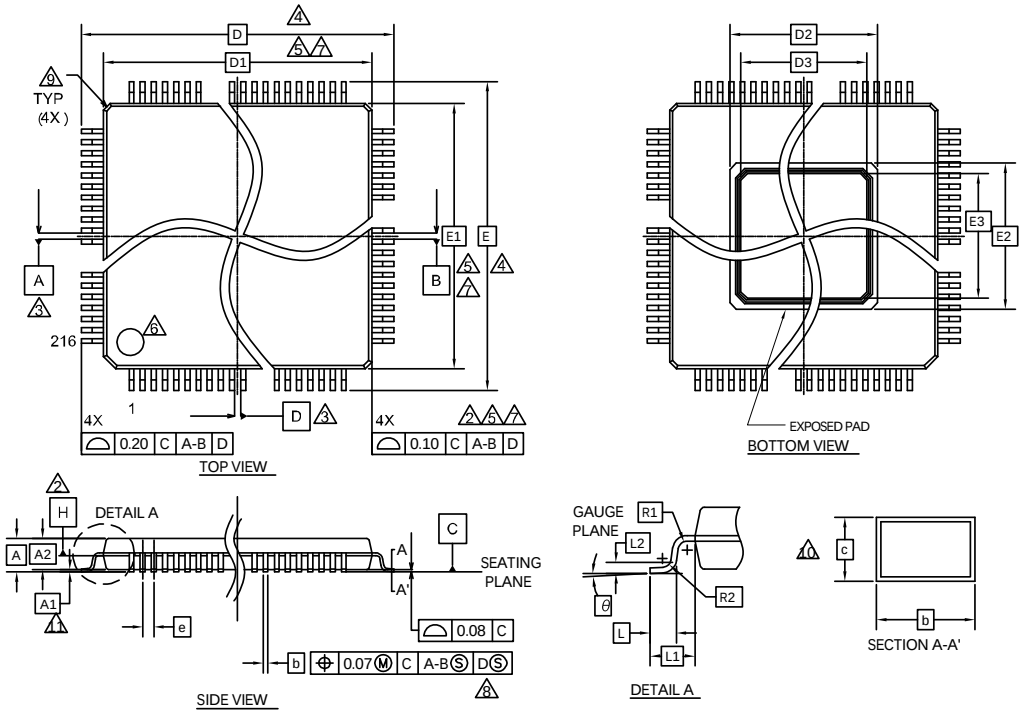
***Notes:***

- *This table only shows the relation between the optional function and the part numbers. That is, all products are not necessarily available for orders. See the order number on the datasheet, and confirm actual availabilities of products.*
- *The sound system is composed of the sound waveform generator, the sound mixer, the audio DAC, PCM-PWM, and I2S0.*
- *The media system means both Ethernet AVB and Media LB.*
- *The CLK_CPU is assigned for CPU clock. The CLK_CD3A0 is assigned for Graphic clock. They are defined at the chapter of Clock Configuration.*
- *Display Output ch.0 is used for RSDS and FPD-LINK (LVDS) as well as DRGB (Digital RGB). The ch.0 of the product which doesn't support FPD-LINK is used for RSDS and DRGB.*
- *HyperBus Interface ch.0 for MCU and ch.1 for graphic subsystem cannot be used simultaneously.*

### 4.2.1 TEQFP216

**Figure** 4-18 **LEQ216**

| Package Type | Package Code |
|---|---|
| TEQFP216 | LEQ216 |



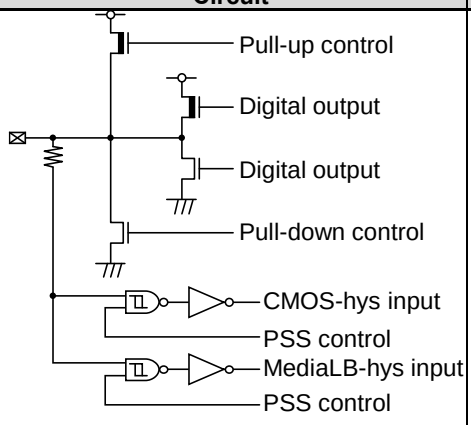
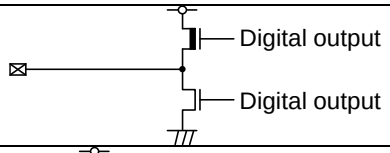
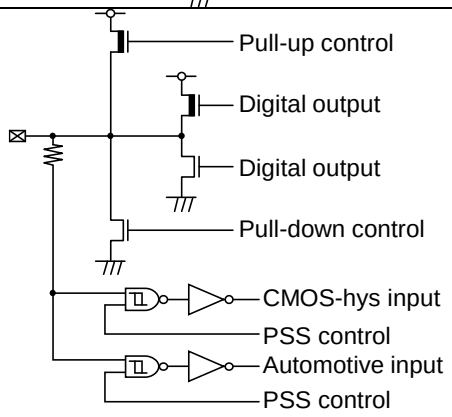
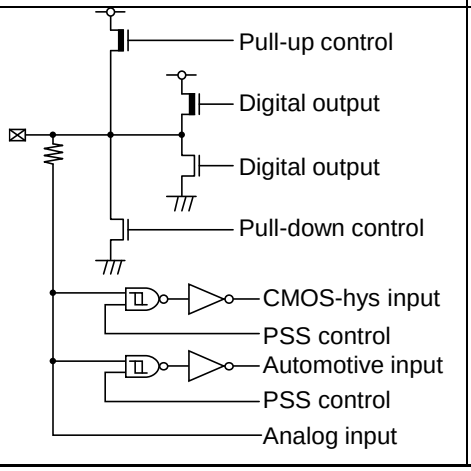

| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | —— | —— | 1.70 |
| A 1 | 0.05 | —— | 0.15 |
| A 2 | 1.35 | 1.40 | 1.45 |
| D | | 26.00 BSC | |
| D 1 | | 24.00 BSC | |
| D 2 | | 9.90 REF | |
| D 3 | | 8.70 REF | |
| E | | 26.00 BSC | |
| E 1 | | 24.00 BSC | |
| E 2 | | 9.90 REF | |
| E 3 | | 8.70 REF | |
| R 1 | 0.08 | —— | —— |
| R 2 | 0.08 | —— | 0.20 |
| θ | 0° | 4° | 8° |
| c | 0.09 | —— | 0.20 |
| b | 0.13 | 0.18 | 0.23 |
| L | 0.45 | 0.60 | 0.75 |
| L 1 | | 1.00 REF | |
| L 2 | | 0.25 | |
| e | | 0.40 BSC | |

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-10860 *B

PACKAGE OUTLINE, 216 LEAD TEQFP
24.0X24.0X1.7 MM LEQ216 REV*B

| Type | Circuit | Remark |
|---|---|---|
| F |  | – General-purpose I/O port<br>– Output 2 mA, 5 mA, 6 mA or 10 mA selectable<br>– 33 kΩ with pull-up resistor control<br>– 33 kΩ with pull-down resistor control<br>– CMOS hysteresis input<br>– MediaLB level hysteresis input |
| G |  | – External 1.2 V regulator control<br>– Output 2 mA |
| H |  | – General-purpose I/O port<br>– Output 1 mA, 2 mA or 5 mA selectable<br>– 50 kΩ with pull-up resistor control<br>– 50 kΩ with pull-down resistor control<br>– CMOS hysteresis input<br>– Automotive hysteresis input |
| I |  | – General-purpose I/O port with analog input<br>– Output 1 mA, 2 mA or 5 mA selectable<br>– 50 kΩ with pull-up resistor control<br>– 50 kΩ with pull-down resistor control<br>– CMOS hysteresis input<br>– Automotive hysteresis input |

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

### *7.1.2 Precautions for Package Mounting*

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress recommended conditions. For detailed information about mount conditions, contact your sales representative.

#### Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

#### Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

#### Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

#### Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

(1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

(2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 ˚C and 30 ˚C. When you open Dry Package that recommends humidity 40% to 70% relative humidity.

(3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

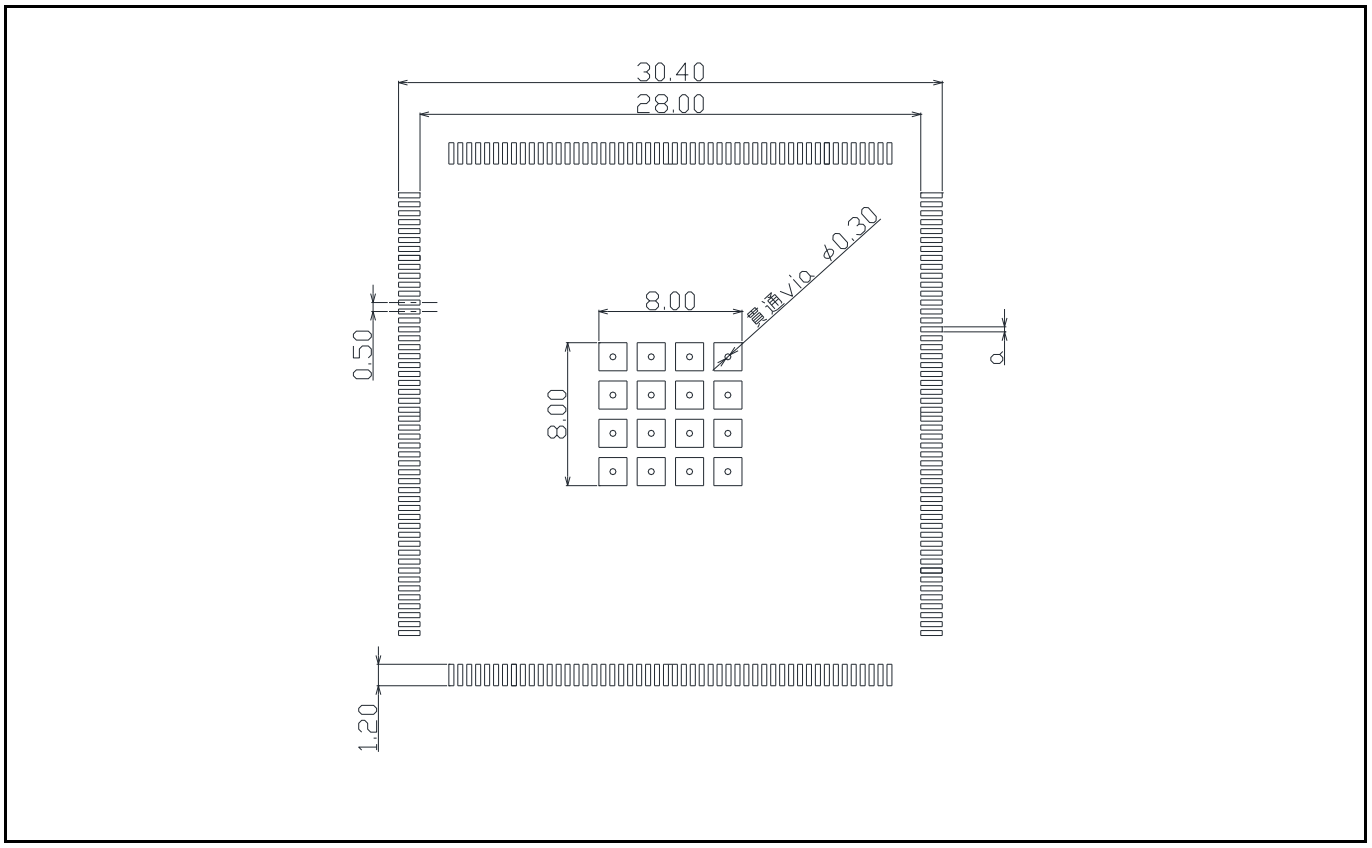
(4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

#### Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125 ˚C/24 h

**Figure 8-4: Land Pattern and Thermal Via LER208**




0.25 mm ≤ a ≤ 0.30 mm

(Condition: See 8.2. Operation Assurance )

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input leakage current | $I_{IL}$ | P2_16, 17, 19, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P4_25 to 31, P5_00 to 20, P6_02 to 31 | $V_{CC}5=V_{CC}53=DV_{CC}=AV_{CC}=5.5$ V $V_{SS} < VI < V_{CC}$ | -5 | - | +5 | µA | 5-V pins 5-V/3-V pins |
| | | P0_00 to 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01 | $V_{CC}3=3.6$ V $V_{SS} < VI < V_{CC3}$ | -10 | - | +10 | µA | 3-V pins |
| Pull-up resistor | $R_{UP1}$ | RSTX, NMIX | - | 25 | 50 | 100 | kΩ | |
| | $R_{UP2}$ | P2_16, 17, 19, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P4_25 to 31, P5_00 to 20, P6_02 to 31 | Pull-up resistor Selected Vcc53 = 4.5 V to 5.5 V | 25 | 50 | 100 | kΩ | 5-V pins 5-V/3-V pins |
| | | P4_25 to 31, P5_00 to 20 | Pull-up resistor Selected Vcc53 = 3.0 V to 3.6 V | 40 | 100 | 200 | kΩ | 5-V/3-V pins |
| | $R_{UP3}$ | P0_00 to 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01 | Pull-up resistor selected | 17 | 33 | 66 | kΩ | 3-V pins |
| | $R_{UP4}$ | JTAG_TDI, JTAG_TMS, JTAG_TCK | - | 25 | 50 | 100 | kΩ | |
| Pull-down resistor | $R_{down1}$ | P2_16, 17, 19, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P4_25 to 31,P5_00 to 20, P6_02 to 31 | Pull-down resistor Selected Vcc53 = 4.5 V to 5.5 V | 25 | 50 | 100 | kΩ | 5-V pins 5-V/3-V pins |
| | | P4_25 to 31,P5_00 to 20 | Pull-down resistor Selected Vcc53 = 3.0 V to 3.6 V | 40 | 100 | 200 | kΩ | 5-V/3-V pins |
| | $R_{down2}$ | P0_00 to 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01 | Pull-down resistor selected | 17 | 33 | 66 | kΩ | 3-V pins |
| | $R_{down3}$ | JTAG_NTRST | - | 25 | 50 | 100 | kΩ | |
| Input capacitance | $C_{IN1}$ | P0_00 to 31, P1_00 to 09, P2_16, 17, 19, 22, 24 to 31, P3_00 to 20, P4_25 to 31, P5_00 to 20, P5_21 22, 27 to 31, P6_00 to 08, 17 to 26 | - | - | 5 | 15 | pF | |
| | $C_{IN2}$ | P3_21 to 31, P4_00 to 12, P6_09 to 16 | - | - | 15 | 45 | pF | When using SMC |

*8.3.2.3 PSS Stop Mode Shutdown*

■This characteristic is specified for the series with the function digits 3, 4, 5, 6, 7, 8, 9, K, L, M, and N.

(Condition: See 8.2. Operation Assurance )

| Symbol | Pin Name | Conditions | Value | | Unit | $T_A$ (°C) | Remark |
|---|---|---|---|---|---|---|---|
| | | | Typ | Max | | | |
| $I_{CCH5}$ | $V_{CC}5$ | PD1=ON, PD4_0=ON, PD4_1=ON | 65 | 270 | µA | 25 | - |
| | | PD1=ON, PD4_0 or PD4_1=ON | 60 | 245 | µA | 25 | - |
| | | PD1=ON | 55 | 220 | µA | 25 | - |

■This characteristic is specified for the series with the function digits B.

(Condition: See 8.2. Operation Assurance )

| Symbol | Pin Name | Conditions | Value | | Unit | $T_A$ (°C) | Remark |
|---|---|---|---|---|---|---|---|
| | | | Typ | Max | | | |
| $I_{CCH5}$ | $V_{CC}5$ | PD1=ON, PD4_0=ON, PD4_1=ON | 65 | 315 | µA | 25 | - |
| | | PD1=ON, PD4_0 or PD4_1=ON | 60 | 290 | µA | 25 | - |
| | | PD1=ON | 55 | 265 | µA | 25 | - |

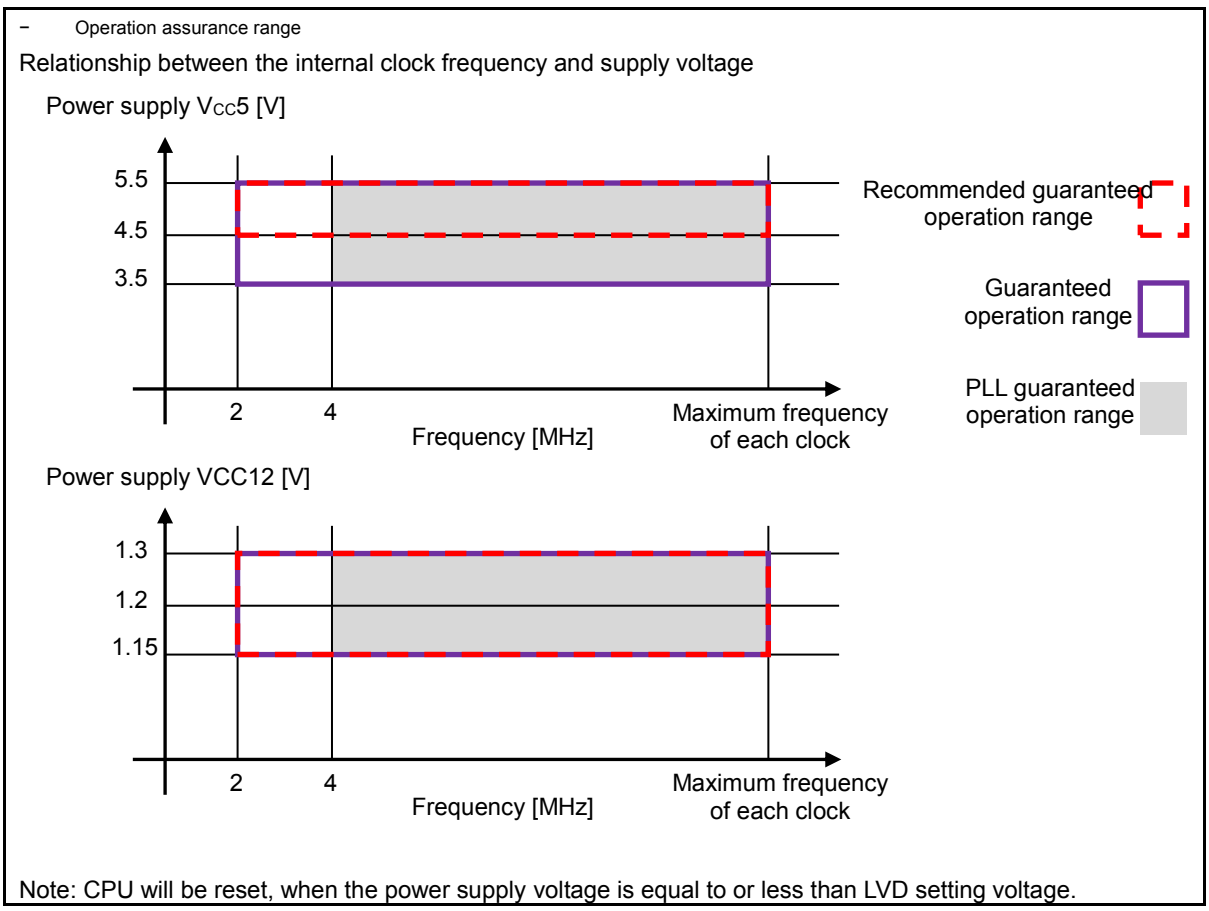
***Notes:***

- *The values will be evaluated after engineering samples release.*
- *The values have been standardized with regulator standby mode (RMSEL=1).*

- *The configurable minimum frequency of PLLn and SSCGn output is 400 MHz.*
- *"Unused" means a clock source which doesn't have any supply destinations. Configure it as disable with performing at the lower clock frequency than the described maximum.*

- Operation assurance range

Relationship between the internal clock frequency and supply voltage




Note: CPU will be reset, when the power supply voltage is equal to or less than LVD setting voltage.

### *8.4.6 Multi-Function Serial*

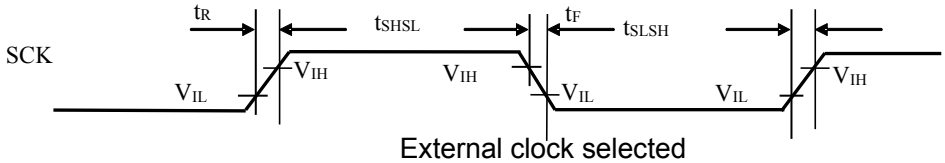
*8.4.6.1 UART (Asynchronous Serial Interface) Timing (SMR: MD2-0=0b000, 0b001)*

#### (1) External Clock Selected (BGR: EXT=1)

(Condition: See 8.2. Operation Assurance )

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCK0 to SCK4, SCK8 to SCK12 | (CL = 50 pF, $I_{OL}$=-2 mA, $I_{OH}$=2 mA), (CL=20 pF, $I_{OL}$=-1 mA, $I_{OH}$=1 mA) | $t_{CLK\_LCPnA}$*1 +10 | - | ns | |
| | | SCK16 to SCK17 | | $t_{CLK\_COMP}$ +10 | - | ns | |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCK0 to SCK4, SCK8 to SCK12 | | $t_{CLK\_LCPnA}$*1 +10 | - | ns | |
| | | SCK16 to SCK17 | | $t_{CLK\_COMP}$ +10 | - | ns | |
| SCK falling time | $t_F$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 | | - | 5 | ns | |
| SCK rising time | $t_R$ | | | - | 5 | ns | |

*1: n=0:ch.0 to ch.4, n=1:ch.8 to ch.12




External clock selected

External clock selected

### (2) Normal Synchronous Transfer (SCR: SPI=0) and Mark Level "L" of Serial Clock Output (SMR: SCINV=1)

(Condition: See 8.2. Operation Assurance )

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK4, SCK8 to SCK12 | Master Mode (CL=20 pF, $I_{OL}$=-5 mA, $I_{OH}$=5 mA) | $3t_{CLK\_LCPnA}$ *1 | - | ns | |
| | | | | $3t_{CLK\_LCPnA}$ *2 | - | | |
| | | SCK16 to SCK17 | | $3t_{CLK\_COMP}$ | - | | |
| SCK ↑ → SOT delay time | $t_{SHOVI}$ | SCK0 to SCK4, SCK8 to SCK12 SOT0 to SOT4, SOT8 to SOT12 | | 0 | 30 | ns | |
| | | | | 0 | 20*3 | | |
| | | SCK16 to SCK17 SOT16 to SOT17 | | 0 | 15 | | |
| Valid SIN → SCK ↓ setup time | $t_{IVSLI}$ | SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12, | | 26.5 | - | ns | |
| | | | | 20*3 | - | | |
| | | SCK16 to SCK17 SIN16 to SIN17 | | 20 | - | | |
| SCK ↓ → Valid SIN hold time | $t_{SLIXI}$ | SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 SOT0 to SOT4, SOT8 to SOT12, SOT16 to SOT17 | | 0 | - | ns | |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCK0 to SCK4, SCK8 to SCK12 | Slave Mode (CL=20 pF, $I_{OL}$=-5 mA, $I_{OH}$=5 mA) | $2t_{CLK\_LCPnA}$ *1 | - | ns | |
| | | | | $2t_{CLK\_LCPnA}$ *2 | - | | |
| | | SCK16 to SCK17 | | $2t_{CLK\_COMP}$ | - | | |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCK0 to SCK4, SCK8 to SCK12 | | $2t_{CLK\_LCPnA}$ *1 | - | ns | |
| | | | | $2t_{CLK\_LCPnA}$ *2 | - | | |
| | | SCK16 to SCK17 | | $2t_{CLK\_COMP}$ | - | | |

### (8) Mark Level "L" of Serial Clock Output (SMR: SCINV=1) and Mark Level "L" of Serial Chip Select (SCSCR: CSLVL=0)

(Condition: See 8.2. Operation Assurance )

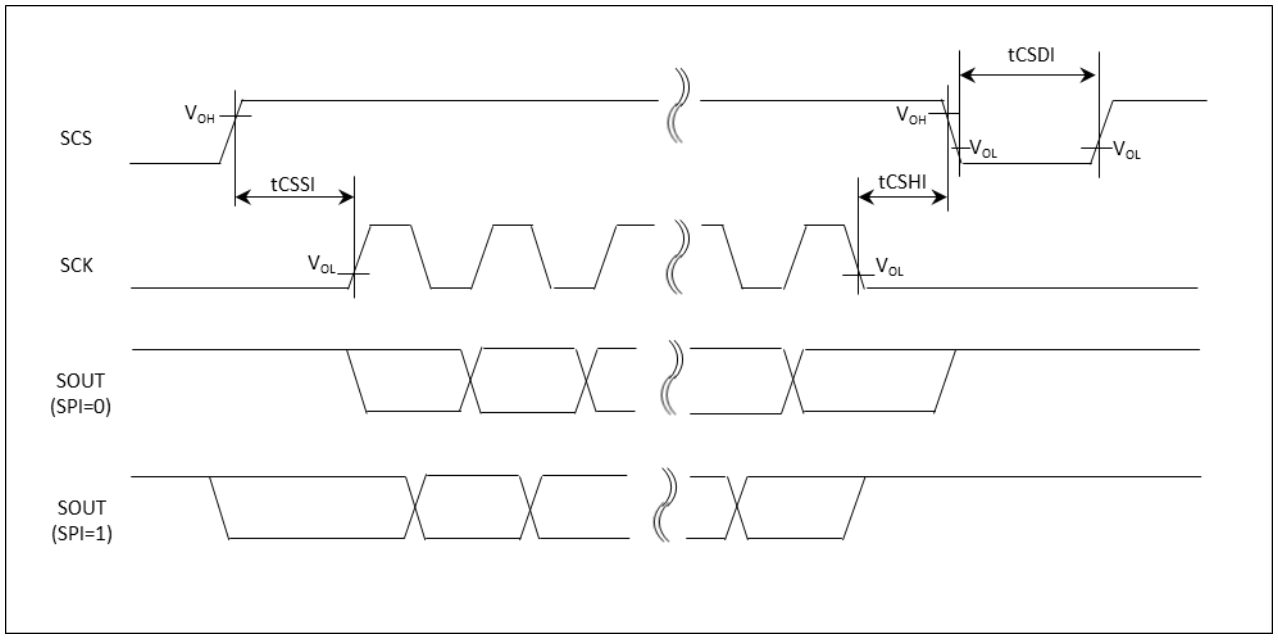
| Parameter | Symbol | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| SCS ↑ →SCK ↑ setup time | $t_{CSSI}$ | Master mode (CL = 20 pF $I_{OL}$=-5 mA, $I_{OH}$=5 mA) | -20*1 | - | ns | |
| SCK ↓ →SCS ↓ hold time | $t_{CSHI}$ | | 0*2 | - | ns | |
| SCS deselect time | $t_{CSDI}$ | | -20+5tcp*3 | - | ns | |
| SCK ↑ →SCS ↑ clock change time | $t_{SCC}$ | Round Function Master mode (CL = 20 pF $I_{OL}$=-5 mA, $I_{OH}$=5 mA) | 3tcp+0 | 3tcp+20 | ns | |

*1) SCSTR1.CSSU=0. $t_{CSSI}$ can be configured.

*2) SCSTR0.CSHD=0. $t_{CSHI}$ can be configured.

*3) SCSTR3/2.CSDS=0. $t_{CSDI}$ can be configured.

tcp is bus clock. Ch0-4 is CLK_LCP0A. Ch8-12 is CLK_LCP1A. Ch16-17 is CLK_COMP.



*8.4.10.5 LVDL2*

(Condition: See 8.2. Operation Assurance )

| Parameter | Pin Name | Conditions | Value | | | Unit | Guaranteed MCU Operation Range | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | | |
| Supply Voltage Range | $V_{CC}12$ | - | 1.1 | - | 1.3 | V | - | - |
| Detection Voltage | $V_{CC}12$ | LVDL2V=00 (Default) | 0.72 | 0.77 | 0.82 | V | No | *1 |
| Release Voltage | $V_{CC}12$ | | 0.795 | 0.845 | 0.895 | V | | |
| Detection Voltage | $V_{CC}12$ | LVDL2V=01 | 0.82 | 0.87 | 0.92 | V | | |
| Release Voltage | $V_{CC}12$ | | 0.895 | 0.945 | 0.995 | V | | |
| Detection Voltage | $V_{CC}12$ | LVDL2V=10 | 0.92 | 0.97 | 1.02 | V | | |
| Release Voltage | $V_{CC}12$ | | 0.995 | 1.045 | 1.095 | V | | |
| Detection Voltage | $V_{CC}12$ | LVDL2V=11 | 1.02 | 1.07 | 1.12 | V | | |
| Release Voltage | $V_{CC}12$ | | 1.095 | 1.145 | 1.195 | V | | |
| Detection Time | - | - | - | - | 30 | µs | - | *2 |

***Notes:***

- **1: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage (1.1 V).*
- **2: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.*

### *8.4.15 DDR-HSSPI*

DDR-HSSPI AC characteristics are specified with the specific reference voltage of VIL, VIH, VOL, VOH = 0.5 Vcc3 as mentioned in Section 8.4.3, regardless of automotive input-level configuration, CMOS Schmitt, and TTL.

#### *8.4.15.1 DDR-HSSPI Interface Timing (SDR Mode)*

(Condition: See 8.2. Operation Assurance )

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| HSSPI clock cycle | $t_{cyc}$ | G_SCLK0<br>M_SCLK0 | (CL = 20 pF, $I_{OL}$=-10 mA, $I_{OH}$=10 mA), | 10 | - | ns | |
| | | | | 20 | - | | when Quad Page Program |
| G_SCLK↑ -> delayed sample clock↑ | $t_{spcnt}$ | - | | 0 | 31.5 | ns | |
| GSDATA -> G_SCLK↑ Input setup time | $t_{isdata}$ | G_SDATA0_0-3<br>G_SDATA1_0-3<br>M_SDATA0_0-3<br>M_SDATA1_0-3 | | *1 | - | ns | |
| G_SCLK↑ -> GSDATA Input hold time | $t_{ihdata}$ | G_SDATA0_0-3<br>G_SDATA1_0-3<br>M_SDATA0_0-3<br>M_SDATA1_0-3 | | *1 | - | ns | |
| G_SCLK↑ -> GSDATA Output delay time | $t_{oddata}$ | G_SDATA0_0-3<br>G_SDATA1_0-3<br>M_SDATA0_0-3<br>M_SDATA1_0-3 | | - | tcyc/2 + 2 | ns | |
| G_SCLK↑ -> GSDATA Output hold time | $t_{ohdata}$ | G_SDATA0_0-3<br>G_SDATA1_0-3<br>M_SDATA0_0-3<br>M_SDATA1_0-3 | | tcyc/2 - 3 | - | ns | |
| GSSEL↓ -> G_SCLK Output delay time | $t_{odsel}$ | G_SSEL0, 1<br>M_SSEL0, 1 | | - 12.00+(SS2CD+0.5)*tcyc | - | ns | |
| G_SCLK↑ -> GSSEL Output hold time | $t_{ohsel}$ | G_SSEL0, 1<br>M_SSEL0, 1 | | tcyc - 2 | - | ns | |

***Notes:***

- *SS2CD [1:0] should be configured as 01, 10, or 11.*
- *For *1, the delay of the delay sample clock can be configured (DLP function).*

*8.4.15.2 DDR-HSSPI Interface Timing (DDR Mode)*

(Condition: See 8.2. Operation Assurance )

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| HSSPI clock cycle | $t_{cyc}$ | G_SCLK0<br>M_SCLK0 | (CL = 20 pF, $I_{OL}$=-10 mA, $I_{OH}$=10 mA), | 12.5 | - | ns | |
| G_SCLK↑↓ -> delayed sample clock↑ | $t_{spcnt}$ | - | | 0 | 31.5 | ns | |
| GSDATA -> G_SCLK↑↓ Input setup time | $t_{isdata}$ | G_SDATA0_0-3<br>G_SDATA1_0-3<br>M_SDATA0_0-3<br>M_SDATA1_0-3 | | *1 | - | ns | |
| G_SCLK↑↓ -> GSDATA Input hold time | $t_{ihdata}$ | G_SDATA0_0-3<br>G_SDATA1_0-3<br>M_SDATA0_0-3<br>M_SDATA1_0-3 | | *1 | - | ns | |
| G_SCLK↑↓ -> GSDATA Output delay time | $t_{oddata}$ | G_SDATA0_0-3<br>G_SDATA1_0-3<br>M_SDATA0_0-3<br>M_SDATA1_0-3 | | - | tcyc/4 + 1.5 | ns | |
| G_SCLK↑↓ -> GSDATA Output hold time | $t_{ohdata}$ | G_SDATA0_0-3<br>G_SDATA1_0-3<br>M_SDATA0_0-3<br>M_SDATA1_0-3 | | Tcyc/4 - 1.0 | - | ns | |
| GSSEL ↓ -> G_SCLK Output delay time | $t_{odsel}$ | G_SSEL0, 1<br>M_SSEL0, 1 | | - 15.75+(SS 2CD+0.5)*t cyc | - | ns | |
| G_SCLK↑ -> GSSEL Output hold time | $t_{ohsel}$ | G_SSEL0, 1<br>M_SSEL0, 1 | | 0.75*tcyc - 2.0 | - | ns | |

***Notes:***

- *SS2CD [1:0] should be configured as 01, 10, or 11.*
- *For *1, the delay of the delay sample clock can be configured (DLP function).*

### *8.4.16 HyperBus*

HyperBus AC characteristics are specified with the specific reference voltage of VIL, VIH, VOL, VOH = 0.5Vcc3 as 8.4.3 regardless of input level configuration automotive, CMOS Schmitt, and TTL.

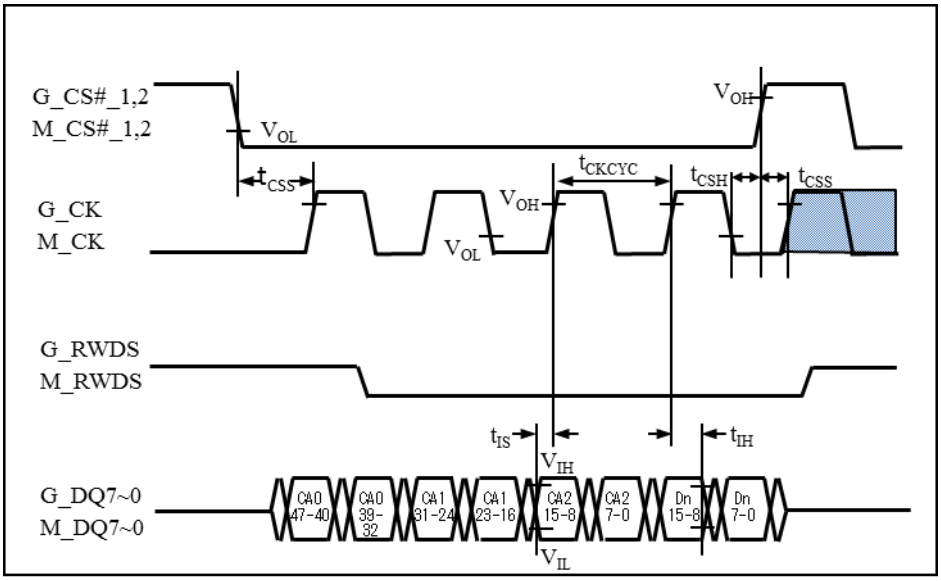
#### *8.4.16.1 HyperBus Write Timing (HyperFlash)*

(Condition: See 8.2. Operation Assurance )

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Hyper Bus clock cycle | $t_{CKCYC}$ | G_CK<br>M_CK | (CL = 20 pF, $I_{OL}$=-10 mA, $I_{OH}$=10 mA), | 12.5 | - | ns | (A) |
| | | | | 10 | - | ns | (B) |
| CS↑↓ -> CK↑<br>Chip Select setup time | $t_{CSS}$ | G_CS#_1,2<br>M_CS#_1,2 | | $t_{CKCYC}$ - 3.25 | - | ns | (A) |
| | | | | $t_{CKCYC}$ -2.0 | - | ns | (B) |
| DQ -> CK↑↓<br>Setup time | $t_{IS}$ | G_DQ7-0<br>M_DQ7-0 | | 1.25 | - | ns | |
| CK↑↓ -> DQ<br>Hold time | $t_{IH}$ | G_DQ7-0<br>M_DQ7-0 | | 1.25 | - | ns | |
| CK↓ -> CS↑<br>Chip select hold time | $t_{CSH}$ | G_CS#_1,2<br>M_CS#_1,2 | | $t_{CKCYC}$/2 | - | ns | |

***Notes:***

- *(A): The value will be targeted by the product series with revision digit A.*
- *(B): The value will be targeted by the product series with after revision digit B.*
- *Hyper Bus clock cycle is always (1/$F_{CLK\_CD1}$)*4.*



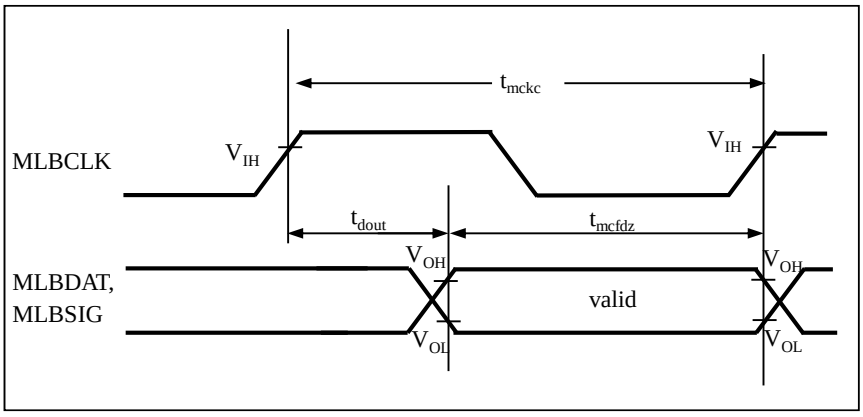
*8.4.18.2 MediaLB Output Timing*

(Condition: See 8.2. Operation Assurance )

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| MLBCLK cycle | $t_{mckc}$ | MLBCLK | (CL = 20 pF, $I_{OL}$=-6 mA, $I_{OH}$=6 mA), | 40 | - | ns | |
| MLBSIG, MLBDAT output stop | $t_{mcfdz}$ | MLBSIG MLBDAT | | 26.5 | - | ns | $t_{mckc}$ - $t_{dout}$ |
| MLBSIG, MLBDAT output delay | $t_{dout}$ | MLBSIG MLBDAT | | 0 | 13.5 | ns | |

***Note:***

- *CLK_HAPP1B0(internal) frequency > MLBCLK(external) frequency*



## 8.6 Audio DAC

### *8.6.1 Electrical Characteristics*

(Condition: See 8.2. Operation Assurance )

| Parameter | Symbol | Pin Name | Conditions *1 | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| system clock frequency | $F_{CLKDA0}$ | - | - | 2.048 | - | 18.432 | MHz | |
| sampling clock | fs | - | - | 8 | - | 48 | kHz | |
| Analog output load resistance *2 | $R_L$ | DAC_L DAC_R | - | 20 | - | - | kΩ | |
| Analog output load capacitance *2 | $C_L$ | | - | - | - | 100 | pF | |
| capacitance | - | C_L C_R | - | 5 | 10 | 20 | µF | |
| Analog output single-end output range (±full scale) | - | DAC_L DAC_R | RL=20 kΩ CL=100 pF | - | 0.673 AVCC3_DAC | - | $V_{P-P}$ | |
| Analog output voltage (zero) | - | | - | - | 0.5 AVCC3_DAC | - | V | |
| THD+N *3 | - | - | signal frequency: 1 kHz LPF(fc: 20 kHz) | - | -82 | -72 | dB | |
| SNR *3 | - | - | signal frequency: 1 kHz LPF(fc: 20 kHz)— − A-weighting filter | 85 | 89 | - | dB | |
| Dynamic range *3 | - | - | | 83 | 86 | - | dB | |
| Out-of-Band Energy | - | - | 20 kHz to 64 fs | - | - | -33 | dB | |
| Channel Separation | - | - | - | - | 80 | - | dB | |
| Output impedance | - | - | - | 150 | 200 | 250 | Ω | |
| PSRR | - | - | digital input: zero — noise 50 Hz | - | -35 | - | dB | |
| | | | digital input: zero — noise 1 kHz | - | -50 | - | dB | |
| | | | digital input: zero — noise 20kHz | - | -40 | - | dB | |
| | | | digital input :full scale sine | - | -13 | - | dB | |
| Supply current normal operation | - | AVCC3_DAC | - | - | 2.2 | 3.2 | mA | |
| Supply current power-down | - | AVCC3_DAC | - | - | - | 100 | µA | |
| Startup Time *4 | - | - | DAE↑ | - | 650 *5 | - | ms | |

***Notes:***

- **1: All parameters specified fs=44.1 kHz, system clock 256 fs and 16-bit data, RL-20 kΩ, $C_L$=100 pF, unless otherwise noted.*
- **2: Refer to bellow note on $R_L$ load connection.*
- **3: These values do not include the noise caused by the analog power supply. (Refer to 7. Use examples)*
- **4: 10µF is connected to C_L, C_R.*
- **5: Startup time (Figure 8-8)*

| Summary | Error Page | Error | Correct Page | Correct | ID |
|---|---|---|---|---|---|
| Case Temperature issue | 64, 65 | Operating temperature<br>TA: -40(min), +105(max) | 80, 81 | Operating temperature<br>TA: -40(min), +105(max)<br>TC: -40(min), +144(max)<br><br>Notes:<br>− Both rating of TA and TC should simultaneously be satisfied as maximum operation temperature.<br>− The following condition should be satisfied in order to facilitate heat dissipation.<br>1. 4 or more layers PCB should be used.<br>2. The area of PCB should be 114.3 mm x 76.2 mm or more, and the thickness should be 1.6 mm or more. (JEDEC standard)<br>3. 1 layer of middle layers at least should be used for dedicated layer to radiate heat with residual copper rate 90% or more. The layer can be used for system ground.<br>4. 35~50% of the die stage area which is exposed at back surface of package should be soldered to a part of 1st layer.<br>5. The part of 1st layer should be connected to the dedicated heat radiation layer with more than 10 thermal via holes. | #283 |
| Main clock frequency | 15 | Main and sub oscillator is available.<br>− A wide range of 3.6 - 4MHz is available for main oscillator | 17 | Main and sub oscillator is available.<br>− A wide range of 3.6 - 16MHz is available for main oscillator | #311 |
| Revision description | 11 | - | 12 | (Inside Figure 2-1: Option and Part Number)<br>C: Support MCAN 3.0.1.<br>D: Support MCAN 3.2. | #313 |
| CPU Clock Maximum | 11 | 200MHz (CPU Clock of function digit A, B, C, and D) | 13 | 160MHz (CPU Clock of function digit A, B, C, and D) | #314 |
| Maximum gap between package and board | 24 | - | 39 | Note:− Same size is specified for MIN, NOM, MAX, then it should be regarded as maximum size. | #315 |

| Summary | Error Page | Error | Correct Page | Correct | ID |
|---|---|---|---|---|---|
| Delete Ethernet restriction for product | 22 | Direct Memory Access Interface, MAC Filtering Block -VLAN tag, IEEE 1588 and IEEE 802.1AS Support, MAC PFC Priority Based Pause Frame Support, and 802.1Qav Support – Credit Based Shaping | 21 | (Delete) | #516 |
| Improvement of description for Pin Assignment | 23 | Alphabets with pin numbers are signs specify I/O circuit type. | 22 | The characters next to the pin number in the pin assignment drawing specify the I/O circuit type.<br>(figure added) | #535 |
| Regarding "red" character in Pin Assignment | 23-38 | The pins which are described in "red" character are not supported, and will be enhanced with next revision products. | 23-35 | The pins which are described in "red" character are not supported product with revision A and C. | #524 |
| Note for Input voltage and Max clamp current | 76 | Maximum clamp current:*A (Remarks)<br>Total maximum clamp current:*A (Remarks) | 75 | Maximum clamp current:*12, *A (Remarks)<br>Total maximum clamp current:*12, *A (Remarks) | #503 |
| TYPO in Absolute Maximum Rating | 76 | Input voltage:VI2:VCC5+0.3(Max)<br>,,,<br>Input voltage:VIE:VCC5+0.3(Max) | 75 | Input voltage:VI2:DVCC+0.3(Max)<br>,,,<br>Input voltage:VIE:VCC53+0.3(Max) | #518 |
| Note for Input voltage and Max clamp current | 78 | - | 77 | *12: VI or VO should never exceed the specified ratings. However, if the maximum current to/from an input is limited by a suitable external resistor, the ICLAMP rating supersedes the VI rating. | #470 |
| Power supply sequence | 80 | Power supply sequence is recommended as VCC5 -> [DVCC or AVCC5 or VCC3 or AVCC3] -> VCC12 -> [AVCC3_LVDS_PLL or VCC3_LVDS_TX] | 79 | Power supply sequence is recommended as VCC5 -> [DVCC or AVCC5 or VCC3 or AVCC3] -> VCC12 -> [AVCC3_LVDS_PLL or VCC3_LVDS_TX].<br>Note that power supplies inside "[]" can be turned on in arbitrary order. | #474 |
| VIH/VIL characteristics for I/O of DVCC | 85, 86 | - | 84, 85 | (Added the "*1" for note of some characteristics and the description) | #439 |
| DS 8.3.1 Port Function Characteristics | 86 | VIL10(Max) 0.3xVcc5 | 85 | VIL10(Max) 0.3xVcc3 | #453 |
| VOH characteristic for I/O of MediaLB | 87 | VOH16:VCC3-0.5(Min) | 86 | VOH16:2.0(Min) | #441 |

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