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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-R5F
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, CSIO, Ethernet, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2.112MB (2.112M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.15V ~ 5.5V
Data Converters	A/D 50x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP Exposed Pad
Supplier Device Package	208-TQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6j328cksmse2000a

Table 2-2: Function Digit Table

Part Number	S6J32X (X = Function Digit)						
Function Digit	**3**	**4**	**5**	**6**	**7**	**8**	**9**
CPU Clock Maximum	240 MHz	240 MHz	240 MHz	240 MHz	240 MHz	240 MHz	240 MHz
Graphics Clock Maximum	200 MHz	200 MHz	200 MHz	200 MHz	200 MHz	200 MHz	200 MHz
Display Output Support	ch.0, 1	ch.0, 1	ch.0, 1	ch.0, 1	ch.0, 1	ch.0, 1	ch.0, 1
Video Capture Support	1 unit	1 unit	1 unit	1 unit	1 unit	1 unit	1 unit
Graphic Engine Type	2D	2D	2D, 3D	2D, 3D	2D	2D, 3D	2D
HyperBus Interface	ch.0, 1	ch.0, 1	ch.0, 1	ch.0, 1	ch.0, 1, 2	ch.0, 1, 2	ch.0, 1, 2
Sound System	N/A	YES	N/A	YES	YES	YES	YES
FPD-Link	N/A	N/A	N/A	YES	N/A	YES	YES
Media System	YES	YES	YES	YES	YES	YES	YES
Chip Select Output of MFS	YES	YES	YES	YES	YES	YES	YES
I^2C	MFS ch.4, 10, 12, 16, 17	MFS ch.4, 10, 12, 16, 17	MFS ch.4, 10, 12, 16, 17	MFS ch.4, 10, 12, 16, 17	MFS ch.4, 10, 12, 16, 17	MFS ch.4, 10, 12, 16, 17	MFS ch.4, 10, 12, 16, 17

Notes:

- *This table only shows the relation between the optional function and the part numbers. That is, all products are not necessarily available for orders. See the order number on the datasheet, and confirm actual availabilities of products.*
- *The sound system is composed of the sound waveform generator, the sound mixer, the audio DAC, PCM-PWM, and I2S0.*
- *The media system means both Ethernet AVB and Media LB.*
- *The CLK_CPU is assigned for CPU clock. The CLK_CD3A0 is assigned for Graphic clock. They are defined at the chapter of Clock Configuration.*
- *Display Output ch.0 is used for RSDS and FPD-LINK (LVDS) as well as DRGB (Digital RGB). The ch.0 of the product which doesn't support FPD-LINK is used for RSDS and DRGB.*
- *Display Output ch.1 is used for FPD-LINK (LVDS) and DRGB (Digital RGB). The ch.1 of the product which doesn't support FPD-LINK is used for DRGB only.*
- *HyperBus Interface ch.0 for MCU and ch.1 for graphic subsystem cannot be used simultaneously.*

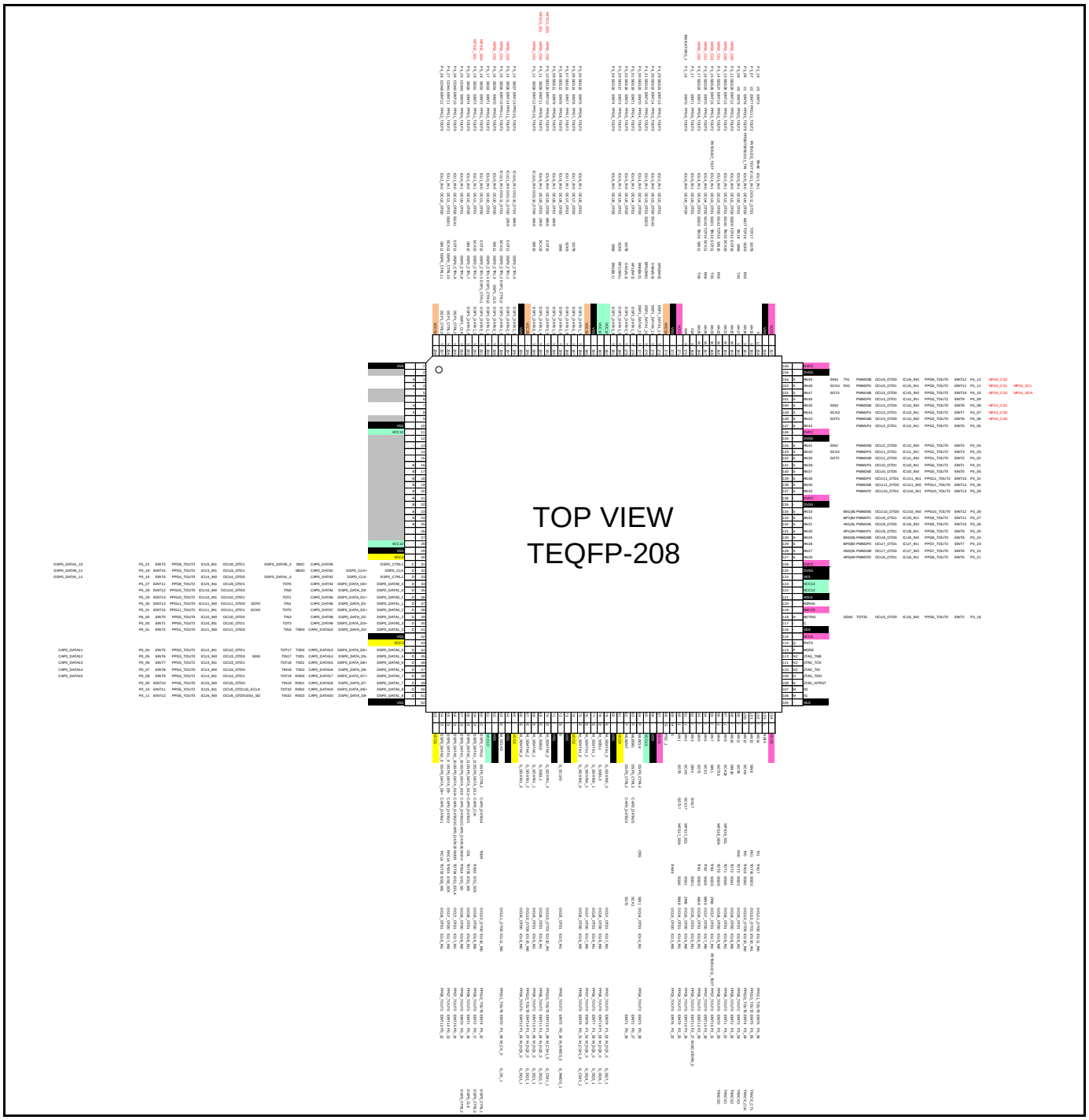
Table 2-3: Function Digit Table

Part Number	S6J32X (X = Function Digit)
Function Digit	**B**
CPU Clock Maximum	160 MHz
Graphics Clock Maximum	160 MHz
Display Output Support	ch.0
Video Capture Support	N/A
Graphic Engine Type	2D
HyperBus Interface	ch.0, 1
Sound System	YES
FPD-Link	N/A
Media System	N/A
Chip Select Output of MFS	N/A
I^2C	MFS ch.16, 17

Notes:

- *This table only shows the relation between the optional function and the part numbers. That is, all products are not necessarily available for orders. See the order number on the datasheet, and confirm actual availabilities of products.*
- *The sound system is composed of the sound waveform generator, the sound mixer, the audio DAC, PCM-PWM, and I2S0.*
- *The media system means both Ethernet AVB and Media LB.*
- *The CLK_CPU is assigned for CPU clock. The CLK_CD3A0 is assigned for Graphic clock. They are defined at the chapter of Clock Configuration.*
- *Display Output ch.0 is used for RSDS and FPD-LINK (LVDS) as well as DRGB (Digital RGB). The ch.0 of the product which doesn't support FPD-LINK is used for RSDS and DRGB.*
- *HyperBus Interface ch.0 for MCU and ch.1 for graphic subsystem cannot be used simultaneously.*

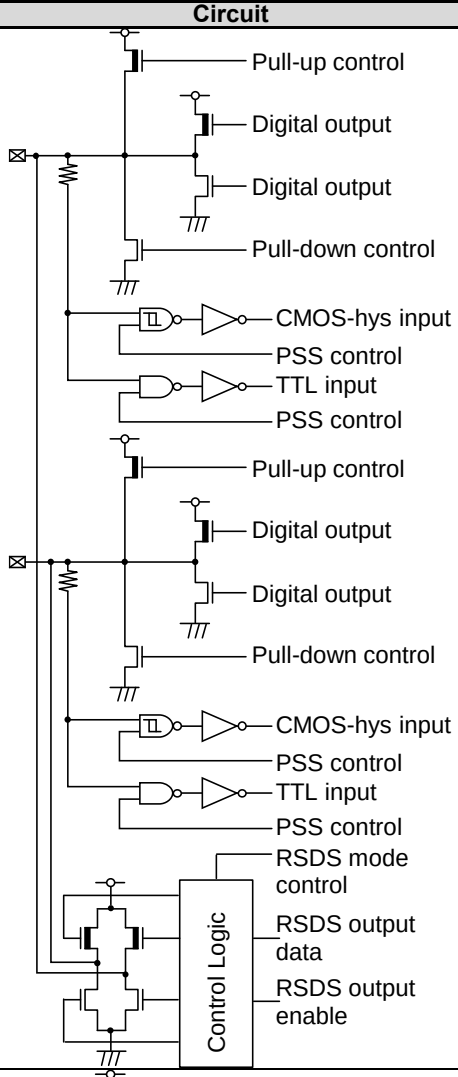
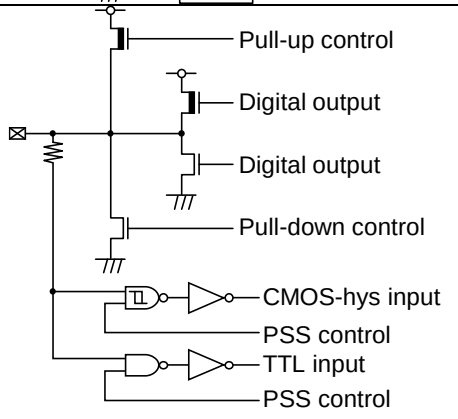
Figure 4-14: TEQFP-208 (S6J323CKxx)



Notes:

- *The pins highlighted in "red" font are not supported for products with revision A and C.*
- *Any function at the following pins is not supported.*

Package Pin Number	Condition on PCB
2, 5, 6, 9, and 12 to 27	Set to ground
3, 4, 7, 8	Open

Type	Circuit	Remark
D		– General-purpose I/O port – Output 2 mA, 5 mA, 10 mA or 20 mA selectable – 33 kΩ with pull-up resistor control – 33 kΩ with pull-down resistor control – CMOS hysteresis input – TTL input – RSDS differential output data
E		– General-purpose I/O port – Output 2 mA, 5 mA or 10 mA selectable – 33 kΩ with pull-up resistor control – 33 kΩ with pull-down resistor control – CMOS hysteresis input – TTL input

6. Port Description

6.1 Port Description List

The table shows the port function of description which is supported. The port function which is not described in the table is not supported for the product.

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
VCC12	+1.2-V power supply pin	11, 28, 61, 85, 122, 123, 182, 183	11, 28, 63, 87, 128, 129, 190, 191	
VCC5	+5.0-V power supply pin	87, 104, 115, 157, 171	89, 108, 119, 163, 179	
VCC3	+3.3-V power supply pin	30, 43, 53, 65, 74, 81	30, 43, 55, 67, 76, 83	
VCC53	+3.3 V/+5.0 V selection power supply pin	173, 185, 194, 208	181, 193, 202, 216	
VCC3_LVDS_Tx	LVDS Tx power supply pin	14, 27	14, 27	
VSS	GND	1, 10, 29, 42, 52, 62, 64, 71, 73, 80, 86, 105, 116, 124, 158, 172, 184, 195	1, 10, 29, 42, 54, 64, 66, 73, 75, 82, 88, 109, 120, 130, 164, 180, 192, 203	
VSS_LVDS_Tx	LVDS Tx GND	15, 26	15, 26	
AVCC3_DAC	Audio DAC power supply pin	6	6	
AVCC3_LVDS_PLL	LVDS PLL power supply pin	13	13	
AVSS_LVDS_PLL	LVDS PLL GND	12	12	
AVCC5	A/D converter analog power supply pin	119	125	
AVRH5	A/D converter upper limit reference voltage pin	120	126	
AVSS	A/D converter GND	2, 5, 9, 121	2, 5, 9, 127	
DVCC	SMC large current port power supply pin	126, 136, 146,156	132, 142, 152,162	
DVSS	SMC large current port GND	125, 135, 145,155	131, 141, 151, 161	
X1	Main clock oscillator output pin	106	110	
X0	Main clock oscillator input pin	107	111	
X1A	Sub-clock oscillator output	169	177	
X0A	Sub-clock oscillator input	170	178	
NMIX	Non-maskable interrupt input pin	103	107	
RSTX	External reset input pin	114	118	
PSC_1	External Power Supply Control pin	88	90	
MODE	Mode Pin	113	117	
C	External capacity connection output pin	117	121	
JTAG_NTRST	JTAG test reset input pin	108	112	
JTAG_TDO	JTAG test data output pin	109	113	
JTAG_TDI	JTAG test data input pin	110	114	
JTAG_TCK	JTAG test clock input pin	111	115	
JTAG_TMS	JTAG test mode state input pin	112	116	
TRACE0	Trace data 0 output pin	96	100	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
EINT11	External interrupt input pin	34, 50, 69, 92, 133, 153, 192, 206	34,52,71, 95,139,159, 170, 200, 214	
EINT12	External interrupt input pin	35, 51, 66, 134, 154, 163, 193, 207	35, 53, 68, 96, 140, 160, 171, 201, 215	
EINT13	External interrupt input pin	36, 54, 68, 93, 137, 164, 174, 196	36, 56, 70, 97, 143, 172, 182, 204	
EINT14	External interrupt input pin	37, 55, 67, 94, 138, 165, 175, 197	37, 57, 69, 98, 144, 173, 183, 205	
EINT15	External interrupt input pin	32, 38, 56, 70, 95, 139, 166, 176, 198	32, 38, 58, 72, 99, 145, 174, 184, 206	
MFS0_CS0	Multi-function serial ch.0 chip select 0 pin	148	154	
MFS0_CS1	Multi-function serial ch.0 chip select 1 pin	153	159	
MFS0_CS2	Multi-function serial ch.0 chip select 2 pin	154	160	
MFS0_CS3	Multi-function serial ch.0 chip select 3 pin	152	158	
MFS2_CS0	Multi-function serial ch.2 chip select 0 pin	149	155	
MFS2_CS1	Multi-function serial ch.2 chip select 1 pin	150	156	
MFS8_CS0	Multi-function serial ch.8 chip select 0 pin	163, 191	171, 199	
MFS8_CS1	Multi-function serial ch.8 chip select 1 pin	167, 198	175, 206	
MFS8_CS2	Multi-function serial ch.8 chip select 2 pin	168, 199	176, 207	
MFS8_CS3	Multi-function serial ch.8 chip select 3 pin	166, 197	174, 205	
MFS9_CS0	Multi-function serial ch.9 chip select 0 pin	164, 192	172, 200	
MFS9_CS1	Multi-function serial ch.9 chip select 1 pin	165, 193	173, 201	
SCK0	Multi-function serial ch.0 clock I/O pin	38, 91	38, 94	
SCK1	Multi-function serial ch.1 clock I/O pin	83, 94	85, 98	
SCK2	Multi-function serial ch.2 clock I/O pin	143	149	
SCK3	Multi-function serial ch.3 clock I/O pin	149	155	
SCK4	Multi-function serial ch.4 clock I/O pin	153	159	
SCK8	Multi-function serial ch.8 clock I/O pin	100, 180	104, 188	
SCK9	Multi-function serial ch.9 clock I/O pin	161, 188	167, 196	
SCK10	Multi-function serial ch.10 clock I/O pin	164, 192	172, 200	
SCK11	Multi-function serial ch.11 clock I/O pin	167, 198, 206	175, 206, 214	
SCK12	Multi-function serial ch.12 clock I/O pin	202	210	
SCK16	Multi-function serial ch.16 clock I/O pin	97	101	
SCK17	Multi-function serial ch.17 clock I/O pin	91	94	
SIN0	Multi-function serial ch.0 serial data input pin	45, 92	47, 95	
SIN1	Multi-function serial ch.1 serial data input pin	84, 95	86, 99	
SIN2	Multi-function serial ch.2 serial data input pin	144	150	
SIN3	Multi-function serial ch.3 serial data input pin	150	156	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
TXD1	Ethernet pin	45	47	
TXD2	Ethernet pin	46	48	
TXD3	Ethernet pin	47	49	
COL	Ethernet pin	58	44, 60	
CRS	Ethernet pin	84	45, 86	
RXER	Ethernet pin	56	58	
RXDV	Ethernet pin	57	59	
RXCLK	Ethernet pin	55	57	
TXER	Ethernet pin	60	62	
TXEN	Ethernet pin	41	41	
TXCLK	Ethernet pin	54	56	
MDC	Ethernet pin	31	31	
MDIO	Ethernet pin	32	32	
MLBCLK	MediaLB pin	84	86	
MLBDAT	MediaLB pin	82	84	
MLBSIG	MediaLB pin	83	85	
TxCLK-	LVDS clock output pin	21	21	Described as TXOUT4M in FPD-Link Converter
TxCLK+	LVDS clock output pin	20	20	Described as TXOUT4P in FPD-Link Converter
TxDOUT0-	LVDS data output pin	25	25	Described as TXOUT0M in FPD-Link Converter
TxDOUT0+	LVDS data output pin	24	24	Described as TXOUT0P in FPD-Link Converter
TxDOUT1-	LVDS data output pin	23	23	Described as TXOUT1M in FPD-Link Converter
TxDOUT1+	LVDS data output pin	22	22	Described as TXOUT1P in FPD-Link Converter
TxDOUT2-	LVDS data output pin	19	19	Described as TXOUT2M in FPD-Link Converter
TxDOUT2+	LVDS data output pin	18	18	Described as TXOUT2P in FPD-Link Converter
TxDOUT3-	LVDS data output pin	17	17	Described as TXOUT3M in FPD-Link Converter
TxDOUT3+	LVDS data output pin	16	16	Described as TXOUT3P in FPD-Link Converter
G_SCLK0	Graphic HS-SPI clock output pin	72	74	
G_SDATA0_0	Graphic HS-SPI0 data 0 pin	75	77	
G_SDATA0_1	Graphic HS-SPI0 data 1 pin	77	79	
G_SDATA0_2	Graphic HS-SPI0 data 2 pin	76	78	
G_SDATA0_3	Graphic HS-SPI0 data 3 pin	79	81	
G_SDATA1_0	Graphic HS-SPI1 data 0 pin	66	68	
G_SDATA1_1	Graphic HS-SPI1 data 1 pin	68	70	
G_SDATA1_2	Graphic HS-SPI1 data 2 pin	67	69	

8.4 AC Characteristics

8.4.1 Source Clock Timing

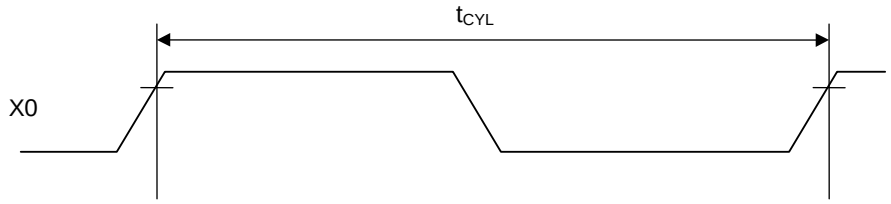
(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	FC	X0, X1	-	3.6	-	16	MHz	
Source oscillation clock cycle time	tCYL	X0, X1	-	62.5	-	277.8	ns	
CAN PLL jitter (when locked)	tPJ	-	-	-10	-	10	ns	
Internal Slow CR oscillation frequency	FCRS	-	-	50	100	150	kHz	
Internal Fast CR oscillation frequency	FCRF	-	-	2.40	4.00	5.61	MHz	Before trim
				3.20	4.00	4.81	MHz	After trim

Notes:

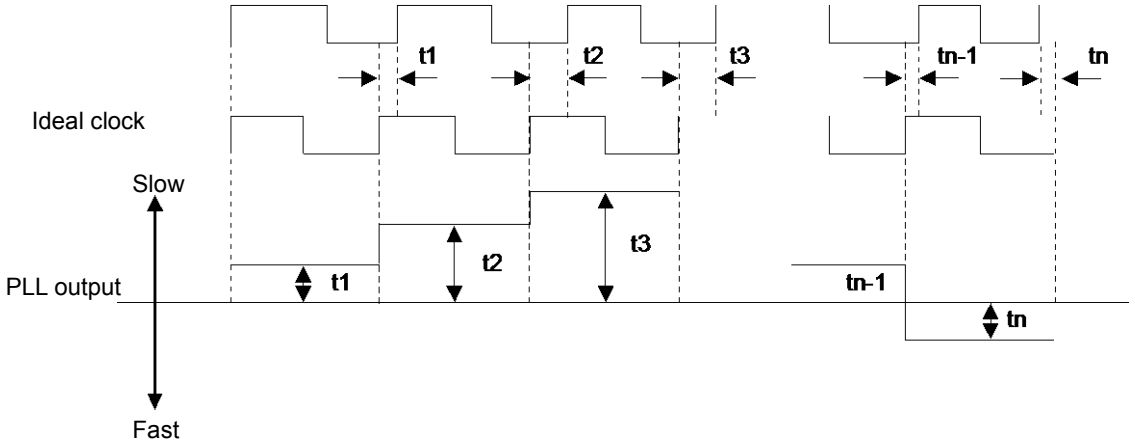
- *The maximum/minimum values have been standardized with the main clock and PLL clock in use.*
- *The error of source oscillator frequency must be smaller than 3000 ppm.*
- *Enough evaluation and adjustment are recommended using oscillator on your system board.*

- X0 and X1 clock timing



CAN PLL jitter

A time difference from the ideal clock is guaranteed for each cycle period within 20,000 cycles.



Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4, SCK8 to SCK12	Slave Mode (CL=20 pF, I_{OL}=-5 mA, I_{OH}=5 mA)	$2t_{CLK\_LCPnA}$*1	-	ns	
				$2t_{CLK\_LCPnA}$*2	-		
		SCK16 to SCK17		$2t_{CLK\_COMP}$	-		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK4, SCK8 to SCK12		$2t_{CLK\_LCPnA}$*1	-	ns	
				$2t_{CLK\_LCPnA}$*2			
		SCK16 to SCK17		$2t_{CLK\_COMP}$	-		
SCK ↓→ SOT delay time	t_{SLOVE}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12,		-	28.5	ns	function digit 3 to 9 K to N
					25*3		
					30		function digit B
		SCK16 to SCK17 SOT16 to SOT17			25		
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17		10	-	ns	function digit 3 to 9 K to N
				11.5			function digit B
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SIN0 to SIN4, SIN8 to SIN12, SIN16 to SIN17		1	-	ns	

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCK falling time	t_F	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17	Slave Mode (CL=20 pF, I_{OL}=-5 mA, I_{OH}=5 mA)	-	5	ns	
SCK rising time	t_R	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17		-	5	ns	

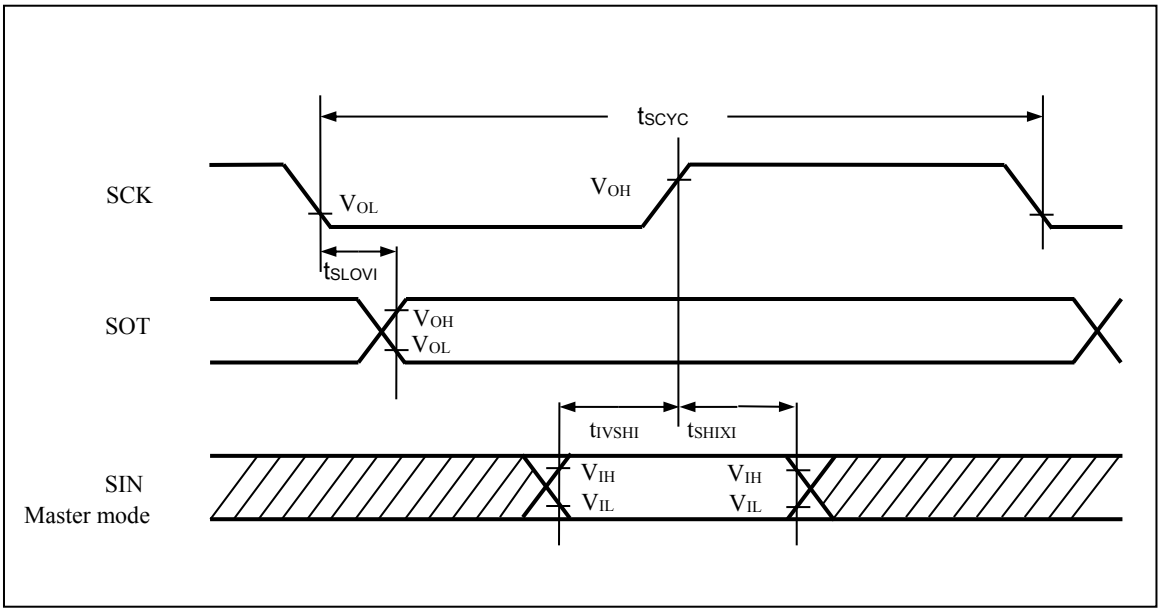
*1: n=0:ch.0 to ch.4, n=1:ch.8 to ch.12

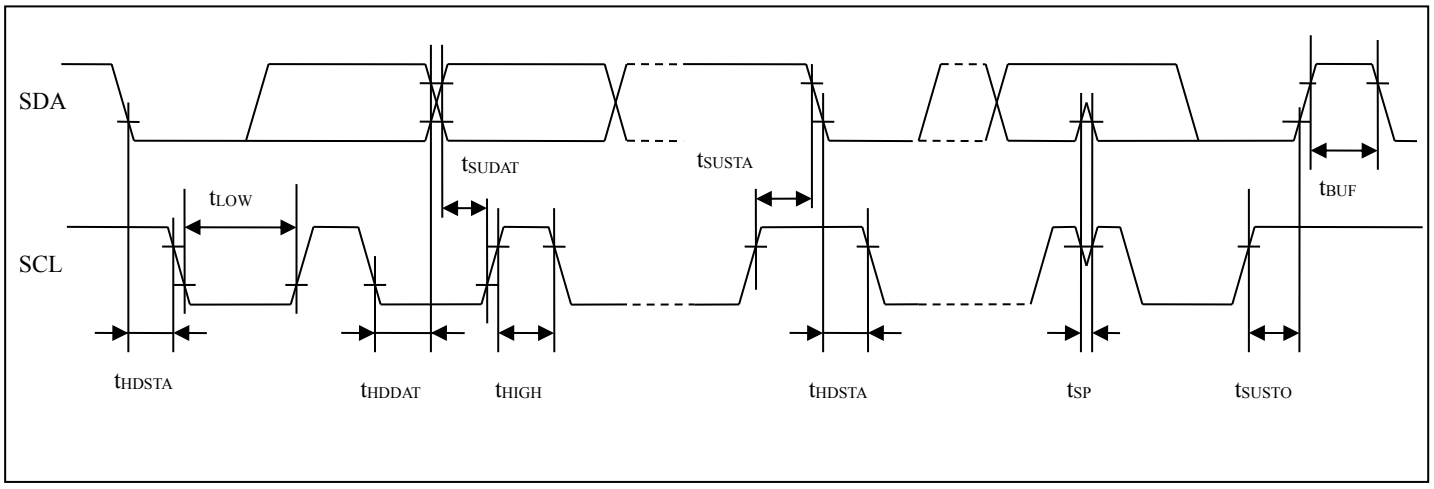
*2: n=0:Group2 of ch.0 /ch1, n=1:Group1 of ch.8 (refer to CHAPTER 11: Port Configuration in HWM)

*3: Group2 of ch.0, ch1, Group1 of ch.8 (refer to CHAPTER 11: Port Configuration in HWM)

Notes:

- *This table provides the alternate current standard for CLK synchronous mode.*
- *CL is the load capability value connected to the pin at the test time.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.*




SDA
SCL
tLOW
tSUDAT
tSUSTA
tBUF
tHDSTA
tHDDAT
tHIGH
tHDSTA
tSP
tSUSTO

8.4.7 Timer Input

(Condition: See 8.2. Operation Assurance)

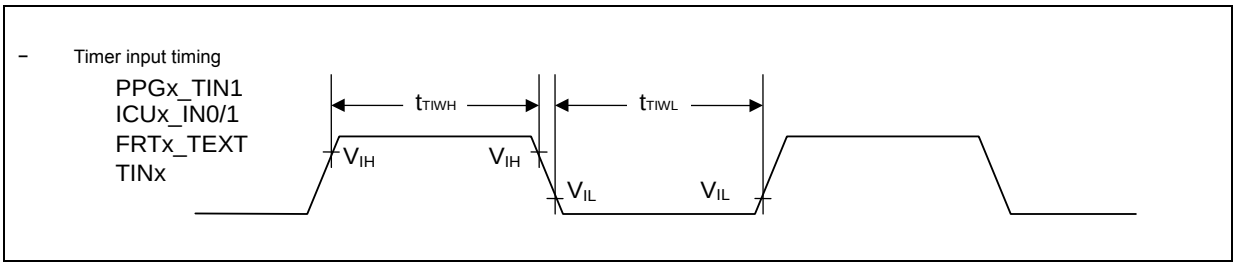
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TWH}, t_{TWL}	PPG0_TIN1 to PPG11_TIN1	-	$4t_{CLK\_LCPnA}$*1	-	ns	$4t_{CLK\_LCPnA}$*1 ≥100 ns
				100			$4t_{CLK\_LCPnA}$*1 <100 ns
		ICU0_IN0 to ICU11_IN0, ICU0_IN1 to ICU11_IN1	-	$4t_{CLK\_LCPnA}$*2	-	ns	$4t_{CLK\_LCPnA}$*2 ≥100 ns
				100			$4t_{CLK\_LCPnA}$*2 <100 ns
		FRT0_TEXT to FRT11_TEXT	-	$4t_{CLK\_LCPnA}$*2	-	ns	$4t_{CLK\_LCPnA}$*2 ≥100 ns
				100			$4t_{CLK\_LCPnA}$*2 <100 ns
		TIN0 to TIN3, TIN16 to TIN19	-	$4t_{CLK\_LCPnA}$*3	-	ns	$4t_{CLK\_LCPnA}$*3 ≥100 ns
				100			$4t_{CLK\_LCPnA}$*3 <100 ns
		TIN32 to TIN35	-	$4t_{CLK\_LLPBM2}$	-	ns	$4t_{CLK\_LLPBM2}$ ≥100 ns
				100			$4t_{CLK\_LLPBM2}$ <100 ns
		TIN48 to TIN49	-	$4t_{CLK\_COMP}$	-	ns	$4t_{CLK\_COMP}$ ≥100 ns
				100			$4t_{CLK\_COMP}$ <100 ns

*1: n=0:ch.0 to ch.5, n=1:ch.6 to ch.11

*2: n=0:ch.0 to ch.7, n=1:ch.8 to ch.11

*3: n=0:ch.0 to ch.3, n=1:ch.16 to ch.19

- Timer input timing

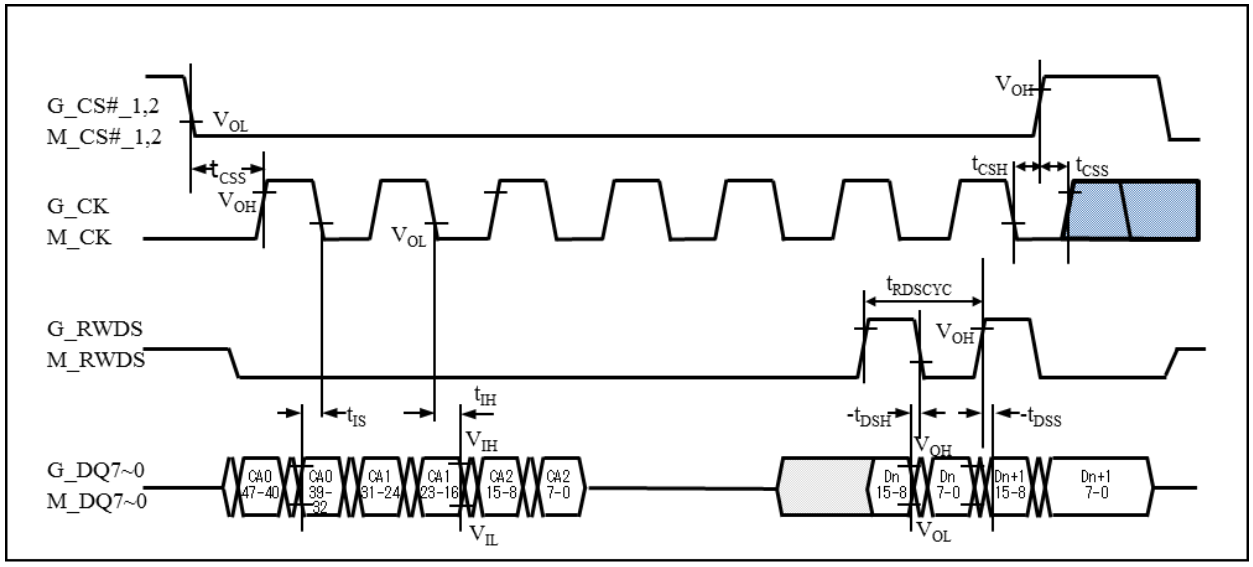


8.4.16.3 Hyper Bus Read Timing (HyperFlash)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Hyper Bus clock cycle	t_{RDSCYC}	G_CK, G_RWDS M_CK, M_RWDS	(CL = 20 pF, I_{OL}=-10 mA, I_{OH}=10 mA),	12.5	-	ns	(A)
				10	-	ns	(B)
CS↑↓ -> CK↑ Chip Select setup time	t_{CSS}	G_CS#_1,2 M_CS#_1,2		t_{RDSCYC} - 3.25	-	ns	(A)
				t_{RDSCYC} -2.0		ns	(B)
DQ -> CK↑↓ Setup time	t_{IS}	G_DQ7-0 M_DQ7-0		1.25	-	ns	
CK↑↓ -> DQ Hold time	t_{IH}	G_DQ7-0 M_DQ7-0		1.25	-	ns	
CK↓ -> CS↑ Chip select hold time	t_{CSH}	G_CS#_1,2 M_CS#_1,2		t_{RDSCYC} / 2	-	ns	
DQ-> RDS↑↓ Setup time	t_{DSS}	G_DQ7-0 M_DQ7-0		-0.8	-	ns	
				-0.85	-		(C)
RDS↑↓-> DQ Hold time	t_{DSH}	G_DQ7-0 M_DQ7-0		-0.8	-	ns	
				-0.9	-		(C)

- *(A): The value is targeted by the product series with revision digit A.*
- *(B): The value is targeted by the product series with after revision digit B.*
- *(C): The value is targeted by the product series with function digit 3 to 9 and revision digit H, M, P.*
- *Hyper Bus clock cycle is always (1/F_{CLK_CD1})*4.*



8.4.18 MediaLB

8.4.18.1 MediaLB Input Timing

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MLBCLK cycle	t_{mckc}	MLBCLK	-	40	-	ns	
MLBSIG, MLBDAT Input setup	t_{dsmcf}	MLBSIG MLBDAT		1.0	-	ns	
MLBSIG, MLBDAT Input hold	t_{dhmcf}	MLBSIG MLBDAT		4.0	-	ns	

Note:

- *CLK_HAPP1B0(internal) frequency > MLBCLK(external) frequency*

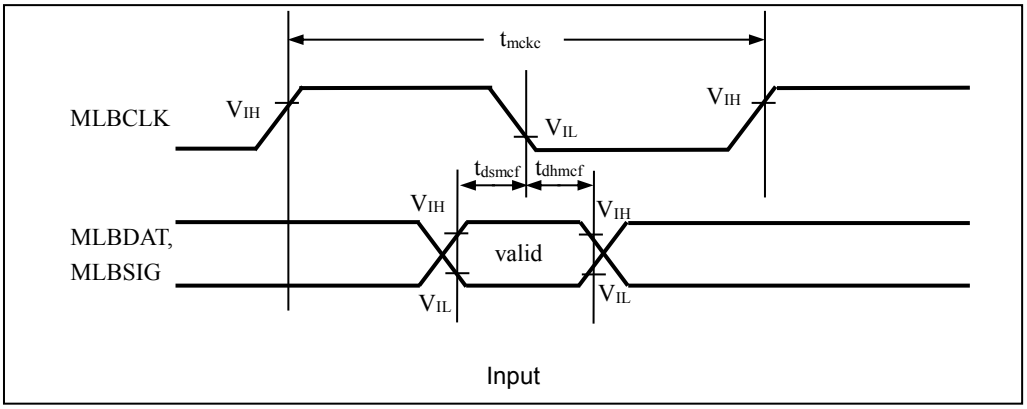
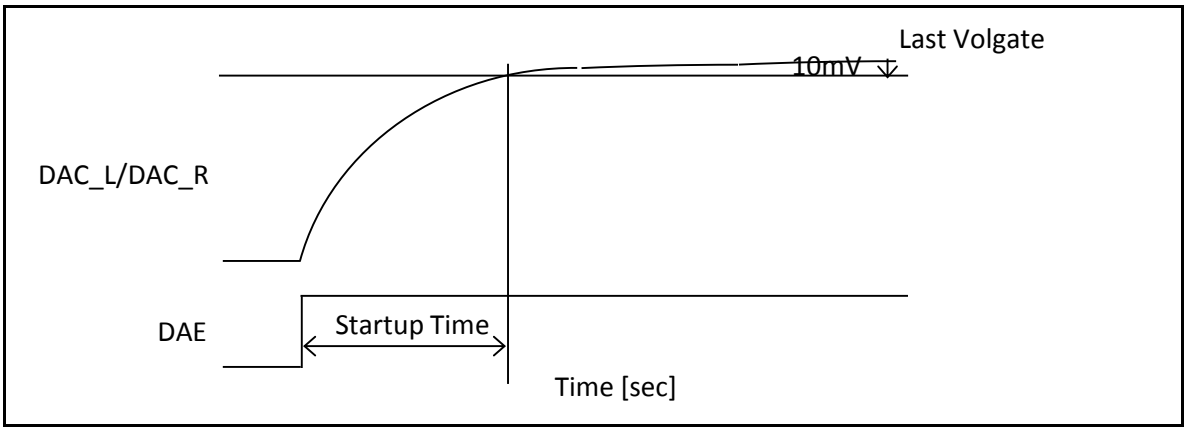


Figure 8-8: Startup Time



Startup time can be calculated as follows.

1. Startup time (TYP) = 650[ms] (Table 5.2)

2. CCOM=10uF×(1±α/100)

CCOM is a capacitor connected to Terminal C_L/C_R including capacitance variance.

α=Capacitance variance [%]

3. Startup time = Start up time (TYP)×(1±α) [ms]

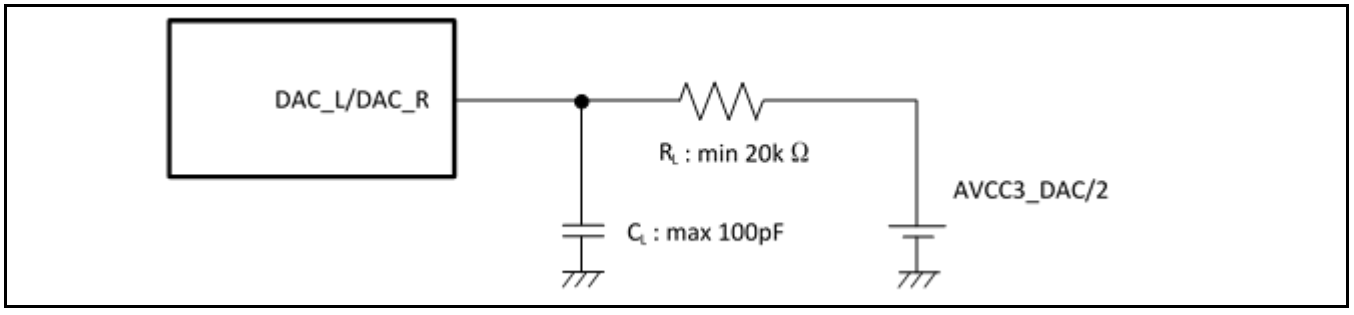
For example, CCOM=11μF then α= (11μF-10μF)/10μF=10[%]

So, Startup time = 650ms × （1+10/100） = 715[ms]

Notes:

- *Two usages of R_L load connection.*
- *Case1: R_L is connected to AVCC3_DAC /2 (Figure 8-9)*
- *Case2: The coupling capacitance must be inserted as shown in (Figure 8-10).*

Figure 8-9: R_L is Connected to AVCC_DAC/2 (Example)



Summary	Error Page	Error	Correct Page	Correct	ID
HyperBus AC specification	108-112	16-1 (3 items) CS ↓ -> RDS ↓ Chip select active to RDS valid (Low): CS ↑ -> RDS(Hi-z) Chip select Inactive to RDS High-Z: CS ↑ -> CS ↓ Chip select HIGH between operation: 16-2 (4 items) CS ↑ -> CS ↓ Chip select HIGH between transaction: CS ↓ -> CS ↑ Chip select maximum LOW time: Read-Writer recovery time : CK ↓ -> CK ↓ (4th) Page open time : 16-3 (7 items) Read Initial Access Time : CS ↑ ↓ -> CK ↑ Chip select active to RDS valid (Low): CS ↑ -> RDS(Hi-Z) Chip select Inactive to RDS High-Z: CK ↑ ↓ -> DQ (Low Z) Clock to DQs Low Z: CS ↑ -> DQ (Hi-Z) Chip select Inactive to DQs High-Z: CK ↑ ↓ -> RDS ↑ ↓ CK transition to RDS transition: CS ↑ -> CS ↓ Chip select HIGH between Operation: 16-4 (8 items) CK ↓ -> CK ↓ (4th) Page open time: CS ↑ -> RWDS(Hi-Z) Chip select Inactive to RWDS High-Z: CK ↑ ↓ -> DQ (Low Z) Clock to DQs Low Z: CS ↑ -> DQ (Hi-Z) Chip select Inactive to DQs High-Z: CK ↑ ↓ -> RWDS ↑ ↓ CK transition to RWDS transition: CS ↑ -> CS ↓ Chip select HIGH between Transition: CS ↓ -> CS ↑ Chip select maximum LOW time: Read-Writer recovery time	109-112	(Removed)	#173

Summary	Error Page	Error	Correct Page	Correct	ID
Power dissipation and Operation temperature	62	-	77, 78	Power dissipation and Operation temperature Case 1, PD - 3300 mW, TA -40 +97 degC, Both should be satisfied. TC -40 +144 degC, Power dissipation and Operation temperature Case 2, PD - 3150 mW, TA -40 +100 degC, Both should be satisfied. TC -40 +144 degC, Power dissipation and Operation temperature Case 3, PD - 3000 mW TA -40 +102 degC, Both should be satisfied. TC -40 +144 degC, Power dissipation and Operation temperature Case 4, PD - 2900 mW, TA -40 +105 degC, Both should be satisfied. TC -40 +144 degC, Power dissipation and Operation temperature Case 5, PD - 2800 mW, TA -40 +105 degC, Both should be satisfied. TC -40 +144 degC, System Thermal Resistance, Theta j-a - 16 degC/W, The minimum value depends on the system specification of heat radiation. The described value is estimated under the condition which is specified at Operation Assurance Condition. Package Thermal Resistance, Theta j-c - 7.5 degC/W,	#317

Summary	Error Page	Error	Correct Page	Correct	ID
Delete "Taget spec"	99, 100, 131-134, 138, 140,142-150, 159	-	98, 99, 100, 131-134, 138, 140, 142-150, 159	(Deleted explanation for target spec)	#504
SSCG Max Frequency	100	Notes: — *1: Target maximum clock frequencies when CPU clock = 240MHz - 232MHz or less is available for SSCG Down Spread. - 240MHz or less is available for PLL.	99	Notes: – *1: Target maximum clock frequencies when CPU clock = 240MHz - 232MHz or less is available for SSCG Down Spered on/off. - 240MHz or less is available for PLL.	#487
Internal Clock Timing	100	Notes:,,,- *3: Target maximum clock frequencies when CPU clock = 160MHz- From *1 to *3, they are not applied to the product series with function digit A, B, C, and D. - *4: Target maximum clock frequencies when CPU clock = 160MHz for the product series with thefunction digit A, B, C, and D.	100	Notes:,,,- *3: Target maximum clock frequencies when CPU clock = 160MHz. This is also a combination of maximum clock frequencies for TC FLASH Programming or Erasing.- From *1 to *3, they are applied to the product series with function digit 3, 4, 5, 6, 7, and 8.- *4: Target maximum clock frequencies when CPU clock = 160MHz for the product series with the function digit A, B, C, and D. This is also a combination of maximum clock frequencies for TC FLASH Programming or Erasing.	#406
Level detection hysteresis width	105	Level detection hysteresis width	104	(Delete)	#457
Default Value of LVDL1	126	LVDL1V=01(Default),,, LVDL1V=10	125	LVDL1V=01,,, LVDL1V=10(Default)	#502
Display AC specification	131	-	131	(- Updated the min/max value in |tDC0D| and tDC0V. - Added the new definition for DSP0_CTRL11-0 of tDC0V. - Update the note for *2 and delete the note for *4. - Updated figure for definition of tDC0V.)	#347

Summary	Error Page	Error	Correct Page	Correct	ID
Display AC specification	132	-	132	(- Updated the min/max value for |tRSD|, tRSV, tSPD, tSPV. - Delete the note for *2. - Updated figure for definition of tSPV and tRSV.)	#506
Display AC specification	133	-	133	(- Updated the min/max value for tDC1D, tDC1V and delete the remarks for tDC1V. - Updated figure for definition of tDC1V.)	#505
FPD-Link Output Clock Frequency	135	Output clock frequency: 1MHz(min),50MHz(max)	135	Output clock frequency: -(min),50MHz(max)	#522
Add "TxCLK+/-" in case of don't support FPD-Link	135	Note: − All the corresponding ports of products which don't support FPD-Link should be connected to GND. AVCC3_LVDS_PLL, AVSS3_LVDS_PLL, VCC3_LVDS_Tx, VSS3_LVDS_Tx, TxDOUTn+/-.	135	Note: − All the corresponding ports of products which don't support FPD-Link should be connected to GND. AVCC3_LVDS_PLL, AVSS3_LVDS_PLL, VCC3_LVDS_Tx, VSS3_LVDS_Tx, TxDOUTn+/-, TxCLK+/-.	#525
DDRHSSPI (SDR) clock cycle for Quad Page Program	138	-	138	HSSPI clock cycle:20(Min):when Quad Page Program	#484
HyperBus AC specification	144	RDS↑↓> DQ (valid) Setup time ,,, RDS↑↓> DQ (invalid)Hold time	144	RDS↑↓> DQ Setup time ,,, RDS↑↓> DQ Hold time	#519
ADC Software Trimming	153	-	153	8.5.4 Calibration ConditionCalibration Condition A/D Converter should be calibrated under the following condition.AVCC=5.0V AVRH=5.0V Ta=25℃ system clock frequency (CLK_LCP1A)= 10MHz See A/D Converter Calibration on the S6J3200 hardware manual.	#358

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				3.Product Description 3.2 Product Description [Improve] Deleted the unnecessary description for PPU of I2S
				4. Package and Pin Assignment 4.1 Pin Assignment [Improve] Added the part number information for figure 4-8 and 4-15
				4. Package and Pin Assignment 4.1.1 TEQFP-216 Pin Assignment [Improve] Added the "M_CK_0" for TEQFP-216 Pin Assignment
				4. Package and Pin Assignment 4.1.2 TEQPF-208 Pin Assignment [Improve] Corrected part number in figure title. (S6J32xCL -> S6J32xCK)
				4. Package and Pin Assignment 4.1.3 TEQPF-256 Pin Assignment [Improve] Corrected the IO-circuit type for pin.217 to 256
				6. Port Description 6.1 Port Description List [Improve] Added the supplementary information for I2C pin name of SCL, SDA.
				7. Precautions and Handling Devices 7.2 Handling Devices [Improve] Deleted the obsolete description about power ramp rate ("About the Power-on Time")
				7. Precautions and Handling Devices 7.2 Handling Devices [Improve] Removed duplicated description
				7. Precautions and Handling Devices 7.2. Handling Devices [Limitation] Added description of how to turn off VCC12 during power off sequence.
				8. Electric Characteristics 8.1 Absolute Maximum Rating [Improve] Deleted "total maximum clamp current" for special spec.
				8. Electric Characteristics 8.1 Absolute Maximum Rating [Limitation] Added the condition to "Analog pin input voltage"
				8. Electric Characteristics 8.2 Operation Assurance Condition [Improve] clarified the rate of die stage area which is exposed at back surface of package for heat dissipation.
				8. Electric Characteristics 8.3.1 Port Function Characteristics [Improve] Remarks of VOH5 is modified.
				8. Electric Characteristics 8.3.2.1 Run Mode [Improve] Added information. "50 MHz" into AVCC3_LVDS_PLL.
				8. Electric Characteristics 8.3.2.2 PSS Timer Mode Shutdown (PD6=OFF) [Enhance] PD4 shutdown support [Improve] Added remarks in osc mode spec
				8. Electric Characteristics 8.4.1 Source Clock Timing [Improve] Corrected the min value of source oscillation clock cycle time.
				8.Electric Characteristics 8.4.3 Internal Clock Timing [Enhancement] Added support for center spread mode with limited condition