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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-R5F
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, CSIO, Ethernet, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2.112MB (2.112M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.15V ~ 5.5V
Data Converters	A/D 50x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP Exposed Pad
Supplier Device Package	208-TQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6j32baksese2000a

Table 2-4: Function Digit Table

Part Number	S6J32X (X = Function Digit)			
Function Digit	**K**	**L**	**M**	**N**
CPU Clock Maximum	240 MHz	240 MHz	240 MHz	240 MHz
Graphics Clock Maximum	200 MHz	200 MHz	200 MHz	200 MHz
Display Output Support	ch.0, 1	ch.0, 1	ch.0, 1	ch.0, 1
Video Capture Support	1 unit	1 unit	1 unit	1 unit
Graphic Engine Type	2D, 3D	2D, 3D	2D, 3D	2D, 3D
HyperBus Interface	ch.0, 1	ch.0, 1	ch.0, 1, 2	ch.0, 1
Sound System	N/A	YES	YES	N/A
FPD-Link	YES	YES	YES	N/A
Media System	YES	YES	YES	YES
Chip Select Output of MFS	YES	YES	YES	YES
I^2C	MFS ch.4, 10, 12, 16, 17	MFS ch.4, 10, 12, 16, 17	MFS ch.4, 10, 12, 16, 17	MFS ch.4, 10, 12, 16, 17

Notes:

- *This table only shows the relation between the optional function and the part numbers. That is, all products are not necessarily available for orders. See the order number on the datasheet, and confirm actual availabilities of products.*
- *The sound system is composed of the sound waveform generator, the sound mixer, the audio DAC, PCM-PWM, and I2S0.*
- *The media system means both Ethernet AVB and Media LB.*
- *The CLK_CPU is assigned for CPU clock. The CLK_CD3A0 is assigned for Graphic clock. They are defined at the chapter of Clock Configuration.*
- *Display Output ch.0 is used for RSDS and FPD-LINK (LVDS) as well as DRGB (Digital RGB). The ch.0 of the product which doesn't support FPD-LINK is used for RSDS and DRGB.*
- *Display Output ch.1 is used for FPD-LINK (LVDS) and DRGB (Digital RGB). The ch.1 of the product which doesn't support FPD-LINK is used for DRGB only.*
- *HyperBus Interface ch.0 for MCU and ch.1 for graphic subsystem cannot be used simultaneously.*

3. Product Description

3.1 Overview

This section explains the product features of the S6J3200 series. The description of this section should precede the duplicated description on platform manual.

3.2 Product Description

Table 3-1: Product Features

Feature	Description
Technology	55-nm CMOS technology with embedded flash Fully automotive qualified according to ISO/TS 16949 and AEC-Q100
Functional Safety	The product series has some functional safety features suited for ASIL-B application.
Peripherals	See function list.
Power Domain (PD)	See the platform manual and the STATE TRANSITION chapter in detail. The product series supports the power-off control of PD2 (including PD3 and 5), PD4_0, PD4_1, and PD6. The power domain resets of PD3 and PD5 included in PD2 are not supported in the product series, and "0" is always read from the reset factor flags of them. This series does not support partial wakeup for PD6.
Debug and Trace	See the platform manual in detail. − Standard 5-pin JTAG interface − 4k Word Embedded Trace Buffer 4-bit trace support for TEQFP package. Full trace (dedicated 16-bit port) with special bond-out package is planned.
System Control	See the platform manual in detail. Main and sub oscillator is available. − A wide range of 3.6 - 16 MHz is available for main oscillator − 32 KHz is available for sub oscillator Sub clock is enable/disable by register settings
Clock	See the platform manual in detail. CLK_CLKO (Clock Output Function) is not supported. Main Oscillation Stabilization Wait Time (at 4 MHz):8.19 ms (Initial value)
Embedded CR oscillation	See the platform manual in detail. Stabilization time is as followings. − 0.35 ms to 0.8 ms for 4 MHz (Fast clock) − 0.43 ms to 1.28 ms for 100 kHz (Slow clock)
Clock Supervisor	See the platform manual in detail. This product series does not support the clock supervisor output port. (Related register and internal circuit is implemented.)
Reset	See the platform manual in detail. Following resets are not mounted on this device or not supported. − INITX: INITX is issued by simultaneous assert of RSTX and MODE, but this product series does not support INITX. − SRSTX (and nSRST pin) The product series does not support EX5VRST and writing EX5VRSTCNT bits in SYSC0_SPECFGR has no effect.
Hardware Watchdog	See the platform manual in detail. Hardware watchdog function stops during PSS mode. In the related register of HWDG_CFG, the bit ALLOWSTOPCLK is always read as 1 (HWDG_CFG.ALLOWSTOPCLK=1). The product series does not support Watchdog Counter Monitor Output port. (Related register and internal circuit is implemented.)

3.2.1 *Ethernet*

The following functions are not supported.

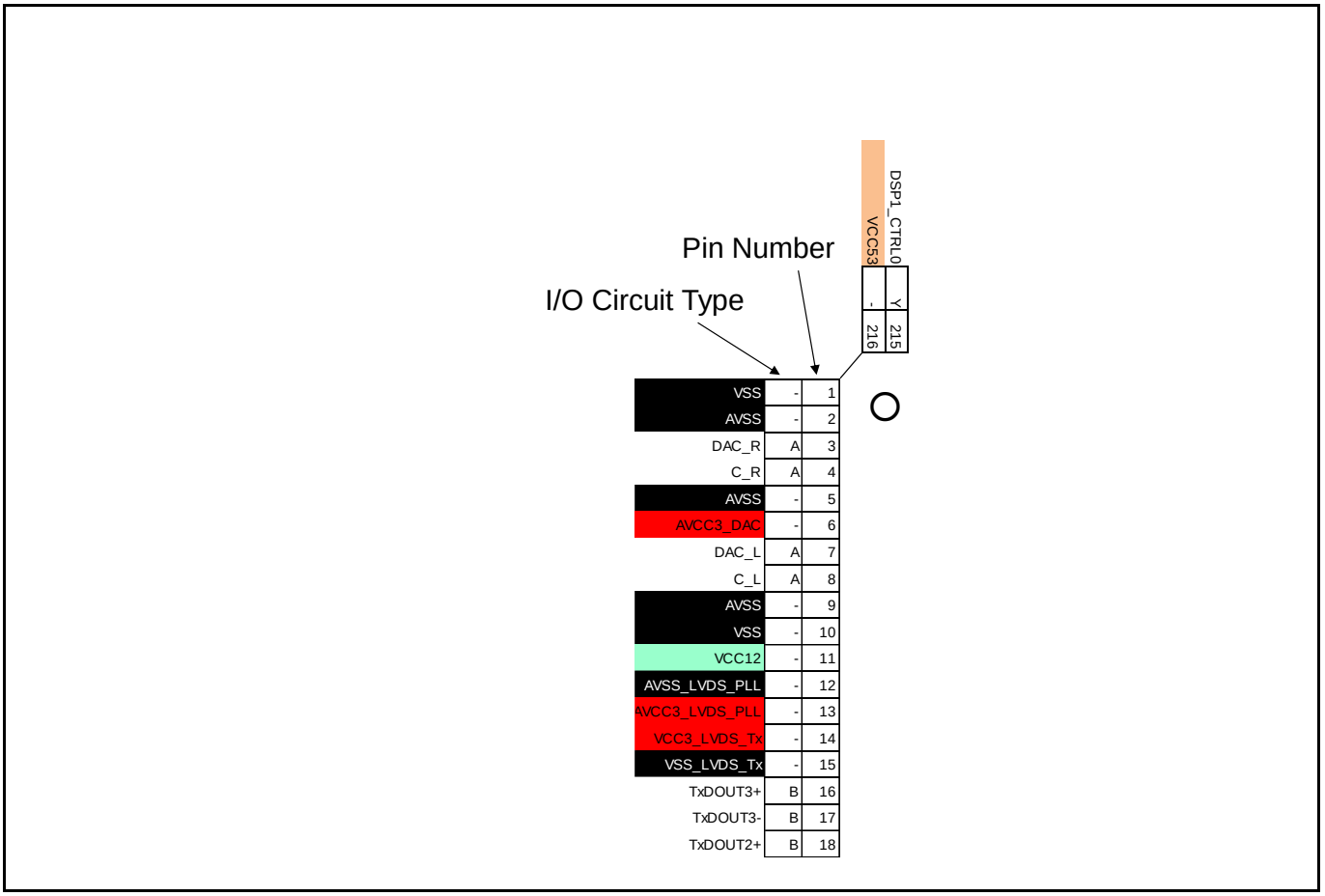
Functions	Remark
External FIFO Interface	
Additional Low Latency TX FIFO Interface for DMA configurations	
MAC Transmit Block - half-duplex - collision - back_pressure	
MAC Filtering Block - external address match - Wakeup On Lan	
Energy Efficient Ethernet support	
LPI Operation in Cadence IP	
PHY Interface - GMII - SGMII - TBI	
10/100/1000 Operation - 1000 M	
SGMII Operation	
Jumbo Frames	
Physical Control Sub-Layer	

4. Package and Pin Assignment

4.1 Pin Assignment

The characters next to the pin number in the pin assignment drawing specify the I/O circuit type.

Figure 4-1: Pin Number and I/O Circuit Type

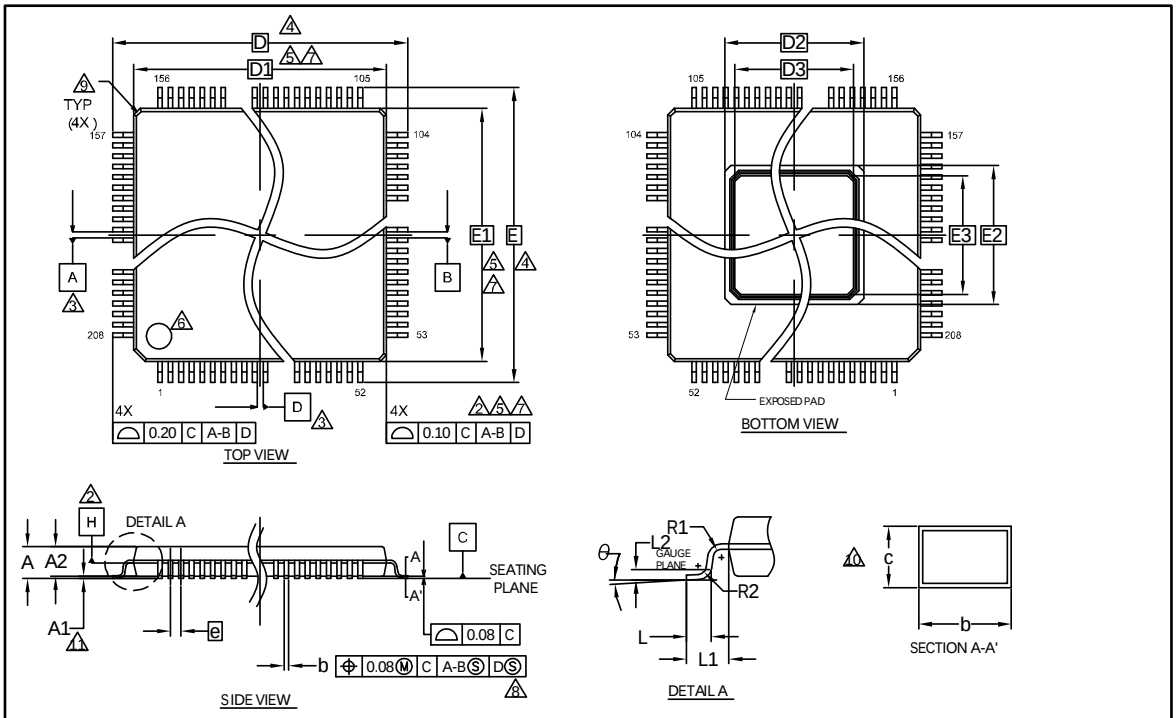


Function Digit	TEQFP-216	TEQFP-208	TEQFP-256
S6J328, S6J329, S6J32M	Figure 4-2	Figure 4-9	Figure 4-17
S6J327	Figure 4-3	Figure 4-10	-
S6J326, S6J32L	Figure 4-4	Figure 4-11	-
S6J325, S6J32N	Figure 4-5	Figure 4-12	-
S6J324	Figure 4-6	Figure 4-13	-
S6J323	Figure 4-7	Figure 4-14	-
S6J32K	Figure 4-8	Figure 4-15	-
B	-	Figure 4-16	-

4.2.2 TEQFP208

Figure 4-19: LET208

Package Type	Package Code
TEQFP208	LET208



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D		30.00 BSC	
D1		28.00 BSC	
D2		9.90 REF	
D3		8.71 REF	
E		30.00 BSC	
E 1		28.00 BSC	
E 2		9.90 REF	
E 3		8.71 REF	
R 1	0.08	—	—
R 2	0.08	—	0.20
θ	0°	4°	8°
c	0.12	—	0.20
b	0.17	0.22	0.27
L	0.45	0.60	0.75
L 1		1.00 REF	
L 2		0.25	
e		0.50 BSC	

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13651 *A

PACKAGE OUTLINE, 208 LEAD TEQFP
28.0X28.0X1.7 MM LET208 REV*A

7.2 Handling Devices

For Latch-Up Prevention

The latch-up phenomenon may occur on a CMOS IC in the following cases: the voltage applied to an input or output pin is higher than VCC or lower than VSS; or the voltage applied between a VCC pin and a VSS pin exceeds the rating. A latch-up causes a rapid increase in the power supply current, possibly resulting in thermal damage to an element. When using the device, take sufficient care not to exceed the maximum rating.

About Handling Unused Pins

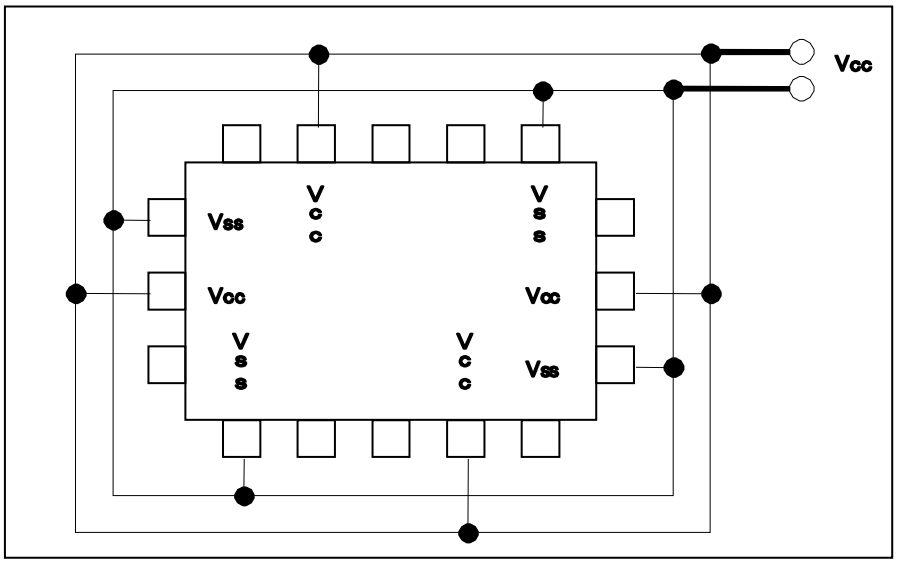
Leaving unused input pins open may cause permanent damage from a malfunction or latch-up. Take measures for unused pins, such as pulling up or pulling down the voltage with resistors of 2 kilo ohms or higher.

If there are any unused input/output pins, set them to the output state and then open them, or set them to the input state and handle them in the same way as input pins.

About Power Supply Pins

If the device has multiple VCC and VSS pins, the device is designed in such a way that the pins that should be at the same potential are connected to each other inside the device to prevent malfunctions such as latch-up. However, to reduce unwanted emissions, prevent malfunctions of strobe signals caused by an increase of the ground level, and observe standards on total output current, be sure to connect all the VCC and VSS pins to the power source and ground externally. Also handle all the VSS power supply pins in this way as shown in the following diagram. If there are multiple VCC or VSS systems, the device does not operate normally even within the guaranteed operating range.

Figure 7-1 Pin Assignment



In addition, consider connecting with low impedance from the power supply source to the VCC and VSS of this device.

We recommend connecting a ceramic capacitor as a bypass capacitor between VCC and VSS, near this device.

About the Crystal Oscillation Circuit

Noise entering the X0 or X1 pin may cause a malfunction. Design the printed circuit board in such a way that the X0 and X1 pins, the crystal oscillator (or ceramic resonator), and a bypass capacitor to ground are located very close to the device.

We recommend that the printed circuit board artwork have the X0 and X1 pins enclosed by ground.

About the Mode Pin (MD)

Use mode pin MD by directly connecting it to a VCC or VSS pin. To prevent noise from causing the device to accidentally enter test mode, reduce the pattern length between each mode pin and a VCC or VSS pin on the printed circuit board, and connect them with low impedance.

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
System Thermal Resistance	Theta j-a	-	16	°C/W	The minimum value depends on the system specification of heat radiation. The described value is estimated under the condition which is specified at Operation Assurance Condition.
Package Thermal Resistance	Theta j-c	-	7.5	°C/W	-
Storage temperature	Tstg	-55	+150	°C	-

*1: These parameters are based on the condition that VSS=AVSS=DVSS=0.0 V.

*2: Take care that DVCC, AVCC5 do not exceed VCC5 at, for example, the power-on time.

*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

*6: Output of 5-V pins.

*7: Output of SMC pins.

*8: Output of 5-V/3-V pins.

*9: Output of 3-V pins.

*10: Output of I^2C.

*11: Output of Media LB pins

*12: VI or VO should never exceed the specified ratings. However, if the maximum current to/from an input is limited by a suitable external resistor, the ICLAMP rating supersedes the VI rating.

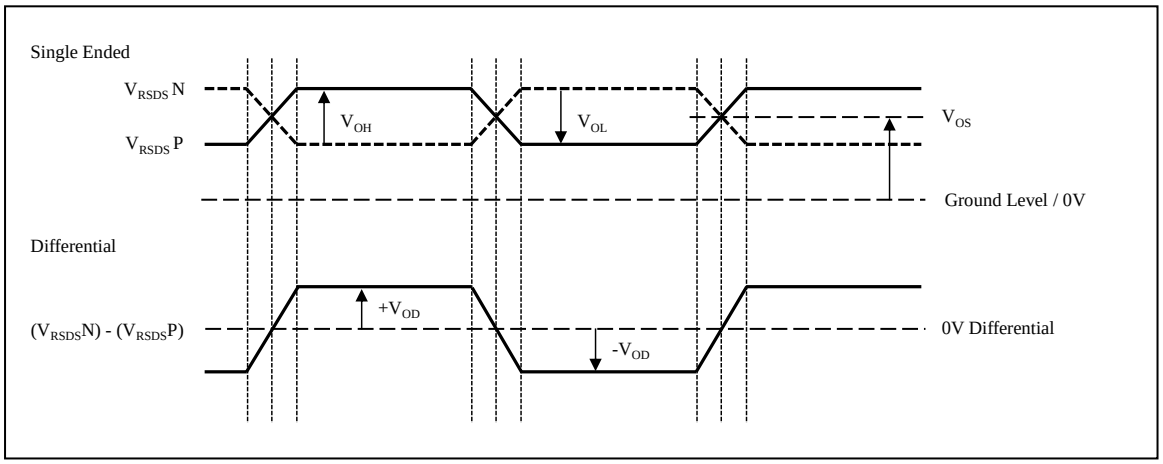
*13: Take care that the output voltage does not exceed AVCC5 + 0.3 V because ADC Analog input pins (AN0-49) are internally connected to the analog elements.

*A: Relevant pins: All general-purpose ports and analog input pins

- Corresponding pins : all general-purpose ports
- Use within the operation assurance condition (See 8.2. Operation Assurance).
- Use at DC voltage (current).
- The +B signal should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the +B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the VCC pin via a protective diode, possibly affecting other devices.
- Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave + B input pins open.

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Output Differential Voltage	$\lvert V_{OD} \rvert$	DSP0_DATAn+, DSP0_DATAn- n=0 to 11	BOOST=0 (Drivability 2mA) R_L = 100 Ω	100	200	600	mV	
			BOOST=1 (Drivability 4mA) R_L = 50 Ω					
Output Offset Voltage	V_{OS}		BOOST=0 (Drivability 2mA) R_L = 100 Ω	0.5	1.2	1.5	V	
			BOOST=1 (Drivability 4mA) R_L = 50 Ω					



8.3.2.3 PSS Stop Mode Shutdown

■This characteristic is specified for the series with the function digits 3, 4, 5, 6, 7, 8, 9, K, L, M, and N.

(Condition: See 8.2. Operation Assurance)

Symbol	Pin Name	Conditions	Value		Unit	T_A (°C)	Remark
			Typ	Max			
I_{CCH5}	$V_{CC}5$	PD1=ON, PD4_0=ON, PD4_1=ON	65	270	µA	25	-
		PD1=ON, PD4_0 or PD4_1=ON	60	245	µA	25	-
		PD1=ON	55	220	µA	25	-

■This characteristic is specified for the series with the function digits B.

(Condition: See 8.2. Operation Assurance)

Symbol	Pin Name	Conditions	Value		Unit	T_A (°C)	Remark
			Typ	Max			
I_{CCH5}	$V_{CC}5$	PD1=ON, PD4_0=ON, PD4_1=ON	65	315	µA	25	-
		PD1=ON, PD4_0 or PD4_1=ON	60	290	µA	25	-
		PD1=ON	55	265	µA	25	-

Notes:

- *The values will be evaluated after engineering samples release.*
- *The values have been standardized with regulator standby mode (RMSEL=1).*

8.4 AC Characteristics

8.4.1 Source Clock Timing

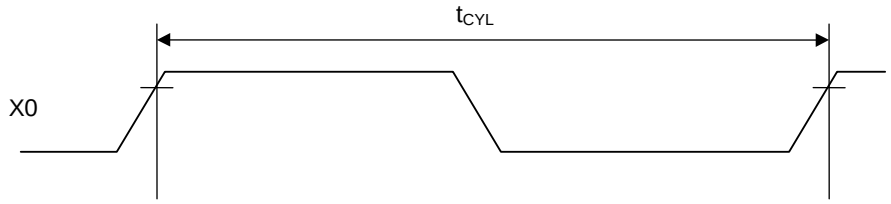
(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	FC	X0, X1	-	3.6	-	16	MHz	
Source oscillation clock cycle time	tCYL	X0, X1	-	62.5	-	277.8	ns	
CAN PLL jitter (when locked)	tPJ	-	-	-10	-	10	ns	
Internal Slow CR oscillation frequency	FCRS	-	-	50	100	150	kHz	
Internal Fast CR oscillation frequency	FCRF	-	-	2.40	4.00	5.61	MHz	Before trim
				3.20	4.00	4.81	MHz	After trim

Notes:

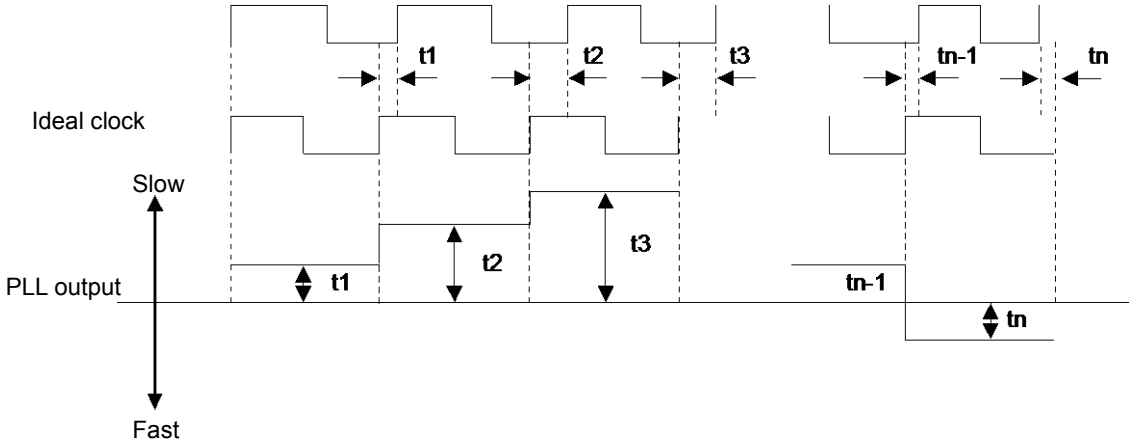
- *The maximum/minimum values have been standardized with the main clock and PLL clock in use.*
- *The error of source oscillator frequency must be smaller than 3000 ppm.*
- *Enough evaluation and adjustment are recommended using oscillator on your system board.*

- X0 and X1 clock timing



CAN PLL jitter

A time difference from the ideal clock is guaranteed for each cycle period within 20,000 cycles.

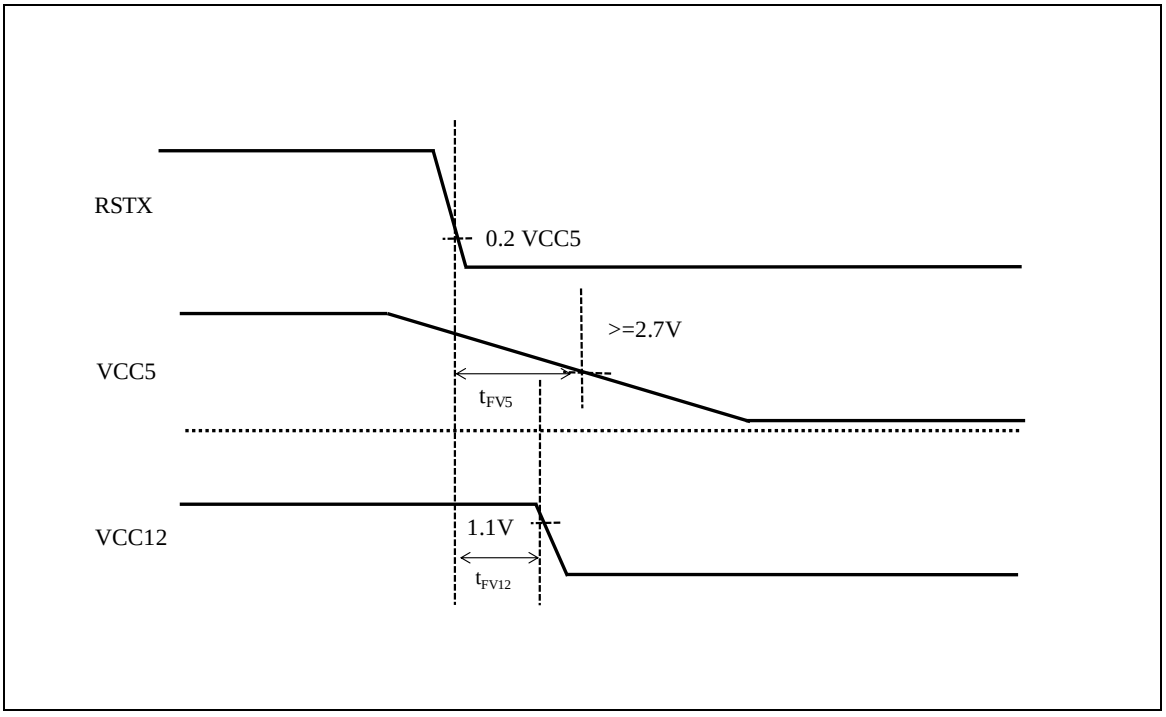


8.4.4.2 Power Supply Voltage Stability Conditions

□ For revision M, P

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
VCC5 stability time after RSTX assertion	t_{FV5}	VCC5	-	35	-	µs	VCC5>=2.7 V
VCC12 stability time after RSTX assertion	t_{FV12}	VCC12		35	-	µs	VCC12>=1.1 V



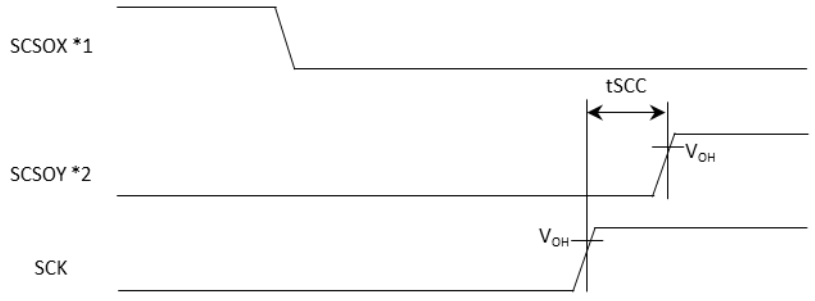
Note:

This AC specification isn't applied except revision M, P.

(2) Normal Synchronous Transfer (SCR: SPI=0) and Mark Level "L" of Serial Clock Output (SMR: SCINV=1)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4, SCK8 to SCK12	Master Mode (CL=20 pF, I_{OL}=-5 mA, I_{OH}=5 mA)	$3t_{CLK\_LCPnA}$ *1	-	ns	
				$3t_{CLK\_LCPnA}$ *2	-		
		SCK16 to SCK17		$3t_{CLK\_COMP}$	-		
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK4, SCK8 to SCK12 SOT0 to SOT4, SOT8 to SOT12		0	30	ns	
				0	20*3		
		SCK16 to SCK17 SOT16 to SOT17		0	15		
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12,		26.5	-	ns	
				20*3	-		
		SCK16 to SCK17 SIN16 to SIN17		20	-		
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 SOT0 to SOT4, SOT8 to SOT12, SOT16 to SOT17		0	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4, SCK8 to SCK12	Slave Mode (CL=20 pF, I_{OL}=-5 mA, I_{OH}=5 mA)	$2t_{CLK\_LCPnA}$ *1	-	ns	
				$2t_{CLK\_LCPnA}$ *2	-		
		SCK16 to SCK17		$2t_{CLK\_COMP}$	-		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK4, SCK8 to SCK12		$2t_{CLK\_LCPnA}$ *1	-	ns	
				$2t_{CLK\_LCPnA}$ *2	-		
		SCK16 to SCK17		$2t_{CLK\_COMP}$	-		



Round Function (CSxSCINV=1, CSxLVL=0), (CSySCINV=0, CSyLVL=0)

*1: X is 0 to 3.

*2: Y is 0 to 3. However, Y and X is a different value.

8.4.10 Low-Voltage Detection

8.4.10.1 LVDL0

(Condition: See 8.2. Operation Assurance)

Parameter	Pin Name	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detection Voltage	-	-	0.9	0.95	1.0	V	*1
Release Voltage	-	-	0.925	1.025	1.125	V	
Level Detection Time	-	-	-	-	30	µs	*2

Notes:

- **1: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.*
- **2: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.*

8.4.10.2 LVDH0

Note:

- *LVDH0 is only used to generate power-on reset. Refer to chapter Power-On Conditions for related parameters.*

8.4.10.3 LVDL1

(Condition: See 8.2. Operation Assurance)

Parameter	Pin Name	Conditions	Value			Unit	Guaranteed MCU Operation Range	Remarks
			Min	Typ	Max			
Detection Voltage	-	LVDL1V=10 (Default)	0.92	0.97	1.02	V	No	*1
Release Voltage	-		0.945	1.045	1.145	V		
Detection Voltage	-	LVDL1V=11	1.02	1.07	1.12	V		
Release Voltage	-		1.095	1.145	1.195	V		
Detection Time	-	-	-	-	30	µs	-	*2

Notes:

- **1: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.*
- **2: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.*

8.4.14.2 For Revision F

(Refer to Figure 2-1: Option and Part Number for S6J320C.)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Output clock frequency	f	-	10	-	50	MHz	
Differential output voltage	V_{OD}	R_L = 100 ohm C_L = 5 pF (differential)	210	300	390	mV	One of three is selectable
			250	350	450	mV	
			295	400	505	mV	
Variation of V_{OD}	delta V_{OD}		-	-	25	mV	
Common mode voltage	V_{CM}		1.075	1.200	1.325	V	One of two is selectable
			1.125	1.250	1.375	V	
Variation of V_{CM}	delta V_{CM}		-	-	25	mV	
Cycle time of TXCLKP/M	T_{CIP}	-	20	T	100	ns	Equals 1/f
Duty of TXCLKP/M	T_{CDT}	-	-	4 / 7 x T	-	ns	
Channel to Channel skew of TXOUTxP/M	T_{CSK}	-	-	-	200	ps	
Skew of TXOUTxP and TXOUTxM	T_{DSK}	-	-	-	50	ps	
Output pulse position for bit 0	T_0	f = 50 MHz	-0.25	0	+0.25	ns	
Output pulse position for bit 1	T_1		1 / 7 x T -0.25	1 / 7 x T	1 / 7 x T +0.25	ns	
Output pulse position for bit 2	T_2		2 / 7 x T -0.25	2 / 7 x T	2 / 7 x T +0.25	ns	
Output pulse position for bit 3	T_3		3 / 7 x T -0.25	3 / 7 x T	3 / 7 x T +0.25	ns	
Output pulse position for bit 4	T_4		4 / 7 x T -0.25	4 / 7 x T	4 / 7 x T +0.25	ns	
Output pulse position for bit 5	T_5		5 / 7 x T -0.25	5 / 7 x T	5 / 7 x T +0.25	ns	
Output pulse position for bit 6	T_6		6 / 7 x T -0.25	6 / 7 x T	6 / 7 x T +0.25	ns	

Notes:

- *All the corresponding ports of products which don't support FPD-Link should be connected to GND. AVCC3_LVDS_PLL, AVSS3_LVDS_PLL, VCC3_LVDS_Tx, VSS3_LVDS_Tx, TxDOUTn+/-, TxCLK+/-.*
- *Channel to Channel skew of TXOUTxP/M is included in output pulse position.*

8.4.15.2 DDR-HSSPI Interface Timing (DDR Mode)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
HSSPI clock cycle	t_{cyc}	G_SCLK0 M_SCLK0	(CL = 20 pF, I_{OL}=-10 mA, I_{OH}=10 mA),	12.5	-	ns	
G_SCLK↑↓ -> delayed sample clock↑	t_{spcnt}	-		0	31.5	ns	
GSDATA -> G_SCLK↑↓ Input setup time	t_{isdata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		*1	-	ns	
G_SCLK↑↓ -> GSDATA Input hold time	t_{ihdata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		*1	-	ns	
G_SCLK↑↓ -> GSDATA Output delay time	t_{oddata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		-	tcyc/4 + 1.5	ns	
G_SCLK↑↓ -> GSDATA Output hold time	t_{ohdata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		Tcyc/4 - 1.0	-	ns	
GSSEL ↓ -> G_SCLK Output delay time	t_{odsel}	G_SSEL0, 1 M_SSEL0, 1		- 15.75+(SS 2CD+0.5)*t cyc	-	ns	
G_SCLK↑ -> GSSEL Output hold time	t_{ohsel}	G_SSEL0, 1 M_SSEL0, 1		0.75*tcyc - 2.0	-	ns	

Notes:

- *SS2CD [1:0] should be configured as 01, 10, or 11.*
- *For *1, the delay of the delay sample clock can be configured (DLP function).*

8.4.22 I2S

8.4.22.1 I2S Timing – Master mode (MSMD=1)

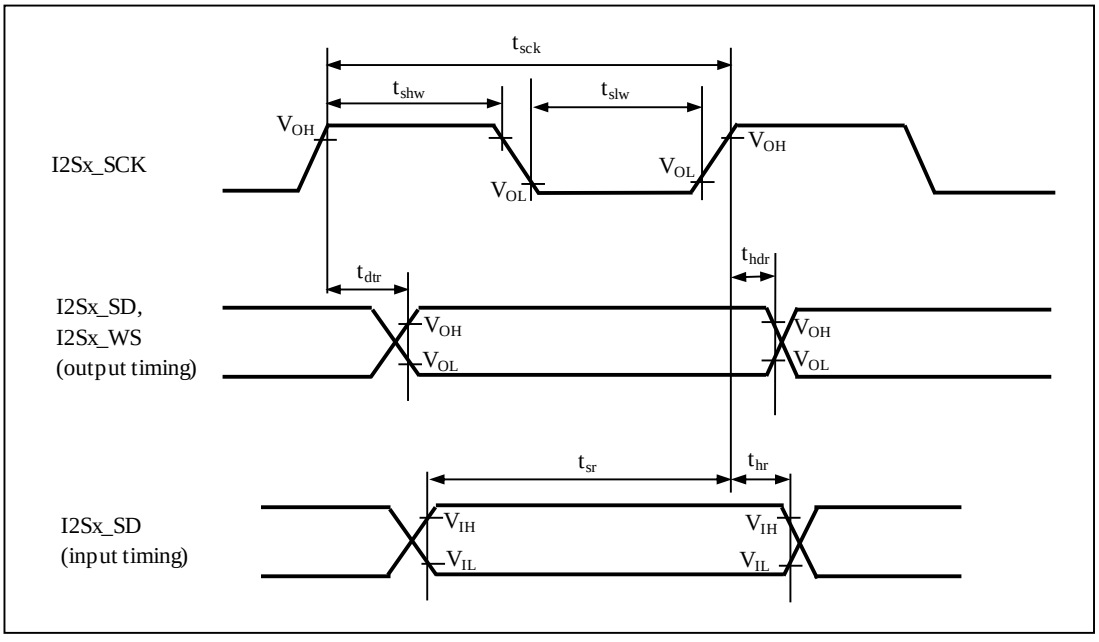
(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
ECLK0/ECLK1 clock cycle	t_{eck}	ECLK0, ECLK1	(CL = 20 pF, I_{OL}=-5 mA, I_{OH}=5 mA) CPOL=0, SMPL=1	20	-	ns	Only relevant if external ECLK input is selected. *1
ECLK0/ECLK1 clock "H" pulse width	t_{ehw}			0.40* t_{eck}	0.60* t_{eck}	ns	
ECLK0/ECLK1 clock "L" pulse width	t_{elw}			0.40* t_{eck}	0.60* t_{eck}	ns	
I2S clock cycle (output SCK)	t_{sck}	I2S0_SCK, I2S1_SCK		66.66	-	ns	
I2S clock "H" pulse width	t_{shw}			0.35* t_{sck}	0.65* t_{sck}	ns	
I2S clock "L" pulse width	t_{slw}			0.35* t_{sck}	0.65* t_{sck}	ns	
Sender delay time SCK↑ -> SD/WS valid	t_{dtr}	I2S0_SCK, I2S1_SCK, I2S0_SD, I2S1_SD, I2S0_WS, I2S1_WS		-	26	ns	*2
Sender hold time SCK↑ -> SD/WS invalid	t_{htr}			-10	-	ns	*2
Receiver setup time SD valid -> SCK↑	t_{sr}	I2S0_SCK, I2S1_SCK, I2S0_SD, I2S1_SD		21	-	ns	*2
Receiver hold time SCK↑ -> SD valid	t_{hr}			10	-	ns	*2

Notes:

*1: ECKM = 1. Refer to the Resource Input Configuration chapter in TRM for required RESSEL register settings.

*2: Refer to the I2S register description chapter in TRM for different combinations of clock polarity (CPOL), sampling point position (SMPL), polarity/pulse_width/frame_sync phase of WS (FSPL, FSLN, FSPH). Actual waveforms and relevant clock edges will change accordingly; the delay values as per above table will remain the same.



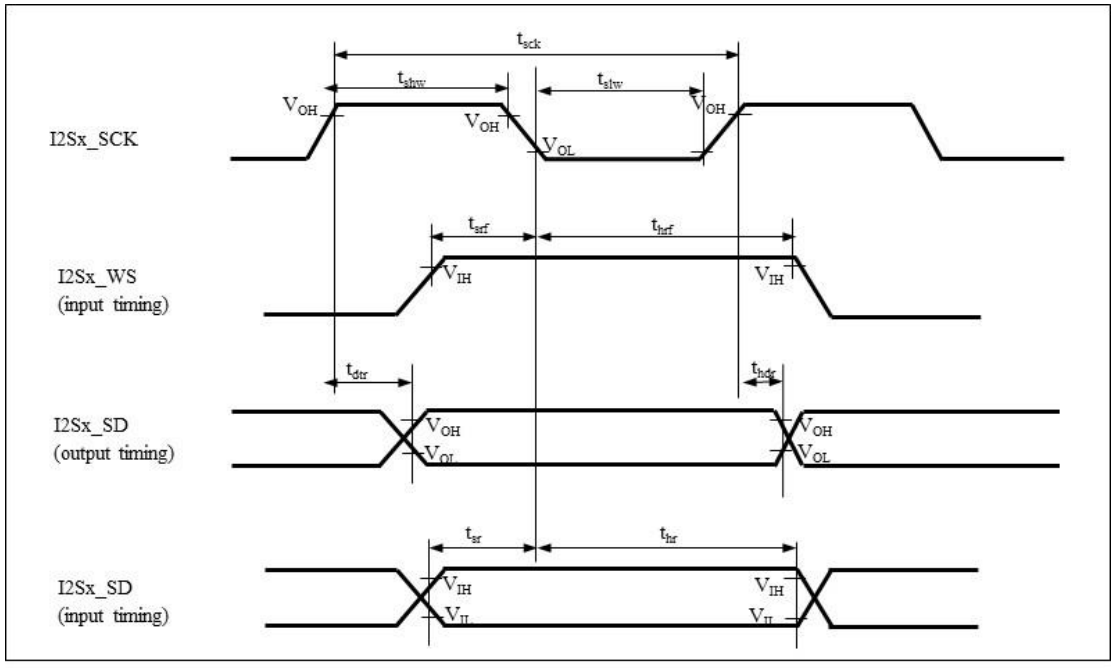
8.4.22.2 I2S Timing – Slave mode (MSMD=0)

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
I2S clock cycle (input SCK)	t_{sck}	I2S0_SCK, I2S1_SCK	(CL = 20 pF, I_{OL}=-5 mA, I_{OH}=5 mA) CPOL=0, SMPL=0	66.66	-	ns	
I2S clock “H” pulse width	t_{shw}	I2S0_SCK, I2S1_SCK		0.40* t_{sck}	0.60* t_{sck}	ns	
I2S clock “L” pulse width	t_{slw}			0.40* t_{sck}	0.60* t_{sck}	ns	
Setup time WS transition -> SCK↓	t_{srf}	I2S0_SCK, I2S1_SCK, I2S0_WS, I2S1_WS		40	-	ns	*1
Hold time SCK↓ -> WS transition	t_{hrf}			10	-	ns	*1
Sender delay time SCK↑ -> SD valid	t_{dtr}	I2S0_SCK, I2S1_SCK, I2S0_SD, I2S1_SD		-	26	ns	*1
Sender hold time SCK↑ -> SD invalid	t_{htr}			-10	-	ns	*1
Receiver setup time SD valid -> SCK↓	t_{sr}	I2S0_SCK, I2S1_SCK, I2S0_SD, I2S1_SD		21	-	ns	*1
Receiver hold time SCK↓ -> SD valid	t_{hr}			10	-	ns	*1

Note:

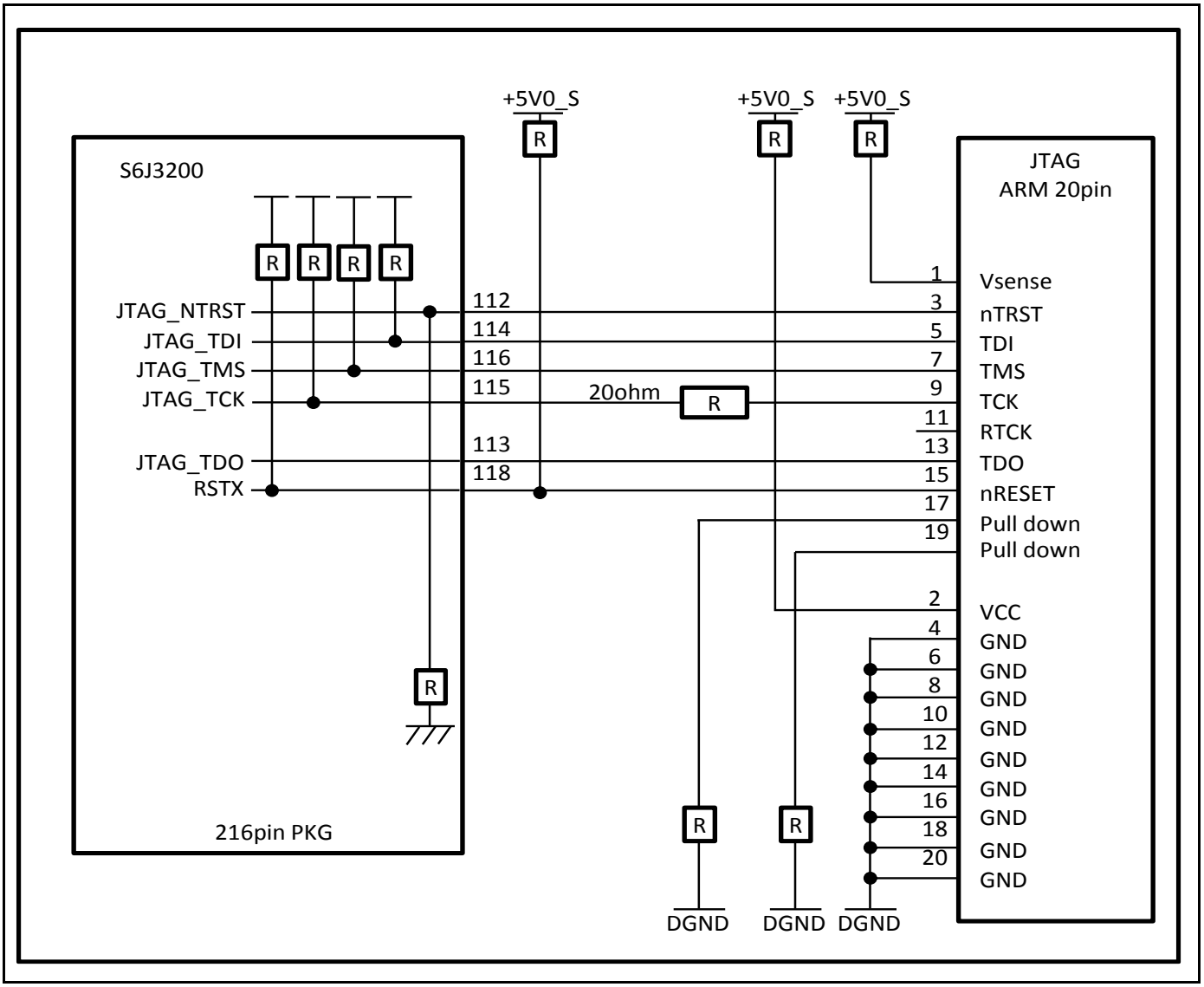
*1: Refer to the I2S register description chapter in the TRM for different combinations of clock polarity (CPOL), sampling point position (SMPL), polarity/pulse_width/frame_sync phase of WS (FSPL, FSLN, FSPH). Actual waveforms and relevant clock edges will change accordingly; the delay valuesbased on the table above will remain the same.



11. Appendix

11.1 Application 1: JTAG tool Connection

This is an application example of JTAG tool connection. See the relevant application note 002-09861 in detail.



Revision	ECN	Orig. of Change	Submission Date	Description of Change
				[Limitation] Add note that this LVDL2 cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage with any setting [Limitation] Add note that this LVDH2 cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage for some of the settings
				8. Electric Characteristics 8.4.10.3 LVDL1 [Improve] Deleted the useless configuration of LVDL1. (LVDL1V=01)
				8.Electric Characteristics 8.4.10.6 LVDH2 [Improve] Typ value of release voltage at conditions of LVDH2V=0001 changes 2.75V to 2.85V.
				8. Electric Characteristics 8.4.11 High Current Output Slew Rate [Improve] Corrected the typo in figure. (VOL8, VOH8 -> VOL, VOH)
				8. Electric Characteristics 8.4.12.2 Display Controller0 Timing (RSDS) [Improve] Delete unnecessary characteristics
				8. Electric Characteristics 8.4.14 FPD-link [Improve] Corrected unit. "Ohm" -> "ohm" [Improve] Corrected remarks on "Common mode voltage". "One of three" -> "One of two" [Improve] Added missing information. "5 pF (differential)" [Improve] Corrected format. "25MHz" -> "25 MHz", "4/7" -> "4 / 7". [Improve] Added cycle to cycle jitter spec. [Improve] Added information. "Equals 1/f" into TCIP. [Improve] Corrected max time in "Cycle time of TXCLKP/M". [Improve] Added other frequency spec into "Output pulse position". [Limitation] Added PLL lock-up time. [Improve] Separately added specs for revision H.
				8. Electric Characteristics 8.4.14. FPD-Link (LVDS) [Limitation] Specified minimum output frequency 5MHz.
				8. Electric Characteristics 8.4.16 HyperBus [Enhance] Enhanced AC spec Hyper Bus read timing and corrected timing chart
				8. Electric Characteristics 8.4.16 HyperBus [Enhance] The series of port reference voltage level VIL/VIH/VOL/VOH for HyperBus AC specification is defined.
				8. Electric Characteristics 8.4.16 HyperBus [Improve] Added a note for clarifying the HyperBus clock cycle and source.
				8. Electric Characteristics 8.4.16 HyperBus [Improve] Corrected the revision digit information.
				8. Electric Characteristics 8.4.19 Port Noise Filter [Improve] Change the description of filter specification and note for GPIO [Improve] Added the filter specification for EINT, TIN [Improve] Added the filter specification for SCL, SDA of I2C
				9. Abbreviation