**Welcome to E-XFL.COM**

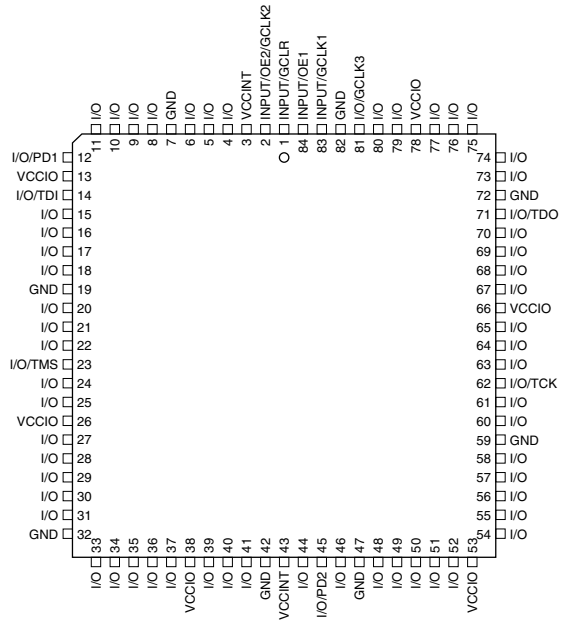
## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

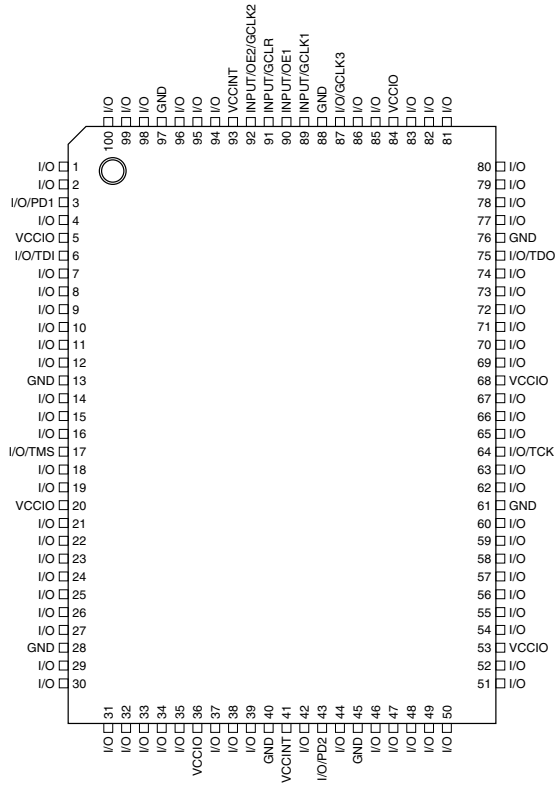
## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Active |
| Programmable Type | In System Programmable (min 10K program/erase cycles) |
| Delay Time tpd(1) Max | 15 ns |
| Voltage Supply - Internal | 3V ~ 3.6V |
| Number of Logic Elements/Blocks | - |
| Number of Macrocells | 128 |
| Number of Gates | - |
| Number of I/O | 64 |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 84-LCC (J-Lead) |
| Supplier Device Package | 84-PLCC (29.31x29.31) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atf1508asv-15ju84 |

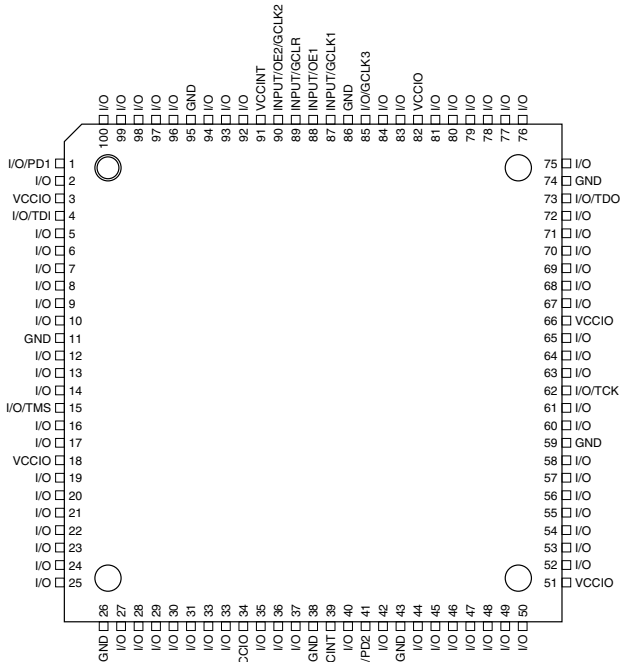
84-lead PLCC
Top View



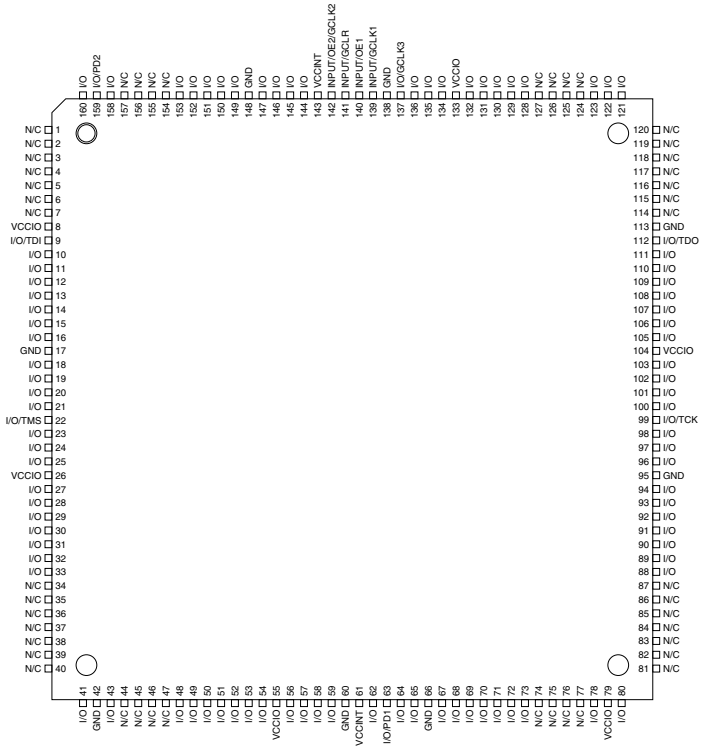

100-lead PQFP
Top View



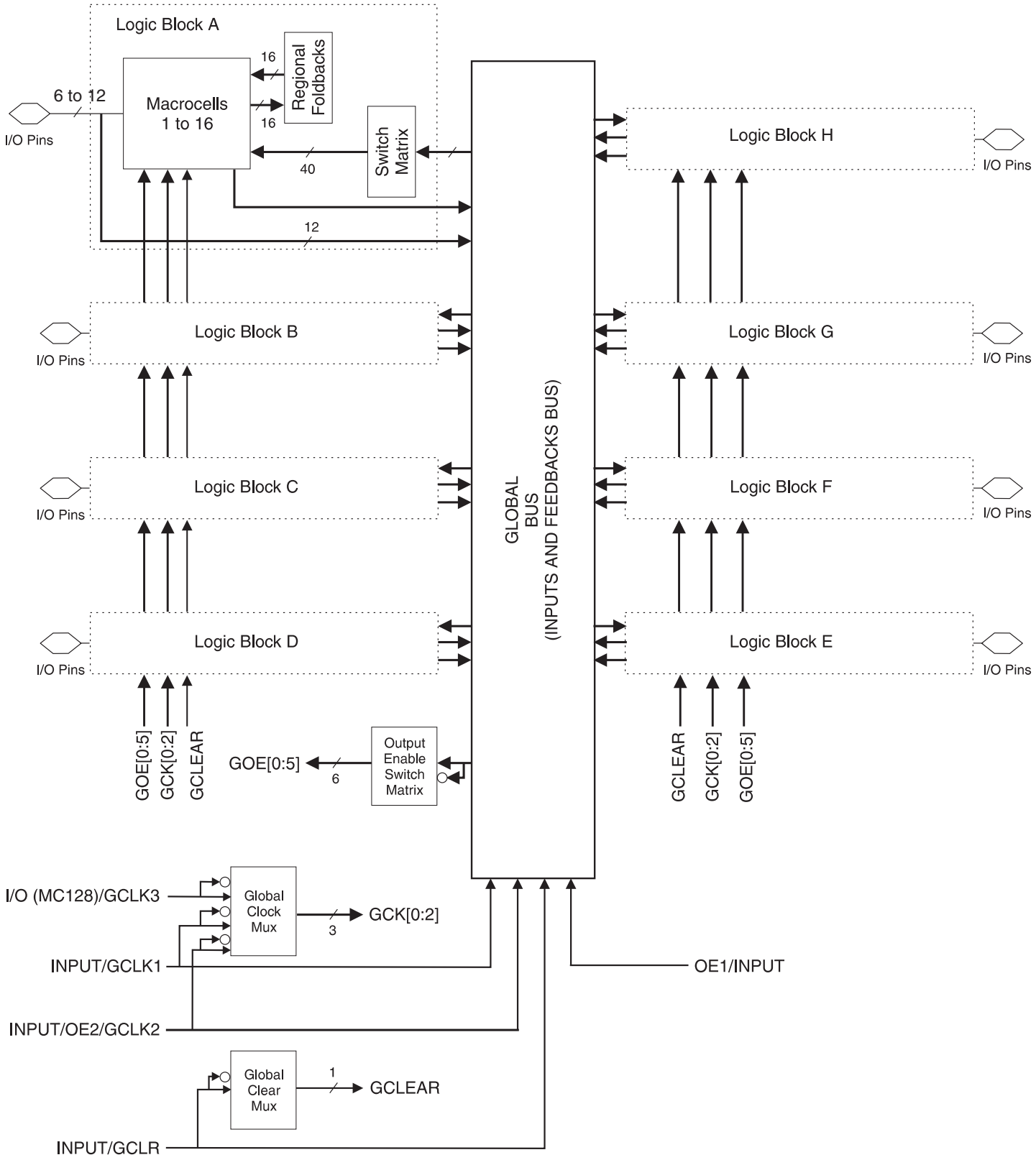

100-lead TQFP
Top View




160-lead PQFP
Top View



## Block Diagram



## Description

The ATF1508ASV(L) is a high-performance, high-density complex programmable logic device (CPLD) that utilizes Atmel's proven electrically-erasable technology. With 128 logic macrocells and up to 100 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI and classic PLDs. The ATF1508ASV(L)'s enhanced routing switch matrices increase usable gate count and increase odds of successful pin-locked design modifications.

The ATF1508ASV(L) has up to 96 bi-directional I/O pins and four dedicated input pins, depending on the type of device package selected. Each dedicated pin can also serve as a global control signal, register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

Each of the 128 macrocells generates a buried feedback that goes to the global bus. Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term that goes to a regional bus. Cascade logic between macrocells in the ATF1508ASV(L) allows fast, efficient generation of complex logic functions. The ATF1508ASV(L) contains eight such logic chains, each capable of creating sum term logic with a fan-in of up to 40 product terms.

The ATF1508ASV(L) macrocell, shown in Figure 1, is flexible enough to support highly-complex logic functions operating at high-speed. The macrocell consists of five sections: product terms and product term select multiplexer, OR/XOR/CASCADE logic, a flip-flop, output select and enable, and logic array inputs.

Unused macrocells are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents of the ATF1508ASV(L). Two bytes (16 bits) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

The ATF1508ASV(L) device is an in-system programmable (ISP) device. It uses the industry-standard 4-pin JTAG interface (IEEE Std. 1149.1), and is fully-compliant with JTAG's Boundary-scan Description Language (BSDL). ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

### Product Terms and Select Mux

Each ATF1508ASV(L) macrocell has five product terms. Each product term receives as its inputs all signals from both the global bus and regional bus.

The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the design compiler, which selects the optimum macrocell configuration.

### OR/XOR/CASCADE Logic

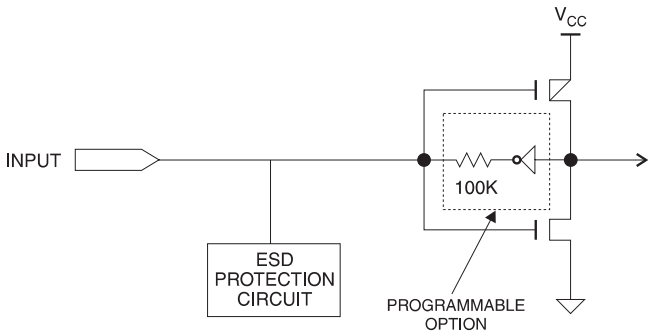
The ATF1508ASV(L)'s logic structure is designed to efficiently support all types of logic. Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5-input AND/OR sum term. With the addition of the CASIN from neighboring macrocells, this can be expanded to as many as 40 product terms with little additional delay.

The macrocell's XOR gate allows efficient implementation of compare and arithmetic functions. One input to the XOR comes from the OR sum term. The other XOR input can be a product term or a fixed high- or low-level. For combinatorial outputs, the fixed level input allows polarity selection. For registered functions, the fixed levels allow DeMorgan minimization of product terms. The XOR gate is also used to emulate T- and JK-type flip-flops.

## Programmable Pin-keeper Option for Inputs and I/Os

The ATF1508ASV(L) offers the option of programming all input and I/O pins so that "pin-keeper" circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high- or low-level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

### Input Diagram

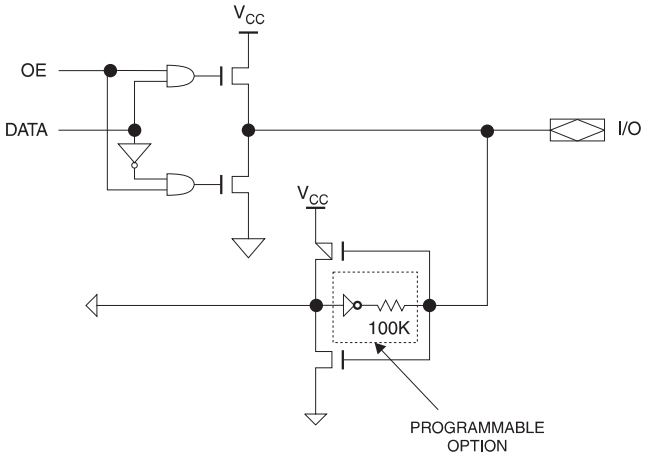



## Speed/Power Management

The ATF1508ASV(L) has several built-in speed and power management features. The ATF1508ASV(L) contains circuitry that automatically puts the device into a low-power standby mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides proportional power-savings for most applications running at system speeds below 5 MHz.

To further reduce power, each ATF1508ASV(L) macrocell has a reduced-power bit feature. This feature allows individual macrocells to be configured for maximum power-savings. This feature may be selected as a design option.

### I/O Diagram



## DC and AC Operating Conditions

| | Commercial | Industrial |
|---|---|---|
| Operating Temperature (Ambient) | 0°C - 70°C | -40°C - 85°C |
| $V_{CC}$ (3.3V) Power Supply | 3.0V - 3.6V | 3.0V - 3.6V |

## DC Characteristics

| Symbol | Parameter | Condition | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $I_{IL}$ | Input or I/O Low Leakage Current | $V_{IN} = V_{CC}$ | | | | -2 | -10 | µA |
| $I_{IH}$ | Input or I/O High Leakage Current | | | | | 2 | 10 | µA |
| $I_{OZ}$ | Tri-State Output Off-State Current | $V_O = V_{CC}$ or GND | | | -40 | | 40 | µA |
| $I_{CC1}$ | Power Supply Current, Standby | $V_{CC}$ = Max $V_{IN}$ = 0, $V_{CC}$ | Std Mode | Com. | | 115 | | mA |
| | | | | Ind. | | 135 | | mA |
| | | | "L" Mode | Com. | | 5 | | µA |
| | | | | Ind. | | 5 | | µA |
| $I_{CC2}$ | Power Supply Current, Power-down Mode | $V_{CC}$ = Max $V_{IN}$ = 0, $V_{CC}$ | "PD" Mode | | | 0.1 | 5 | mA |
| $I_{CC3}$ (2) | Reduced-power Mode Supply Current, Standby | $V_{CC}$ = Max $V_{IN}$ = 0, $V_{CC}$ | Std Mode | Com. | | 60 | | mA |
| | | | | Ind. | | 80 | | mA |
| $V_{IL}$ | Input Low Voltage | | | | -0.3 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | | | 1.7 | | $V_{CCIO}$ + 0.3 | V |
| $V_{OL}$ | Output Low Voltage (TTL) | $V_{IN} = V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min, $I_{OL}$ = 8 mA | | Com. | | | 0.45 | V |
| | | | | Ind. | | | 0.45 | V |
| | Output Low Voltage (CMOS) | $V_{IN} = V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min, $I_{OL}$ = 0.1 mA | | Com. | | | 0.2 | V |
| | | | | Ind. | | | 0.2 | V |
| $V_{OH}$ | Output High Voltage – 3.3V (TTL) | $V_{IN} = V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min, $I_{OH}$ = -2.0 mA | | | 2.4 | | | V |
| | Output High Voltage – 3.3V (CMOS) | $V_{IN} = V_{IH}$ or $V_{IL}$ $V_{CCIO}$ = Min, $I_{OH}$ = -0.1 mA | | | $V_{CCIO}$ - 0.2 | | | V |

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. $I_{CC3}$ refers to the current in the reduced-power mode when macrocell reduced-power is turned ON.

## Pin Capacitance

| | Typ | Max | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | | 8 | pF | $V_{IN}$ = 0V; f = 1.0 MHz |
| $C_{I/O}$ | | 8 | pF | $V_{OUT}$ = 0V; f = 1.0 MHz |

Note: Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested. The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12 pF.

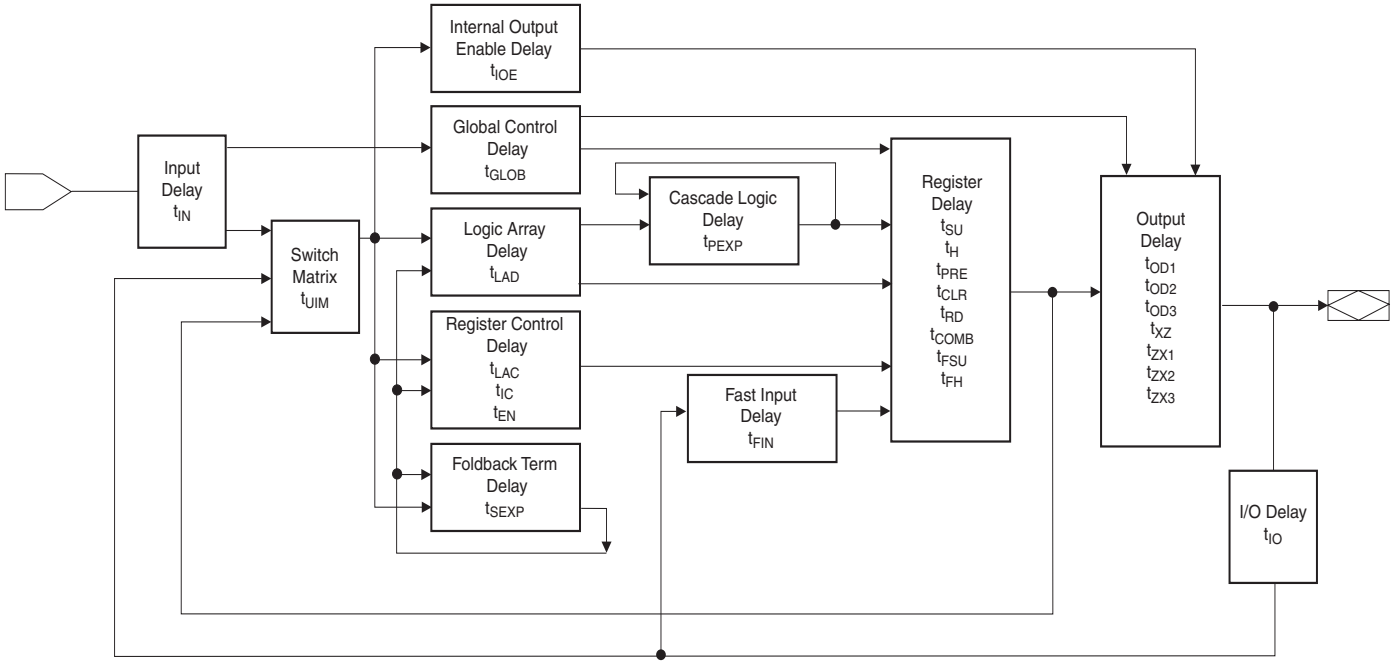
## Absolute Maximum Ratings*

| | |
|---|---|
| Temperature Under Bias | -40°C to +85°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -2.0V to +7.0V(1) |
| Voltage on Input Pins with Respect to Ground During Programming | -2.0V to +14.0V(1) |
| Programming Voltage with Respect to Ground | -2.0V to +14.0V(1) |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is $V_{CC}$ + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

## Timing Model

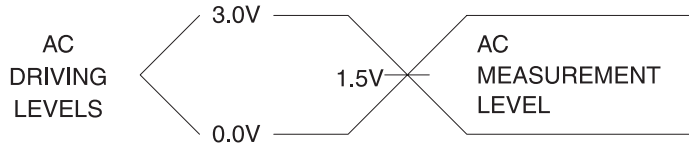


## AC Characteristics[1] (Continued)

| Symbol | Parameter | -15 | | -20 | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{ZX2}$ | Output Buffer Enable Delay (Slow slew rate = OFF; $V_{CCIO}$ = 3.3V; $C_L$ = 35 pF) | | 7 | | 9 | ns |
| $t_{ZX3}$ | Output Buffer Enable Delay (Slow slew rate = ON; $V_{CCIO}$ = 5.0V/3.3V; $C_L$ = 35 pF) | | 10 | | 11 | ns |
| $t_{XZ}$ | Output Buffer Disable Delay ($C_L$ = 5 pF) | | 6 | | 7 | ns |
| $t_{SU}$ | Register Setup Time | 5 | | 6 | | ns |
| $t_H$ | Register Hold Time | 4 | | 5 | | ns |
| $t_{FSU}$ | Register Setup Time of Fast Input | 2 | | 2 | | ns |
| $t_{FH}$ | Register Hold Time of Fast Input | 2 | | 2 | | ns |
| $t_{RD}$ | Register Delay | | 2 | | 2.5 | ns |
| $t_{COMB}$ | Combinatorial Delay | | 2 | | 3 | ns |
| $t_{IC}$ | Array Clock Delay | | 6 | | 7 | ns |
| $t_{EN}$ | Register Enable Time | | 6 | | 7 | ns |
| $t_{GLOB}$ | Global Control Delay | | 2 | | 3 | ns |
| $t_{PRE}$ | Register Preset Time | | 4 | | 5 | ns |
| $t_{CLR}$ | Register Clear Time | | 4 | | 5 | ns |
| $t_{UIM}$ | Switch Matrix Delay | | 2 | | 2.5 | ns |
| $t_{RPA}$ | Reduced-Power Adder[2] | | 10 | | 13 | ns |

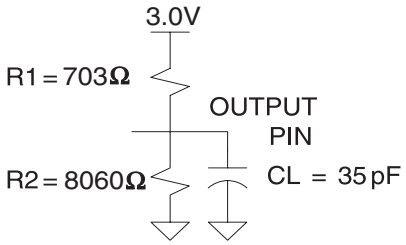
Notes: 1. See ordering information for valid part numbers.
2. The $t_{RPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$,$t_{TIC}$, $t_{ACL}$, and $t_{SEXP}$ parameters for macrocells running in the reduced-power mode.

## Input Test Waveforms and Measurement Levels




$t_R$, $t_F$ = 1.5 ns typical

## Output AC Test Loads




## Power-down Mode

The ATF1508ASV(L) includes two pins for optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin. When the PD1 and PD2 pin is high, the device supply current is reduced to less than 5 mA. During power-down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a high-Z state at the onset will remain at high-Z. During power-down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. The power-down pin feature is enabled in the logic design file. Designs using either power-down pin may not use the PD pin logic array input. However, buried logic resources in this macrocell may still be used.

## Power Down AC Characteristics(1)(2)

| Symbol | Parameter | -15 | | -20 | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{IVDH}$ | Valid I, I/O before PD High | 15 | | 20 | | ns |
| $t_{GVDH}$ | Valid OE(2) before PD High | 15 | | 20 | | ns |
| $t_{CVDH}$ | Valid Clock(2) before PD High | 15 | | 20 | | ns |
| $t_{DHIX}$ | I, I/O Don't Care after PD High | | 25 | | 30 | ns |
| $t_{DHGX}$ | OE(2) Don't Care after PD High | | 25 | | 30 | ns |
| $t_{DHCX}$ | Clock(2) Don't Care after PD High | | 25 | | 30 | ns |
| $t_{DLIV}$ | PD Low to Valid I, I/O | | 1 | | 1 | µs |
| $t_{DLGV}$ | PD Low to Valid OE (Pin or Term) | | 1 | | 1 | µs |
| $t_{DLCV}$ | PD Low to Valid Clock (Pin or Term) | | 1 | | 1 | µs |
| $t_{DLOV}$ | PD Low to Valid Output | | 1 | | 1 | µs |

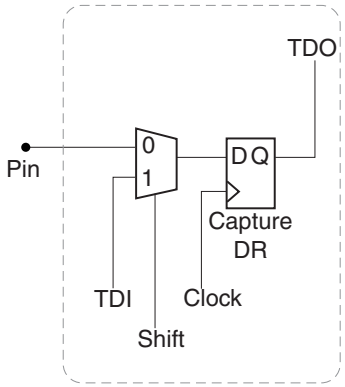
Notes: 1. For slow slew outputs, add $t_{SSO}$.
2. Pin or product term.

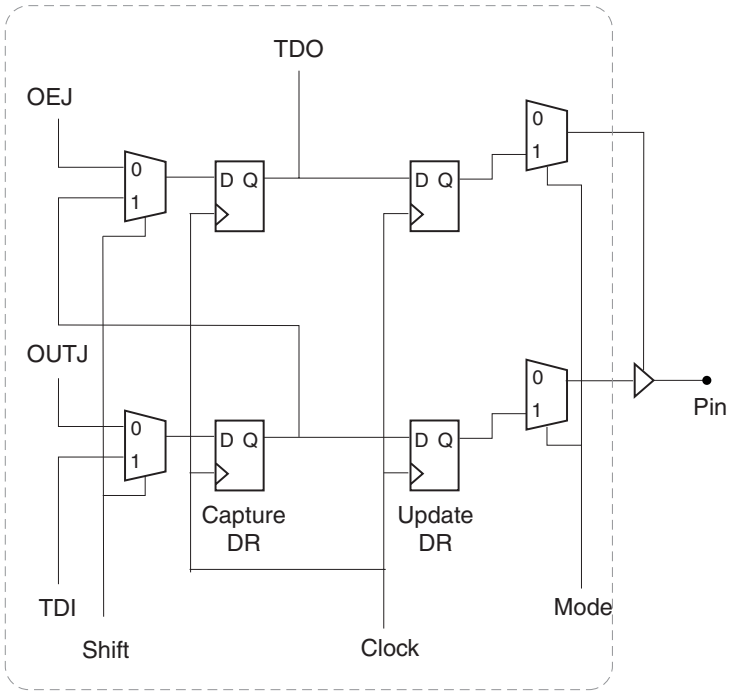
## Boundary-scan Definition Language (BSDL) Models for the ATF1508

These are now available in all package types via the Atmel web site. These models can be used for Boundary-scan Test Operation in the ATF1508ASV(L) and have been scheduled to conform to the IEEE 1149.1 standard.

## BSC Configuration for Macrocell

**Pin BSC**




**Macrocell BSC**

## ATF1508ASV(L) Dedicated Pinouts

| Dedicated Pin | 84-lead J-lead | 100-lead PQFP | 100-lead TQFP | 160-lead PQFP |
|---|---|---|---|---|
| INPUT/OE2/GCLK2 | 2 | 92 | 90 | 142 |
| INPUT/GCLR | 1 | 91 | 89 | 141 |
| INPUT/OE1 | 84 | 90 | 88 | 140 |
| INPUT/GCLK1 | 83 | 89 | 87 | 139 |
| I/O/GCLK3 | 81 | 87 | 85 | 137 |
| I/O/PD (1, 2) | 12,45 | 3,43 | 1,41 | 63,159 |
| I/O/TDI(JTAG) | 14 | 6 | 4 | 9 |
| I/O/TMS(JTAG) | 23 | 17 | 15 | 22 |
| I/O/TCK(JTAG) | 62 | 64 | 62 | 99 |
| I/O/TDO(JTAG) | 71 | 75 | 73 | 112 |
| GND | 7,19,32,42, 47,59,72,82 | 13,28,40,45, 61,76,88,97 | 11,26,38,43, 59,74,86,95 | 17,42,60,66,95, 113,138,148 |
| VCC | 3,13,26,38, 43,53,66,78 | 5,20,36,41, 53,68,84,93 | 3,18,34,39, 51,66,82,91 | 8,26,55,61,79,104,133,143 |
| N/C | - | - | - | 1,2,3,4,5,6,7,34,35,36, 37,38,39,40,44,45,46, 47,74,75,76,77,81,82, 83,84,85,86,87,114, 115,116,117,118,119, 120,124,125,126,127, 154,155,156,157 |
| # of SIGNAL PINS | 68 | 84 | 84 | 100 |
| # USER I/O PINS | 64 | 80 | 80 | 96 |

| | |
|---|---|
| OE (1, 2) | Global OE pins |
| GCLR | Global Clear pin |
| GCLK (1, 2, 3) | Global Clock pins |
| PD (1, 2) | Power-down pins |
| TDI, TMS, TCK, TDO | JTAG pins used for boundary-scan testing or in-system programming |
| GND | Ground pins |
| VCC | VCC pins for the device |

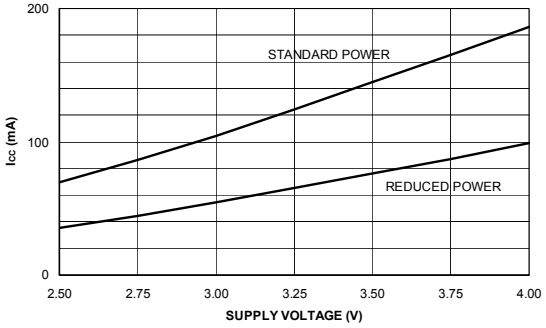
## ATF1508ASV(L) I/O Pinouts

| MC | PLB | 84-lead J-lead | 100-lead PQFP | 100-lead TQFP | 160-lead PQFP | MC | PLB | 84-lead J-lead | 100-lead PQFP | 100-lead TQFP | 160-lead PQFP |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | A | - | 4 | 2 | 160 | 33 | C | - | 27 | 25 | 41 |
| 2 | A | - | - | - | - | 34 | C | - | - | - | - |
| 3 | A/ **PD1** | 12 | 3 | 1 | 159 | 35 | C | 31 | 26 | 24 | 33 |
| 4 | A | - | - | - | 158 | 36 | C | - | - | - | 32 |
| 5 | A | 11 | 2 | 100 | 153 | 37 | C | 30 | 25 | 23 | 31 |
| 6 | A | 10 | 1 | 99 | 152 | 38 | C | 29 | 24 | 22 | 30 |
| 7 | A | - | - | - | - | 39 | C | - | - | - | - |
| 8 | A | 9 | 100 | 98 | 151 | 40 | C | 28 | 23 | 21 | 29 |
| 9 | A | - | 99 | 97 | 150 | 41 | C | - | 22 | 20 | 28 |
| 10 | A | - | - | - | - | 42 | C | - | - | - | - |
| 11 | A | 8 | 98 | 96 | 149 | 43 | C | 27 | 21 | 19 | 27 |
| 12 | A | - | - | - | 147 | 44 | C | - | - | - | 25 |
| 13 | A | 6 | 96 | 94 | 146 | 45 | C | 25 | 19 | 17 | 24 |
| 14 | A | 5 | 95 | 93 | 145 | 46 | C | 24 | 18 | 16 | 23 |
| 15 | A | - | - | - | - | 47 | C | - | - | - | - |
| 16 | A | 4 | 94 | 92 | 144 | 48 | C/ **TMS** | 23 | 17 | 15 | 22 |
| 17 | B | 22 | 16 | 14 | 21 | 49 | D | 41 | 39 | 37 | 59 |
| 18 | B | - | - | - | - | 50 | D | - | - | - | - |
| 19 | B | 21 | 15 | 13 | 20 | 51 | D | 40 | 38 | 36 | 58 |
| 20 | B | - | - | - | 19 | 52 | D | - | - | - | 57 |
| 21 | B | 20 | 14 | 12 | 18 | 53 | D | 39 | 37 | 35 | 56 |
| 22 | B | - | 12 | 10 | 16 | 54 | D | - | 35 | 33 | 54 |
| 23 | B | - | - | - | - | 55 | D | - | - | - | - |
| 24 | B | 18 | 11 | 9 | 15 | 56 | D | 37 | 34 | 32 | 53 |
| 25 | B | 17 | 10 | 8 | 14 | 57 | D | 36 | 33 | 31 | 52 |
| 26 | B | - | - | - | - | 58 | D | - | - | - | - |
| 27 | B | 16 | 9 | 7 | 13 | 59 | D | 35 | 32 | 30 | 51 |
| 28 | B | - | - | - | 12 | 60 | D | - | - | - | 50 |
| 29 | B | 15 | 8 | 6 | 11 | 61 | D | 34 | 31 | 29 | 49 |
| 30 | B | - | 7 | 5 | 10 | 62 | D | - | 30 | 28 | 48 |
| 31 | B | - | - | - | - | 63 | D | - | - | - | - |
| 32 | B/ **TDI** | 14 | 6 | 4 | 9 | 64 | D | 33 | 29 | 27 | 43 |
| 65 | E | 44 | 42 | 40 | 62 | 97 | G | 63 | 65 | 63 | 100 |
| 66 | E | - | - | - | - | 98 | G | - | - | - | - |

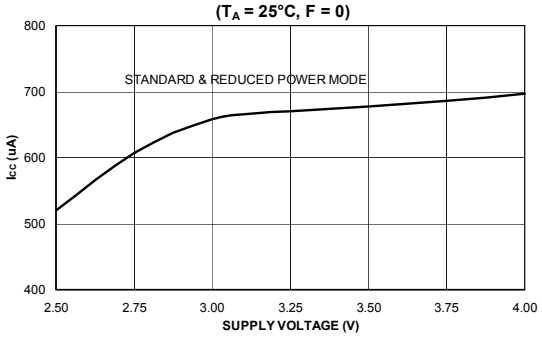
## ATF1508ASV(L) I/O Pinouts (Continued)

| MC | PLB | 84-lead J-lead | 100-lead PQFP | 100-lead TQFP | 160-lead PQFP | MC | PLB | 84-lead J-lead | 100-lead PQFP | 100-lead TQFP | 160-lead PQFP |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 67 | E/ **PD2** | 45 | 43 | 41 | 63 | 99 | G | 64 | 66 | 64 | 101 |
| 68 | E | - | - | - | 64 | 100 | G | - | - | - | 102 |
| 69 | E | 46 | 44 | 42 | 65 | 101 | G | 65 | 67 | 65 | 103 |
| 70 | E | - | 46 | 44 | 67 | 102 | G | - | 69 | 67 | 105 |
| 71 | E | - | - | - | - | 103 | G | - | - | - | - |
| 72 | E | 48 | 47 | 45 | 68 | 104 | G | 67 | 70 | 68 | 106 |
| 73 | E | 49 | 48 | 46 | 69 | 105 | G | 68 | 71 | 69 | 107 |
| 74 | E | - | - | - | - | 106 | G | - | - | - | - |
| 75 | E | 50 | 49 | 47 | 70 | 107 | G | 69 | 72 | 70 | 108 |
| 76 | E | - | - | - | 71 | 108 | G | - | - | - | 109 |
| 77 | E | 51 | 50 | 48 | 72 | 109 | G | 70 | 73 | 71 | 110 |
| 78 | E | - | 51 | 49 | 73 | 110 | G | - | 74 | 72 | 111 |
| 79 | E | - | - | - | - | 111 | G | - | - | - | - |
| 80 | E | 52 | 52 | 50 | 78 | 112 | G/ **TDO** | 71 | 75 | 73 | 112 |
| 81 | F | - | 54 | 52 | 80 | 113 | H | - | 77 | 75 | 121 |
| 82 | F | - | - | - | - | 114 | H | - | - | - | - |
| 83 | F | 54 | 55 | 53 | 88 | 115 | H | 73 | 78 | 76 | 122 |
| 84 | F | - | - | - | 89 | 116 | H | - | - | - | 123 |
| 85 | F | 55 | 56 | 54 | 90 | 117 | H | 74 | 79 | 77 | 128 |
| 86 | F | 56 | 57 | 55 | 91 | 118 | H | 75 | 80 | 78 | 129 |
| 87 | F | - | - | - | - | 119 | H | - | - | - | - |
| 88 | F | 57 | 58 | 56 | 92 | 120 | H | 76 | 81 | 79 | 130 |
| 89 | F | - | 59 | 57 | 93 | 121 | H | - | 82 | 80 | 131 |
| 90 | F | - | - | - | - | 122 | H | - | - | - | - |
| 91 | F | 58 | 60 | 58 | 94 | 123 | H | 77 | 83 | 81 | 132 |
| 92 | F | - | - | - | 96 | 124 | H | - | - | - | 134 |
| 93 | F | 60 | 62 | 60 | 97 | 125 | H | 79 | 85 | 83 | 135 |
| 94 | F | 61 | 63 | 61 | 98 | 126 | H | 80 | 86 | 84 | 136 |
| 95 | F | - | - | - | - | 127 | H | - | - | - | - |
| 96 | F/ **TCK** | 62 | 64 | 62 | 99 | 128 | H/ **GCLK3** | 81 | 87 | 85 | 137 |

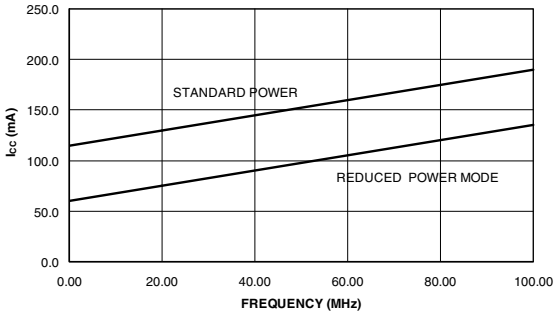
**SUPPLY CURRENT VS. SUPPLY VOLTAGE**
**($T_A$ = 25°C, F = 0)**



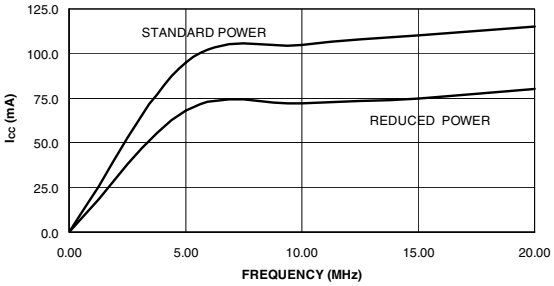

**SUPPLY CURRENT VS. SUPPLY VOLTAGE**
**PIN-CONTROLLED POWER-DOWN MODE**
**($T_A$ = 25°C, F = 0)**



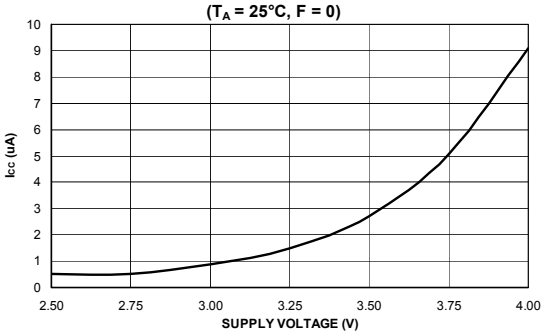

**SUPPLY CURRENT VS. FREQUENCY**
**STANDARD POWER ($T_A$ = 25°C)**




**SUPPLY CURRENT VS. FREQUENCY**
**LOW-POWER ("L") VERSION**
**($T_A$ = 25°C)**




**SUPPLY CURRENT VS. SUPPLY VOLTAGE**
**LOW POWER ("L") MODE**
**($T_A$ = 25°C, F = 0)**



# Ordering Information

## ATF1508ASV(L) Standard Package Options

| $t_{PD}$ (ns) | $t_{CO1}$ (ns) | $f_{MAX}$ (MHz) | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| 15 | 8 | 100 | ATF1508ASV-15 JC84 | 84J | Commercial (0°C to 70°C) |
| | | | ATF1508ASV-15 QC100 | 100Q1 | |
| | | | ATF1508ASV-15 AC100 | 100A | |
| | | | ATF1508ASV-15 QC160 | 160Q | |
| | 8 | 100 | ATF1508ASV-15 JI84 | 84J | Industrial (-40°C to +85°C) |
| | | | ATF1508ASV-15 QI100 | 100Q1 | |
| | | | ATF1508ASV-15 AI100 | 100A | |
| | | | ATF1508ASV-15 QI160 | 160Q | |
| 20 | 12 | 83.3 | ATF1508ASVL-20 JC84 | 84J | Commercial (0°C to 70°C) |
| | | | ATF1508ASVL-20 QC100 | 100Q1 | |
| | | | ATF1508ASVL-20 AC100 | 100A | |
| | | | ATF1508ASVL-20 QC160 | 160Q | |
| | 12 | 83.3 | ATF1508ASVL-20 JI84 | 84J | Industrial (-40°C to +85°C) |
| | | | ATF1508ASVL-20 QI100 | 100Q1 | |
| | | | ATF1508ASVL-20 AI100 | 100A | |
| | | | ATF1508ASVL-20 QI160 | 160Q | |

Note: 1. The last time buy is Sept. 30, 2005 for shaded parts.

## Using “C” Product for Industrial

There is very little risk in using “C” devices for industrial applications because the $V_{CC}$ conditions for 3.3V products are the same for commercial and industrial (there is only 15°C difference at the high end of the temperature range). To use commercial product for industrial temperature ranges, de-rate $I_{CC}$ by 15%.

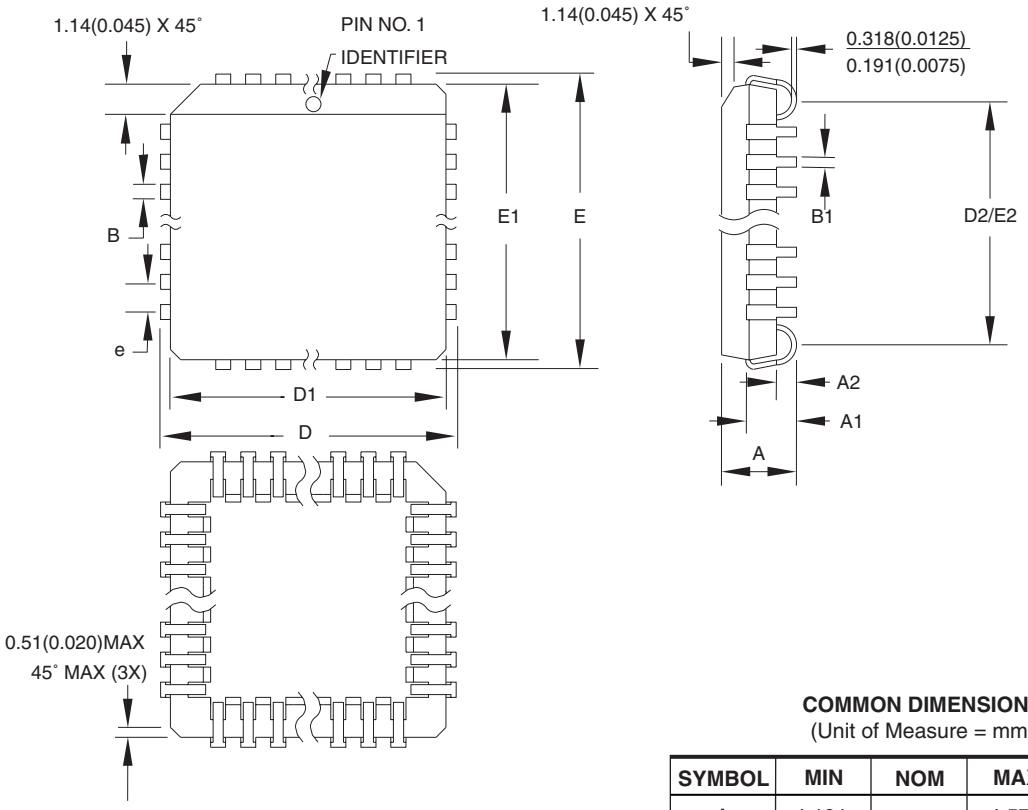
## ATF1508ASV(L) Green Package Options (Pb/Halide-free/RoHS Compliant)

| $t_{PD}$ (ns) | $t_{CO1}$ (ns) | $f_{MAX}$ (MHz) | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| 15 | 8 | 100 | ATF1508ASV-15 JU84 | 84J | Industrial (-40°C to +85°C) |
| | | | ATF1508ASV-15 AU100 | 100A | |
| 20 | 12 | 83.3 | ATF1508ASVL-20 JU84 | 84J | Industrial (-40°C to +85°C) |
| | | | ATF1508ASVL-20 AU100 | 100A | |

| Package Type | |
|---|---|
| **84J** | 84-lead, Plastic J-leaded Chip Carrier (PLCC) |
| **100Q1** | 100-lead, Plastic Quad Pin Flat Package (PQFP) |
| **100A** | 100-lead, Very Thin Plastic Gull Wing Quad Flat Package (TQFP) |
| **160Q** | 160-lead, Plastic Quad Pin Flat Package (PQFP) |

## Packaging Information

### 84J – PLCC




**COMMON DIMENSIONS**
(Unit of Measure = mm)

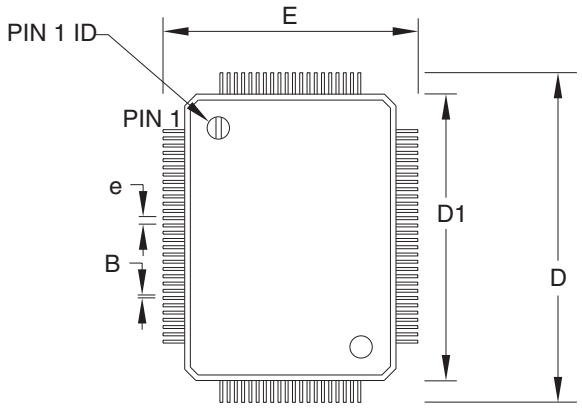
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 4.191 | – | 4.572 | |
| A1 | 2.286 | – | 3.048 | |
| A2 | 0.508 | – | – | |
| D | 30.099 | – | 30.353 | |
| D1 | 29.210 | – | 29.413 | Note 2 |
| E | 30.099 | – | 30.353 | |
| E1 | 29.210 | – | 29.413 | Note 2 |
| D2/E2 | 27.686 | – | 28.702 | |
| B | 0.660 | – | 0.813 | |
| B1 | 0.330 | – | 0.533 | |
| e | 1.270 TYP | | | |

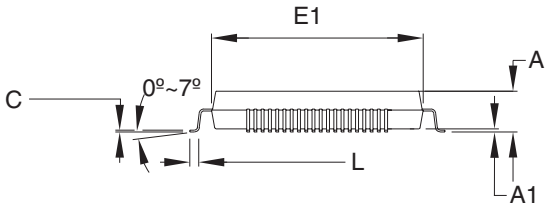
Notes:
1. This package conforms to JEDEC reference MS-018, Variation AF.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **84J**, 84-lead, Plastic J-leaded Chip Carrier (PLCC) | 84J | B |

## 100Q1 – PQFP



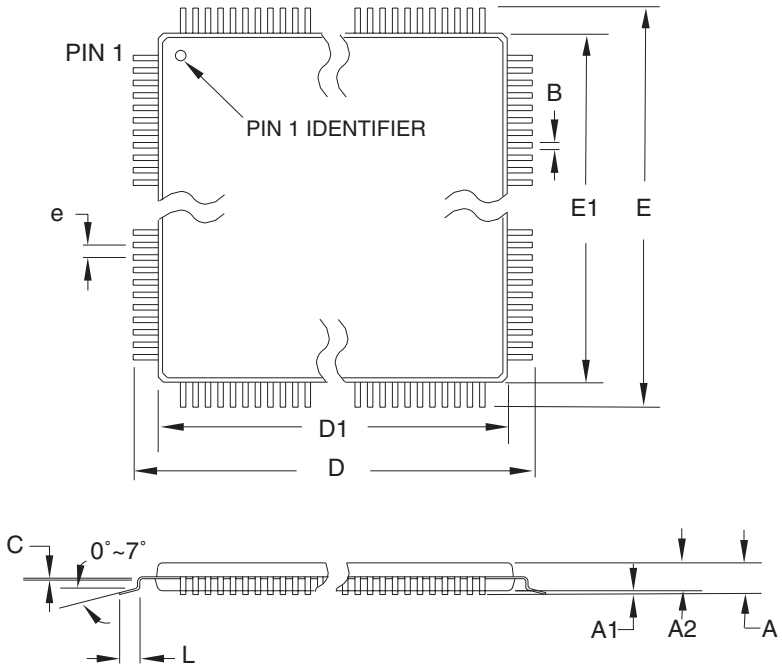

**COMMON DIMENSIONS**
(Unit of Measure = mm)
JEDEC STANDARD MS-022, GC-1

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | 3.04 | 3.4 | |
| A1 | 0.25 | 0.33 | 0.5 | |
| D | | 23.20 BSC | | |
| E | | 17.20 BSC | | |
| E1 | | 14.00 BSC | | |
| B | 0.22 | – | 0.40 | |
| C | 0.11 | – | 0.23 | |
| D1 | | 20 BSC | | |
| L | 0.73 | – | 1.03 | |
| e | | 0.65 BSC | | |

07/6/2005

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **100Q1**, 100-lead, 14 x 20 mm Body, 3.2 mm Footprint, 0.65 mm Pitch, Plastic Quad Flat Package (PQFP) | 100Q1 | C |

## 100A – TQFP




**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 15.75 | 16.00 | 16.25 | |
| D1 | 13.90 | 14.00 | 14.10 | Note 2 |
| E | 15.75 | 16.00 | 16.25 | |
| E1 | 13.90 | 14.00 | 14.10 | Note 2 |
| B | 0.17 | – | 0.27 | |
| C | 0.09 | – | 0.20 | |
| L | 0.45 | – | 0.75 | |
| e | 0.50 TYP | | | |

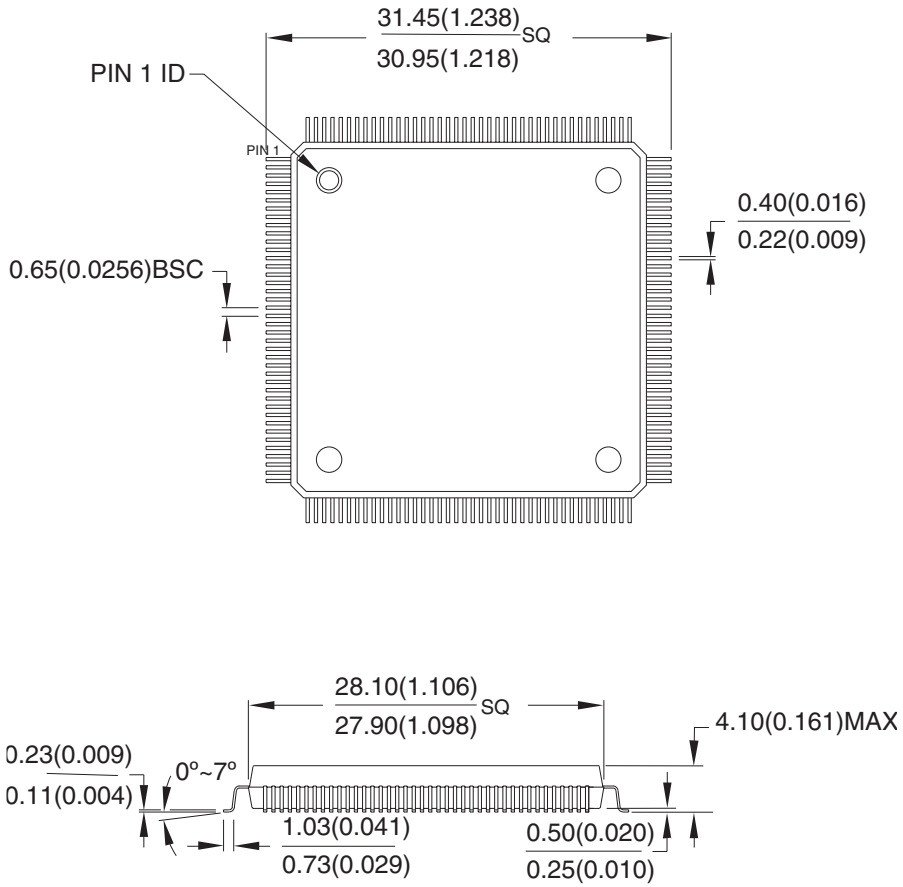
Notes:
1. This package conforms to JEDEC reference MS-026, Variation AED.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.08 mm maximum.

10/5/2001

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **100A,** 100-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.5 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP) | 100A | C |

## 160Q – PQFP

Dimensions in Millimeters and (Inches).
Controlling dimension: Millimeters.
JEDEC Standard MS-022 DC-1




10/23/03

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **160Q**, 160-lead, 28 x 28 mm Body, 3.2 mm Footprint,<br>0.65 mm Pitch, Plastic Quad Flat Package (PQFP) | 160Q | B |

## Revision History

| Revision | Comments |
|---|---|
| 1408H | Corrected list of last buy parts. |
| 1408G | Green package options added. |

## Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

## Regional Headquarters

*Europe*

Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

*Asia*

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

*Japan*

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

## Atmel Operations

*Memory*

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

*Microcontrollers*

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

*ASIC/ASSP/Smart Cards*

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

*RF/Automotive*

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

*Biometrics/Imaging/Hi-Rel MPU/*
*High Speed Converters/RF Datacom*

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

---

*Literature Requests*
www.atmel.com/literature

**Disclaimer:** The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. **EXCEPT AS SET FORTH IN ATMEL'S TERMS AND CONDITIONS OF SALE LOCATED ON ATMEL'S WEB SITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.** Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and product descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel's products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

**© Atmel Corporation 2005**. **All rights reserved.** Atmel®, logo and combinations thereof, Everywhere You Are® and others, are registered trademarks or trademarks of Atmel Corporation or its subsidiaries. Other terms and product names may be trademarks of others.

Printed on recycled paper.

1408H–PLD–7/05 xM