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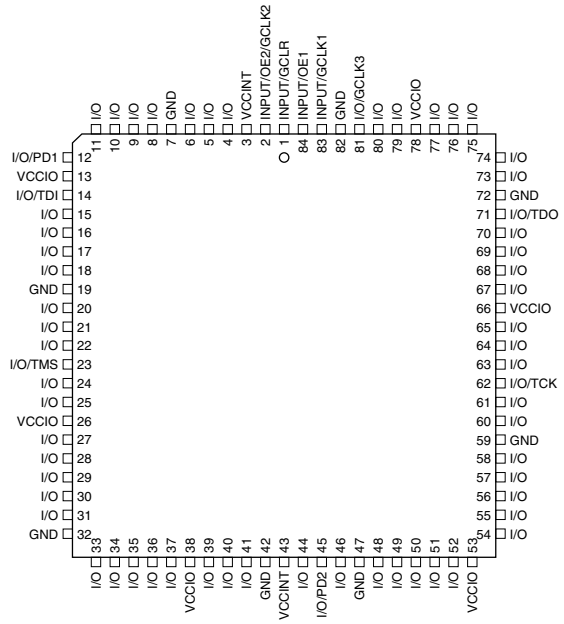
Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

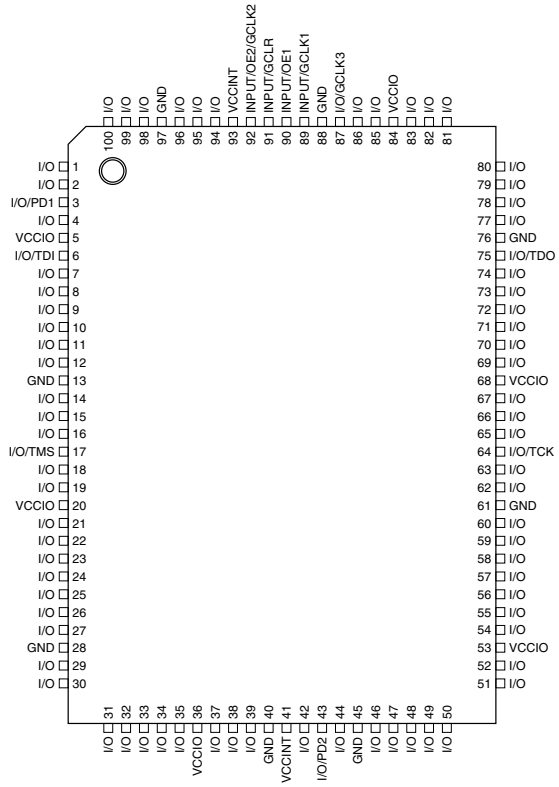
Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	20 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	80
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atf1508asvl-20ai100

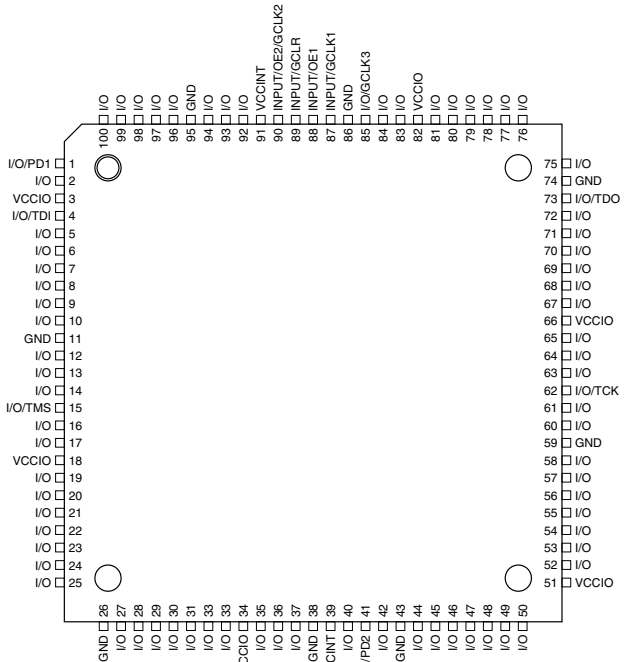
84-lead PLCC
Top View



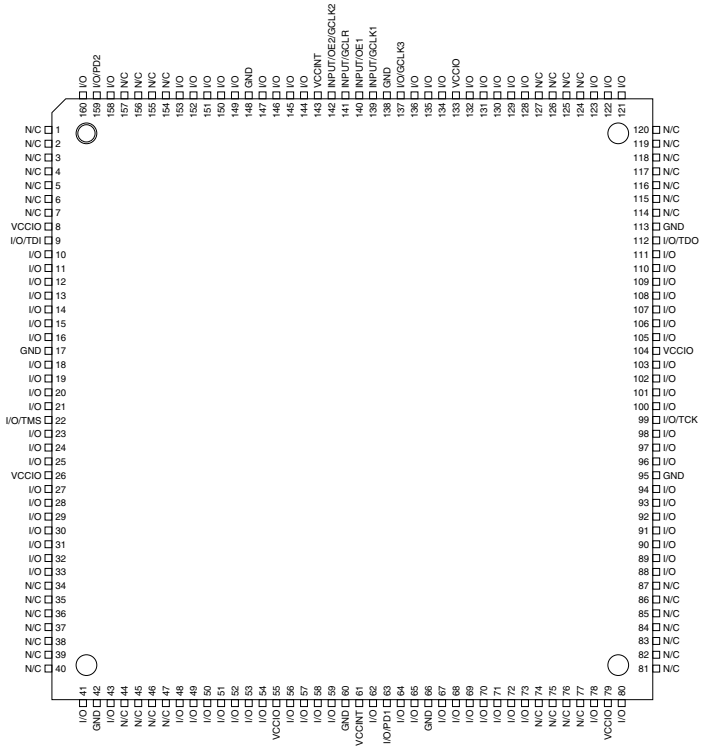
100-lead PQFP
Top View



100-lead TQFP
Top View



160-lead PQFP
Top View



Description

The ATF1508ASV(L) is a high-performance, high-density complex programmable logic device (CPLD) that utilizes Atmel's proven electrically-erasable technology. With 128 logic macrocells and up to 100 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI and classic PLDs. The ATF1508ASV(L)'s enhanced routing switch matrices increase usable gate count and increase odds of successful pin-locked design modifications.

The ATF1508ASV(L) has up to 96 bi-directional I/O pins and four dedicated input pins, depending on the type of device package selected. Each dedicated pin can also serve as a global control signal, register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

Each of the 128 macrocells generates a buried feedback that goes to the global bus. Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term that goes to a regional bus. Cascade logic between macrocells in the ATF1508ASV(L) allows fast, efficient generation of complex logic functions. The ATF1508ASV(L) contains eight such logic chains, each capable of creating sum term logic with a fan-in of up to 40 product terms.

The ATF1508ASV(L) macrocell, shown in Figure 1, is flexible enough to support highly-complex logic functions operating at high-speed. The macrocell consists of five sections: product terms and product term select multiplexer, OR/XOR/CASCADE logic, a flip-flop, output select and enable, and logic array inputs.

Unused macrocells are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents of the ATF1508ASV(L). Two bytes (16 bits) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

The ATF1508ASV(L) device is an in-system programmable (ISP) device. It uses the industry-standard 4-pin JTAG interface (IEEE Std. 1149.1), and is fully-compliant with JTAG's Boundary-scan Description Language (BSDL). ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

Product Terms and Select Mux

Each ATF1508ASV(L) macrocell has five product terms. Each product term receives as its inputs all signals from both the global bus and regional bus.

The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the design compiler, which selects the optimum macrocell configuration.

OR/XOR/CASCADE Logic

The ATF1508ASV(L)'s logic structure is designed to efficiently support all types of logic. Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5-input AND/OR sum term. With the addition of the CASIN from neighboring macrocells, this can be expanded to as many as 40 product terms with little additional delay.

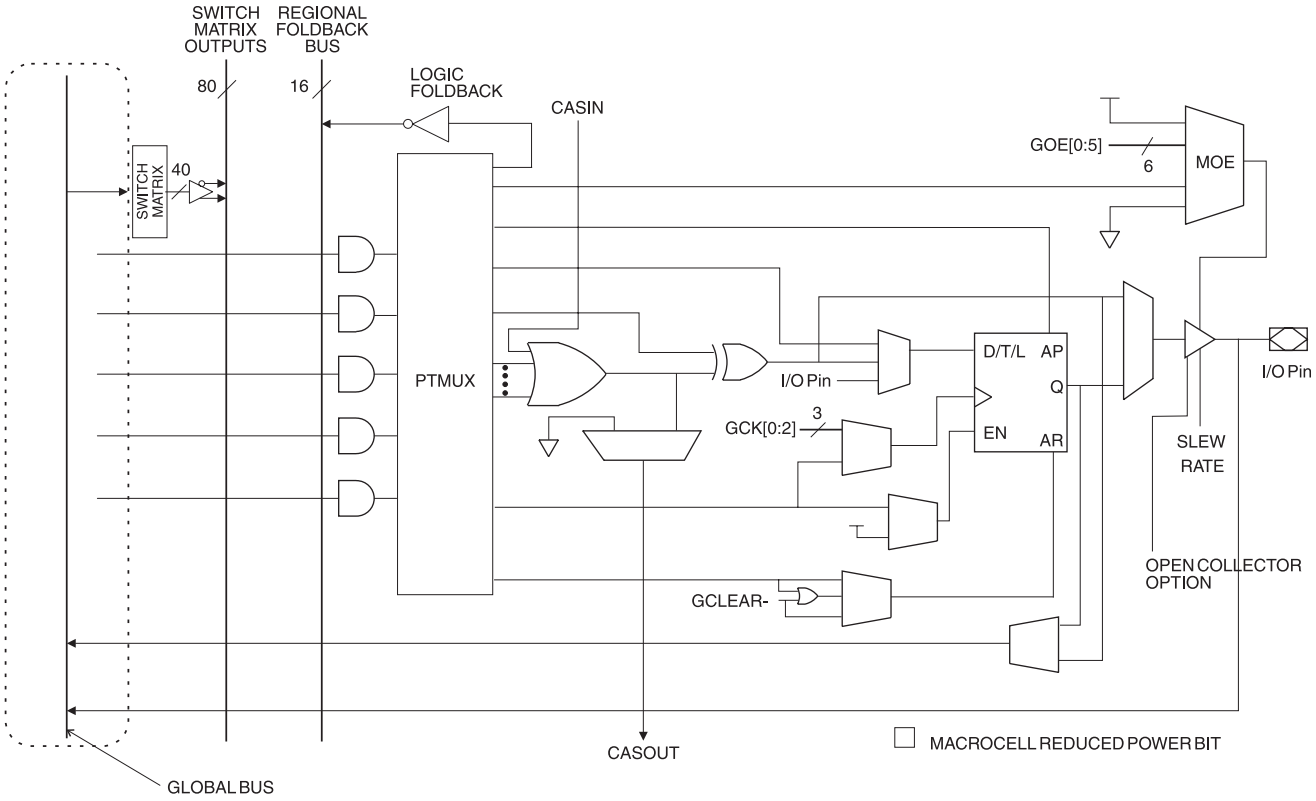
The macrocell's XOR gate allows efficient implementation of compare and arithmetic functions. One input to the XOR comes from the OR sum term. The other XOR input can be a product term or a fixed high- or low-level. For combinatorial outputs, the fixed level input allows polarity selection. For registered functions, the fixed levels allow DeMorgan minimization of product terms. The XOR gate is also used to emulate T- and JK-type flip-flops.

Flip-flop

The ATF1508ASV(L)'s flip-flop has very flexible data and control functions. The data input can come from either the XOR gate, from a separate product term or directly from the I/O pin. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell. (This feature is automatically implemented by the fitter software). In addition to D, T, JK and SR operation, the flip-flop can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

The clock itself can either be the Global CLK Signal (GCK) or an individual product term. The flip-flop changes state on the clock's rising edge. When the GCK signal is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored. The flip-flop's asynchronous reset signal (AR) can be either the Global Clear (GCLEAR), a product term, or always off. AR can also be a logic OR of GCLEAR with a product term. The asynchronous preset (AP) can be a product term or always off.

Figure 1. ATF1508ASV(L) Macrocell



Extra Feedback

The ATF15xxSE Family macrocell output can be selected as registered or combinatorial. The extra buried feedback signal can be either combinatorial or a registered signal regardless of whether the output is combinatorial or registered. (This enhancement function is automatically implemented by the fitter software.) Feedback of a buried combinatorial output allows the creation of a second latch within a macrocell.

I/O Control

The output enable multiplexer (MOE) controls the output enable signal. Each I/O can be individually configured as an input, output or for bi-directional operation. The output enable for each macrocell can be selected from the true or compliment of the two output enable pins, a subset of the I/O pins, or a subset of the I/O macrocells. This selection is automatically done by the fitter software when the I/O is configured as an input, all macrocell resources are still available, including the buried feedback, expander and cascade logic.

Global Bus/Switch Matrix

The global bus contains all input and I/O pin signals as well as the buried feedback signal from all 128 macrocells. The switch matrix in each logic block receives as its inputs all signals from the global bus. Under software control, up to 40 of these signals can be selected as inputs to the logic block.

Foldback Bus

Each macrocell also generates a foldback product term. This signal goes to the regional bus and is available to 16 macrocells. The foldback is an inverse polarity of one of the macrocell's product terms. The 16 foldback terms in each region allow generation of high fan-in sum terms (up to 21 product terms) with little additional delay.

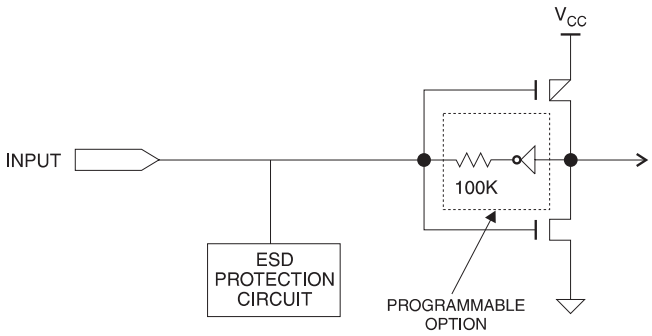
Open-collector Output Option

This option enables the device output to provide control signals such as an interrupt that can be asserted by any of the several devices.

Programmable Pin-keeper Option for Inputs and I/Os

The ATF1508ASV(L) offers the option of programming all input and I/O pins so that "pin-keeper" circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high- or low-level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Input Diagram

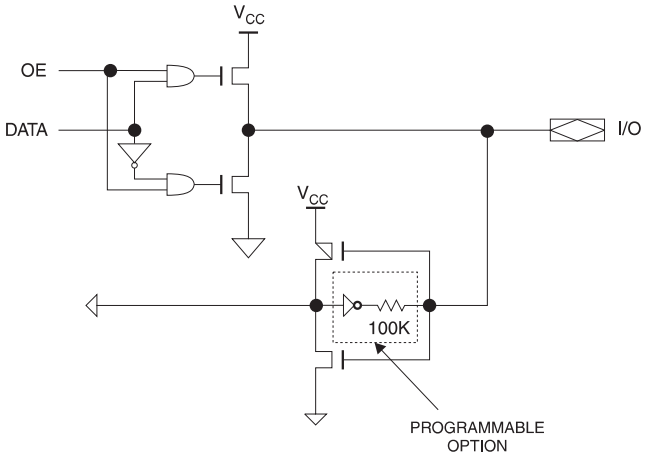


Speed/Power Management

The ATF1508ASV(L) has several built-in speed and power management features. The ATF1508ASV(L) contains circuitry that automatically puts the device into a low-power standby mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides proportional power-savings for most applications running at system speeds below 5 MHz.

To further reduce power, each ATF1508ASV(L) macrocell has a reduced-power bit feature. This feature allows individual macrocells to be configured for maximum power-savings. This feature may be selected as a design option.

I/O Diagram



All ATF1508 also have an optional power-down mode. In this mode, current drops to below 10 mA. When the power-down option is selected, either PD1 or PD2 pins (or both) can be used to power down the part. The power-down option is selected in the design source file. When enabled, the device goes into power-down when either PD1 or PD2 is high. In the power-down mode, all internal logic signals are latched and held, as are any enabled outputs.

All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output. However, the pin's macrocell may still be used to generate buried foldback and cascade logic signals.

All power-down AC characteristic parameters are computed from external input or I/O pins, with reduced-power bit turned on. For macrocells in reduced-power mode (reduced-power bit turned on), the reduced-power adder, t_{RPA}, must be added to the AC parameters, which include the data paths t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{ACH} and t_{SEXP}.

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching, and may be specified as fast switching in the design file.

Design Software Support

ATF1508ASV(L) designs are supported by several third-party tools. Automated fitters allow logic synthesis using a variety of high-level description languages and formats.

Power-up Reset

The ATF1508ASV is designed with a power-up reset, a feature critical for state machine initialization. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be initialized, and the state of each output will depend on the polarity of its buffer. However, due to the asynchronous nature of reset and uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and,
3. The clock must remain stable during T_D.

The ATF1508ASV has two options for the hysteresis about the reset level, V_{RST}, Small and Large. To ensure a robust operating environment in applications where the device is operated near 3.0V, Atmel recommends that during the fitting process users configure the device with the Power-up Reset hysteresis set to Large. For conversions, Atmel POF2JED users should include the flag "-power_reset" on the command line after "filename.POF". To allow the registers to be properly reinitialized with the Large hysteresis option selected, the following condition is added:

4. If V_{CC} falls below 2.0V, it must shut off completely before the device is turned on again.

When the Large hysteresis option is active, I_{CC} is reduced by several hundred microamps as well.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF1508ASV(L) fuse patterns. Once programmed, fuse verify is inhibited. However, User Signature and device ID remains accessible.

Programming

ATF1508ASV(L) devices are in-system programmable (ISP) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for programming and facilitates rapid design iterations and field changes.

Atmel provides ISP hardware and software to allow programming of the ATF1508ASV(L) via the PC. ISP is performed by using either a download cable, a comparable board tester or a simple microprocessor interface.

To allow ISP programming support by the Automated Test Equipment (ATE) vendors, Serial Vector Format (SVF) files can be created by the Atmel ISP software. Conversion to other ATE tester format beside SVF is also possible

ATF1508ASV(L) devices can also be programmed using standard third-party programmers. With third-party programmer, the JTAG ISP port can be disabled thereby allowing four additional I/O pins to be used for logic.

Contact your local Atmel representatives or Atmel PLD applications for details.

ISP Programming Protection

The ATF1508ASV(L) has a special feature that locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The inputs and I/O default to high-Z state during such a condition. In addition the pin-keeper option preserves the former state during device programming.

All ATF1508ASV(L) devices are initially shipped in the erased state thereby making them ready to use for ISP.

Note: For more information refer to the “Designing for In-System Programmability with Atmel CPLDs” application note.

AC Characteristics(1)

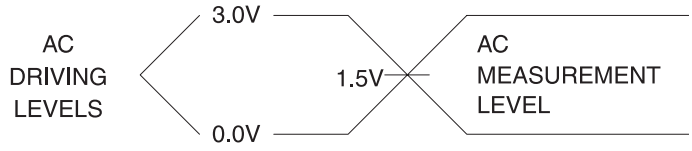
Symbol	Parameter	-15		-20		Units
		Min	Max	Min	Max	
t_{PD1}	Input or Feedback to Non-registered Output	3	15		20	ns
t_{PD2}	I/O Input or Feedback to Non-registered Feedback	3	12		16	ns
t_{SU}	Global Clock Setup Time	11		13.5		ns
t_{H}	Global Clock Hold Time	0		0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	3		3		ns
t_{FH}	Global Clock Hold Time of Fast Input	1.0		2.0		MHz
t_{COP}	Global Clock to Output Delay		9		12	ns
t_{CH}	Global Clock High Time	5		6		ns
t_{CL}	Global Clock Low Time	5		6		ns
t_{ASU}	Array Clock Setup Time	5		7		ns
t_{AH}	Array Clock Hold Time	4		4		ns
t_{ACOP}	Array Clock Output Delay		15		18.5	ns
t_{ACH}	Array Clock High Time	6		8		ns
t_{ACL}	Array Clock Low Time	6		8		ns
t_{CNT}	Minimum Clock Global Period		13		17	ns
f_{CNT}	Maximum Internal Global Clock Frequency	76.9		66		MHz
t_{ACNT}	Minimum Array Clock Period		13		17	ns
f_{ACNT}	Maximum Internal Array Clock Frequency	76.9		58.8		MHz
f_{MAX}	Maximum Clock Frequency	100		83.3		MHz
t_{IN}	Input Pad and Buffer Delay		2		2.5	ns
t_{IO}	I/O Input Pad and Buffer Delay		2		2.5	ns
t_{FIN}	Fast Input Delay		2		2	ns
t_{SEXP}	Foldback Term Delay		8		10	ns
t_{PEXP}	Cascade Logic Delay		1		1	ns
t_{LAD}	Logic Array Delay		6		8	ns
t_{LAC}	Logic Control Delay		3.5		4.5	ns
t_{IOE}	Internal Output Enable Delay		3		3	ns
t_{OD1}	Output Buffer and Pad Delay (Slow slew rate = OFF; V_{CCIO} = 5V; C_L = 35 pF)		3		4	ns
t_{OD2}	Output Buffer and Pad Delay (Slow slew rate = OFF; V_{CCIO} = 3.3V; C_L = 35 pF)		3		4	ns
t_{OD3}	Output Buffer and Pad Delay (Slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L = 35 pF)		5		6	ns
t_{ZX1}	Output Buffer Enable Delay (Slow slew rate = OFF; V_{CCIO} = 5.0V; C_L = 35 pF)		7		9	

AC Characteristics[1] (Continued)

Symbol	Parameter	-15		-20		Units
		Min	Max	Min	Max	
t_{ZX2}	Output Buffer Enable Delay (Slow slew rate = OFF; V_{CCIO} = 3.3V; C_L = 35 pF)		7		9	ns
t_{ZX3}	Output Buffer Enable Delay (Slow slew rate = ON; V_{CCIO} = 5.0V/3.3V; C_L = 35 pF)		10		11	ns
t_{XZ}	Output Buffer Disable Delay (C_L = 5 pF)		6		7	ns
t_{SU}	Register Setup Time	5		6		ns
t_H	Register Hold Time	4		5		ns
t_{FSU}	Register Setup Time of Fast Input	2		2		ns
t_{FH}	Register Hold Time of Fast Input	2		2		ns
t_{RD}	Register Delay		2		2.5	ns
t_{COMB}	Combinatorial Delay		2		3	ns
t_{IC}	Array Clock Delay		6		7	ns
t_{EN}	Register Enable Time		6		7	ns
t_{GLOB}	Global Control Delay		2		3	ns
t_{PRE}	Register Preset Time		4		5	ns
t_{CLR}	Register Clear Time		4		5	ns
t_{UIM}	Switch Matrix Delay		2		2.5	ns
t_{RPA}	Reduced-Power Adder[2]		10		13	ns

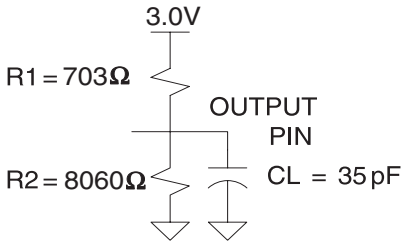
Notes: 1. See ordering information for valid part numbers.
2. The t_{RPA} parameter must be added to the t_{LAD}, t_{LAC},t_{TIC}, t_{ACL}, and t_{SEXP} parameters for macrocells running in the reduced-power mode.

Input Test Waveforms and Measurement Levels



t_R, t_F = 1.5 ns typical

Output AC Test Loads



Power-down Mode

The ATF1508ASV(L) includes two pins for optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin. When the PD1 and PD2 pin is high, the device supply current is reduced to less than 5 mA. During power-down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a high-Z state at the onset will remain at high-Z. During power-down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. The power-down pin feature is enabled in the logic design file. Designs using either power-down pin may not use the PD pin logic array input. However, buried logic resources in this macrocell may still be used.

Power Down AC Characteristics(1)(2)

Symbol	Parameter	-15		-20		Units
		Min	Max	Min	Max	
t_{IVDH}	Valid I, I/O before PD High	15		20		ns
t_{GVDH}	Valid OE(2) before PD High	15		20		ns
t_{CVDH}	Valid Clock(2) before PD High	15		20		ns
t_{DHIX}	I, I/O Don't Care after PD High		25		30	ns
t_{DHGX}	OE(2) Don't Care after PD High		25		30	ns
t_{DHCX}	Clock(2) Don't Care after PD High		25		30	ns
t_{DLIV}	PD Low to Valid I, I/O		1		1	µs
t_{DLGV}	PD Low to Valid OE (Pin or Term)		1		1	µs
t_{DLCV}	PD Low to Valid Clock (Pin or Term)		1		1	µs
t_{DLOV}	PD Low to Valid Output		1		1	µs

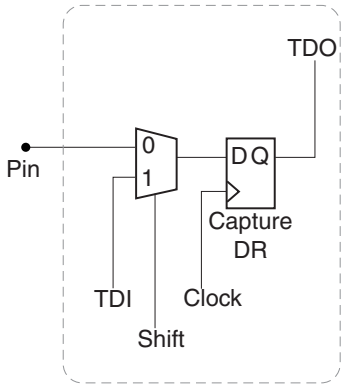
Notes: 1. For slow slew outputs, add t_{SSO}.
2. Pin or product term.

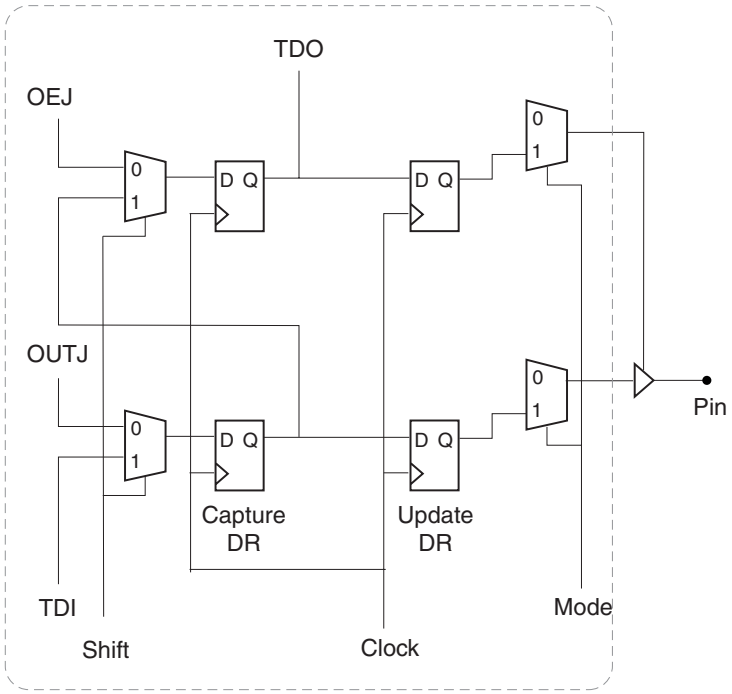
Boundary-scan Definition Language (BSDL) Models for the ATF1508

These are now available in all package types via the Atmel web site. These models can be used for Boundary-scan Test Operation in the ATF1508ASV(L) and have been scheduled to conform to the IEEE 1149.1 standard.

BSC Configuration for Macrocell

Pin BSC





Macrocell BSC

ATF1508ASV(L) Dedicated Pinouts

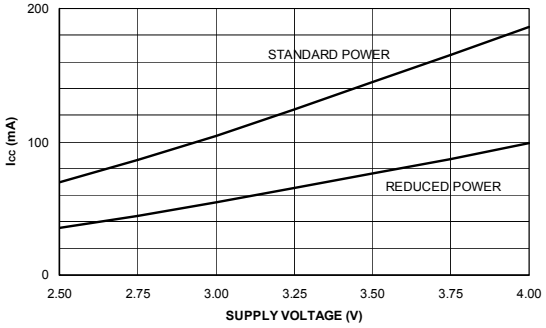
Dedicated Pin	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP
INPUT/OE2/GCLK2	2	92	90	142
INPUT/GCLR	1	91	89	141
INPUT/OE1	84	90	88	140
INPUT/GCLK1	83	89	87	139
I/O/GCLK3	81	87	85	137
I/O/PD (1, 2)	12,45	3,43	1,41	63,159
I/O/TDI(JTAG)	14	6	4	9
I/O/TMS(JTAG)	23	17	15	22
I/O/TCK(JTAG)	62	64	62	99
I/O/TDO(JTAG)	71	75	73	112
GND	7,19,32,42, 47,59,72,82	13,28,40,45, 61,76,88,97	11,26,38,43, 59,74,86,95	17,42,60,66,95, 113,138,148
VCC	3,13,26,38, 43,53,66,78	5,20,36,41, 53,68,84,93	3,18,34,39, 51,66,82,91	8,26,55,61,79,104,133,143
N/C	-	-	-	1,2,3,4,5,6,7,34,35,36, 37,38,39,40,44,45,46, 47,74,75,76,77,81,82, 83,84,85,86,87,114, 115,116,117,118,119, 120,124,125,126,127, 154,155,156,157
# of SIGNAL PINS	68	84	84	100
# USER I/O PINS	64	80	80	96

OE (1, 2)	Global OE pins
GCLR	Global Clear pin
GCLK (1, 2, 3)	Global Clock pins
PD (1, 2)	Power-down pins
TDI, TMS, TCK, TDO	JTAG pins used for boundary-scan testing or in-system programming
GND	Ground pins
VCC	VCC pins for the device

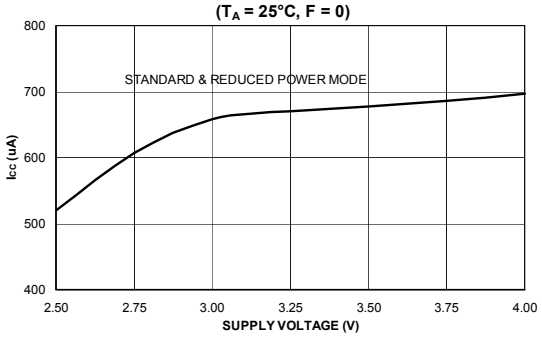
ATF1508ASV(L) I/O Pinouts

MC	PLB	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP	MC	PLB	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP
1	A	-	4	2	160	33	C	-	27	25	41
2	A	-	-	-	-	34	C	-	-	-	-
3	A/ **PD1**	12	3	1	159	35	C	31	26	24	33
4	A	-	-	-	158	36	C	-	-	-	32
5	A	11	2	100	153	37	C	30	25	23	31
6	A	10	1	99	152	38	C	29	24	22	30
7	A	-	-	-	-	39	C	-	-	-	-
8	A	9	100	98	151	40	C	28	23	21	29
9	A	-	99	97	150	41	C	-	22	20	28
10	A	-	-	-	-	42	C	-	-	-	-
11	A	8	98	96	149	43	C	27	21	19	27
12	A	-	-	-	147	44	C	-	-	-	25
13	A	6	96	94	146	45	C	25	19	17	24
14	A	5	95	93	145	46	C	24	18	16	23
15	A	-	-	-	-	47	C	-	-	-	-
16	A	4	94	92	144	48	C/ **TMS**	23	17	15	22
17	B	22	16	14	21	49	D	41	39	37	59
18	B	-	-	-	-	50	D	-	-	-	-
19	B	21	15	13	20	51	D	40	38	36	58
20	B	-	-	-	19	52	D	-	-	-	57
21	B	20	14	12	18	53	D	39	37	35	56
22	B	-	12	10	16	54	D	-	35	33	54
23	B	-	-	-	-	55	D	-	-	-	-
24	B	18	11	9	15	56	D	37	34	32	53
25	B	17	10	8	14	57	D	36	33	31	52
26	B	-	-	-	-	58	D	-	-	-	-
27	B	16	9	7	13	59	D	35	32	30	51
28	B	-	-	-	12	60	D	-	-	-	50
29	B	15	8	6	11	61	D	34	31	29	49
30	B	-	7	5	10	62	D	-	30	28	48
31	B	-	-	-	-	63	D	-	-	-	-
32	B/ **TDI**	14	6	4	9	64	D	33	29	27	43
65	E	44	42	40	62	97	G	63	65	63	100
66	E	-	-	-	-	98	G	-	-	-	-

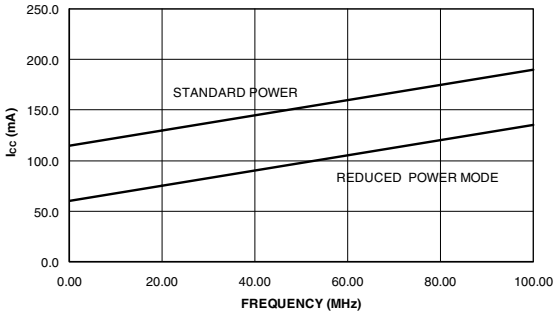
SUPPLY CURRENT VS. SUPPLY VOLTAGE
(T_A = 25°C, F = 0)



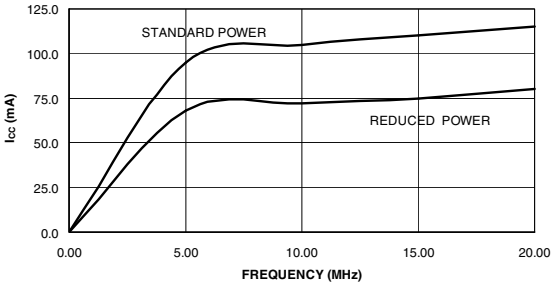
SUPPLY CURRENT VS. SUPPLY VOLTAGE
PIN-CONTROLLED POWER-DOWN MODE
(T_A = 25°C, F = 0)



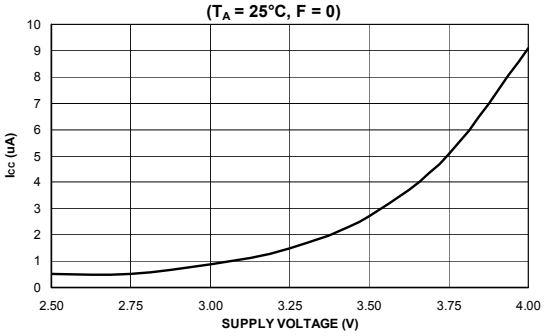
SUPPLY CURRENT VS. FREQUENCY
STANDARD POWER (T_A = 25°C)



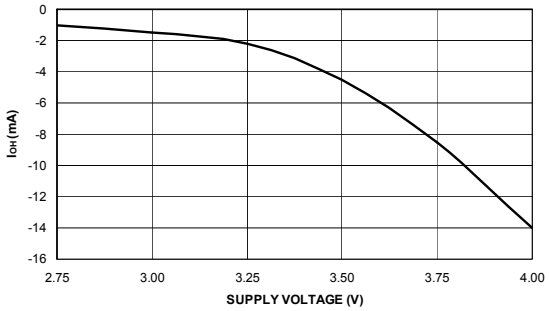
SUPPLY CURRENT VS. FREQUENCY
LOW-POWER ("L") VERSION
(T_A = 25°C)



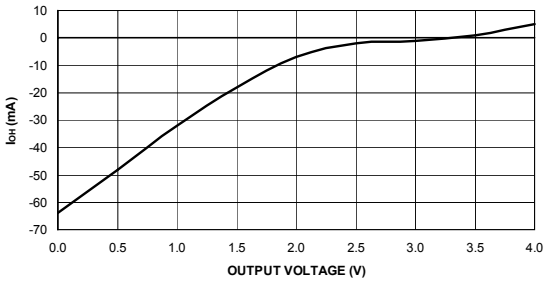
SUPPLY CURRENT VS. SUPPLY VOLTAGE
LOW POWER ("L") MODE
(T_A = 25°C, F = 0)



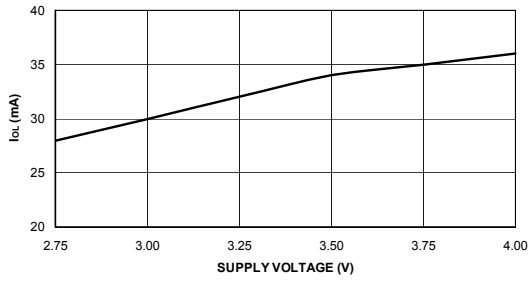
OUTPUT SOURCE CURRENT
VS. SUPPLY VOLTAGE (V_{OH} = 2.4V, T_A = 25°C)



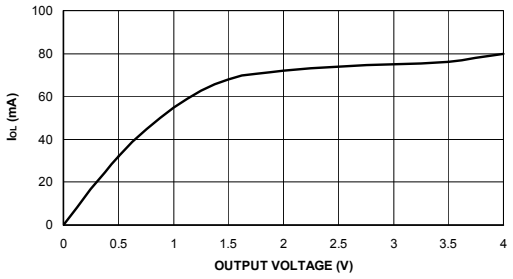
OUTPUT SOURCE CURRENT
VS. OUTPUT VOLTAGE (V_{CC} = 3.3V,T_A = 25°C)



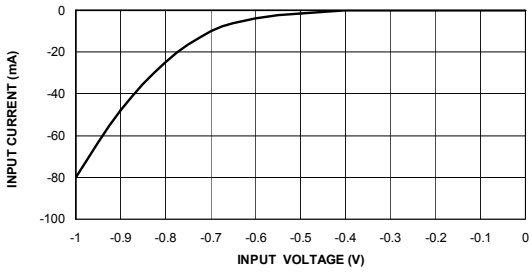
OUTPUT SINK CURRENT
VS. SUPPLY VOLTAGE (V_{OL} = 0.5V, T_A = 25°C)



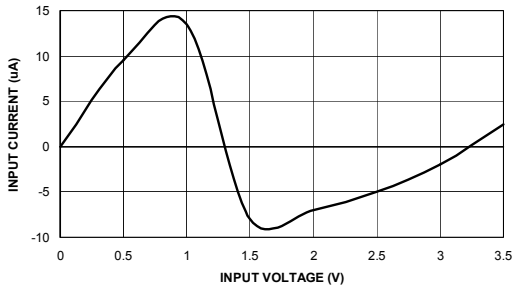
OUTPUT SINK CURRENT
VS. OUTPUT VOLTAGE (V_{CC} = 3.3V, T_A = 25°C)



INPUT CLAMP CURRENT
VS. INPUT VOLTAGE (V_{CC} = 3.3V, T_A = 25°C)



INPUT CURRENT vs. INPUT VOLTAGE
(V_{CC} = 3.3V, T_A = 25°C)



Ordering Information

ATF1508ASV(L) Standard Package Options

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
15	8	100	ATF1508ASV-15 JC84	84J	Commercial (0°C to 70°C)
			ATF1508ASV-15 QC100	100Q1	
			ATF1508ASV-15 AC100	100A	
			ATF1508ASV-15 QC160	160Q	
	8	100	ATF1508ASV-15 JI84	84J	Industrial (-40°C to +85°C)
			ATF1508ASV-15 QI100	100Q1	
			ATF1508ASV-15 AI100	100A	
			ATF1508ASV-15 QI160	160Q	
20	12	83.3	ATF1508ASVL-20 JC84	84J	Commercial (0°C to 70°C)
			ATF1508ASVL-20 QC100	100Q1	
			ATF1508ASVL-20 AC100	100A	
			ATF1508ASVL-20 QC160	160Q	
	12	83.3	ATF1508ASVL-20 JI84	84J	Industrial (-40°C to +85°C)
			ATF1508ASVL-20 QI100	100Q1	
			ATF1508ASVL-20 AI100	100A	
			ATF1508ASVL-20 QI160	160Q	

Note: 1. The last time buy is Sept. 30, 2005 for shaded parts.

Using “C” Product for Industrial

There is very little risk in using “C” devices for industrial applications because the V_{CC} conditions for 3.3V products are the same for commercial and industrial (there is only 15°C difference at the high end of the temperature range). To use commercial product for industrial temperature ranges, de-rate I_{CC} by 15%.

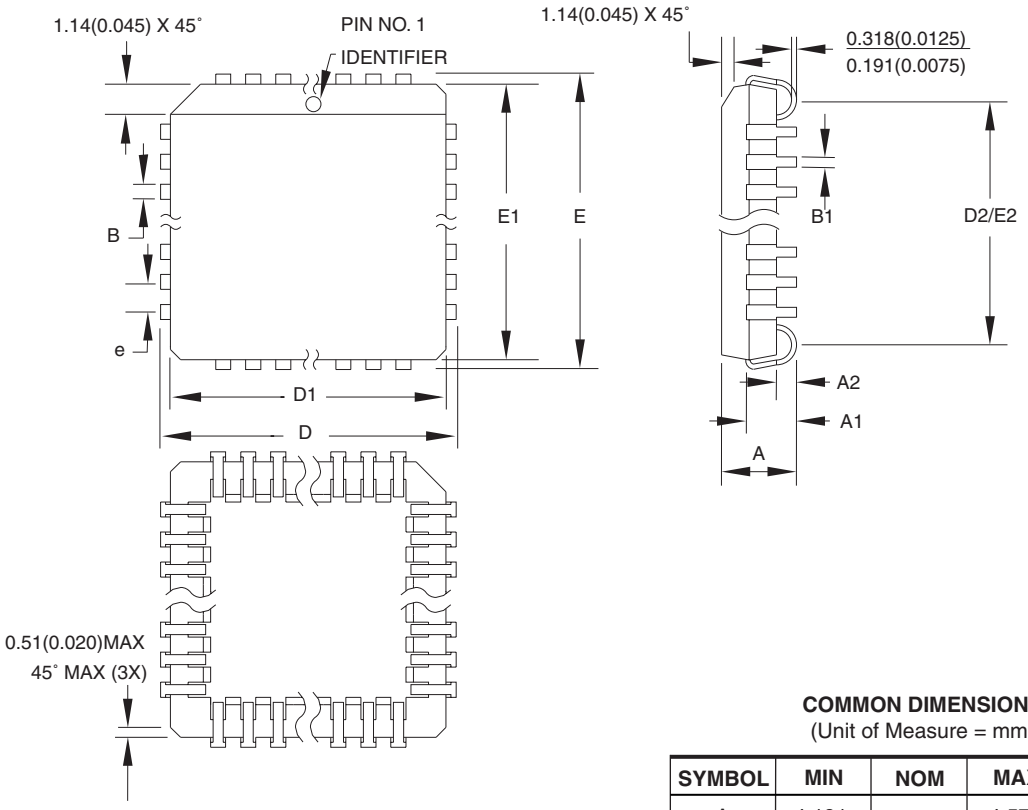
ATF1508ASV(L) Green Package Options (Pb/Halide-free/RoHS Compliant)

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
15	8	100	ATF1508ASV-15 JU84	84J	Industrial (-40°C to +85°C)
			ATF1508ASV-15 AU100	100A	
20	12	83.3	ATF1508ASVL-20 JU84	84J	Industrial (-40°C to +85°C)
			ATF1508ASVL-20 AU100	100A	

Package Type	
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100Q1	100-lead, Plastic Quad Pin Flat Package (PQFP)
100A	100-lead, Very Thin Plastic Gull Wing Quad Flat Package (TQFP)
160Q	160-lead, Plastic Quad Pin Flat Package (PQFP)

Packaging Information

84J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

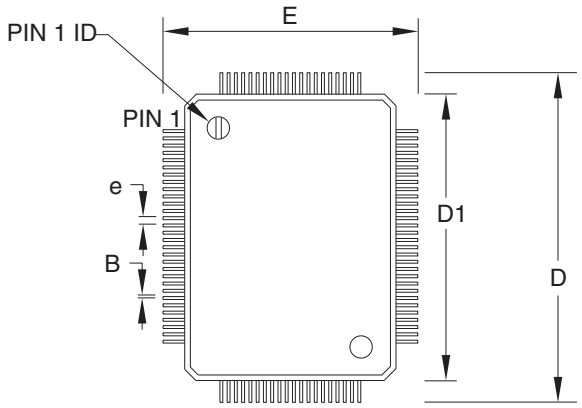
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	30.099	–	30.353	
D1	29.210	–	29.413	Note 2
E	30.099	–	30.353	
E1	29.210	–	29.413	Note 2
D2/E2	27.686	–	28.702	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

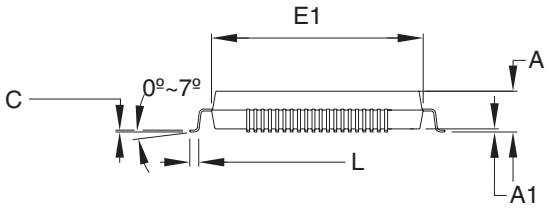
Notes:
1. This package conforms to JEDEC reference MS-018, Variation AF.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**84J**, 84-lead, Plastic J-leaded Chip Carrier (PLCC)	84J	B

100Q1 – PQFP





COMMON DIMENSIONS
(Unit of Measure = mm)
JEDEC STANDARD MS-022, GC-1

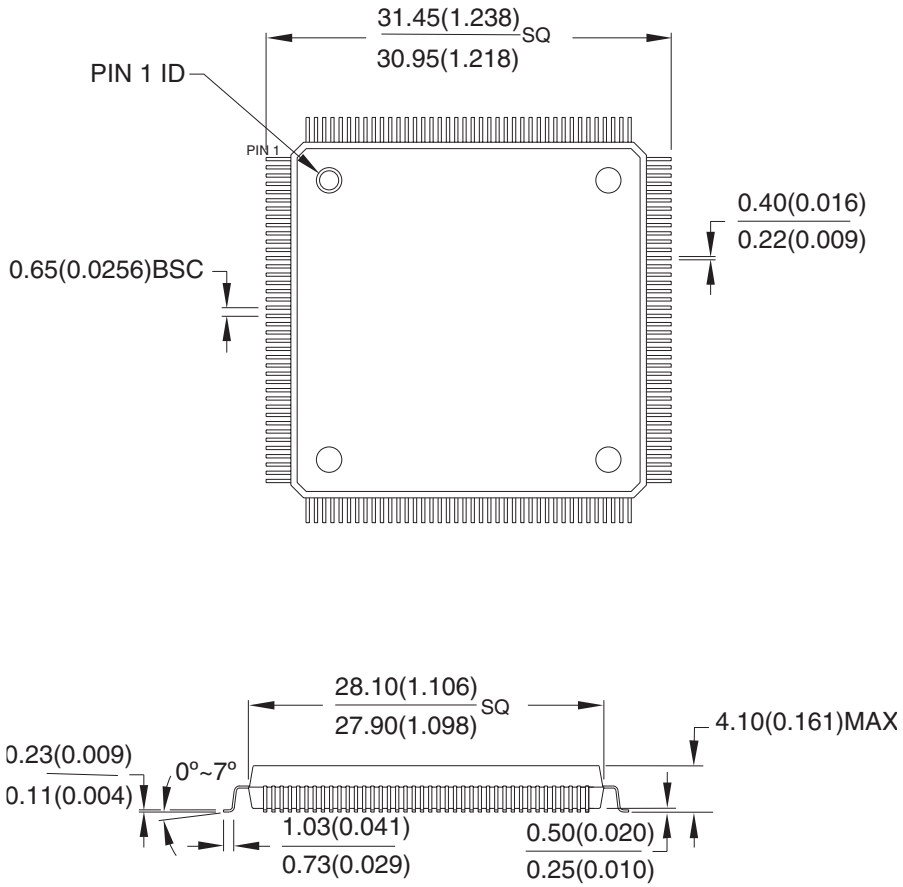
SYMBOL	MIN	NOM	MAX	NOTE
A	–	3.04	3.4	
A1	0.25	0.33	0.5	
D		23.20 BSC		
E		17.20 BSC		
E1		14.00 BSC		
B	0.22	–	0.40	
C	0.11	–	0.23	
D1		20 BSC		
L	0.73	–	1.03	
e		0.65 BSC		

07/6/2005

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100Q1**, 100-lead, 14 x 20 mm Body, 3.2 mm Footprint, 0.65 mm Pitch, Plastic Quad Flat Package (PQFP)	100Q1	C

160Q – PQFP

Dimensions in Millimeters and (Inches).
Controlling dimension: Millimeters.
JEDEC Standard MS-022 DC-1



10/23/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**160Q**, 160-lead, 28 x 28 mm Body, 3.2 mm Footprint, 0.65 mm Pitch, Plastic Quad Flat Package (PQFP)	160Q	B

Revision History

Revision	Comments
1408H	Corrected list of last buy parts.
1408G	Green package options added.