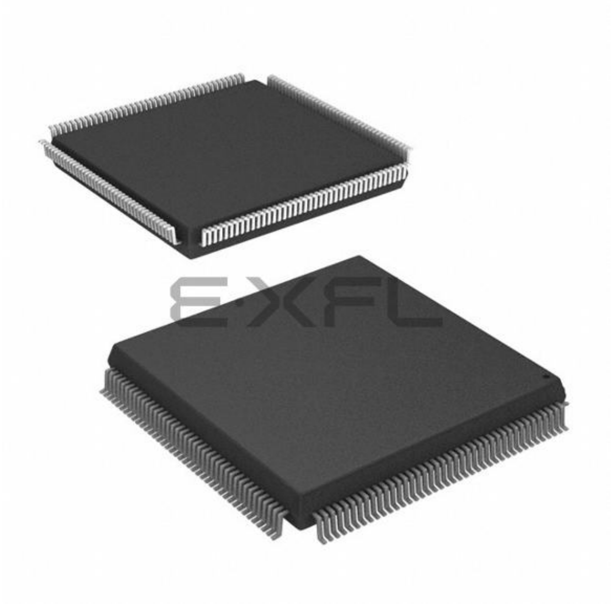


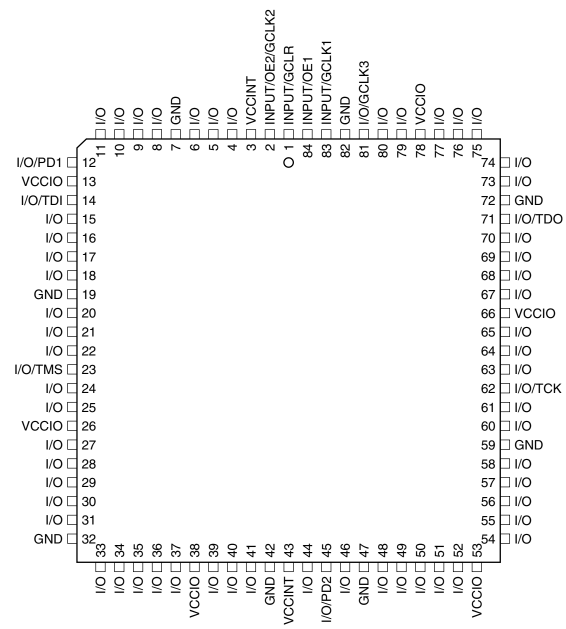
Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

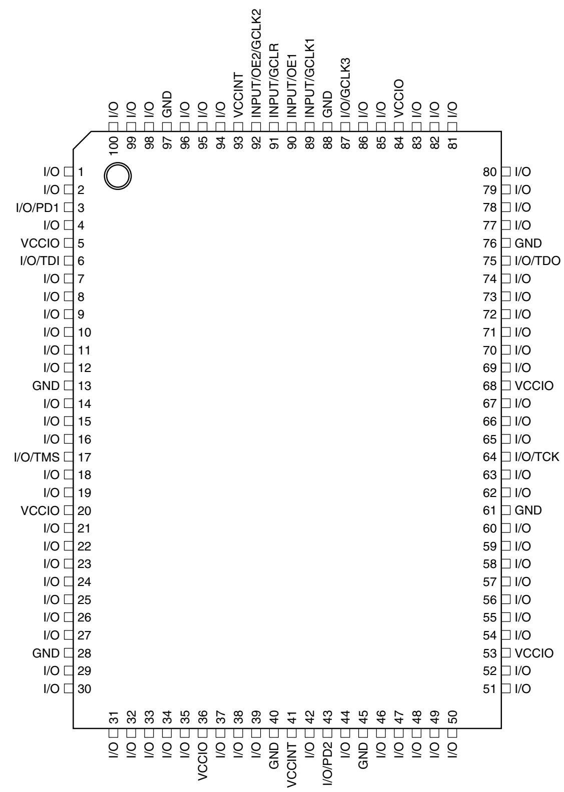
Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	20 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	96
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atf1508asvl-20qi160

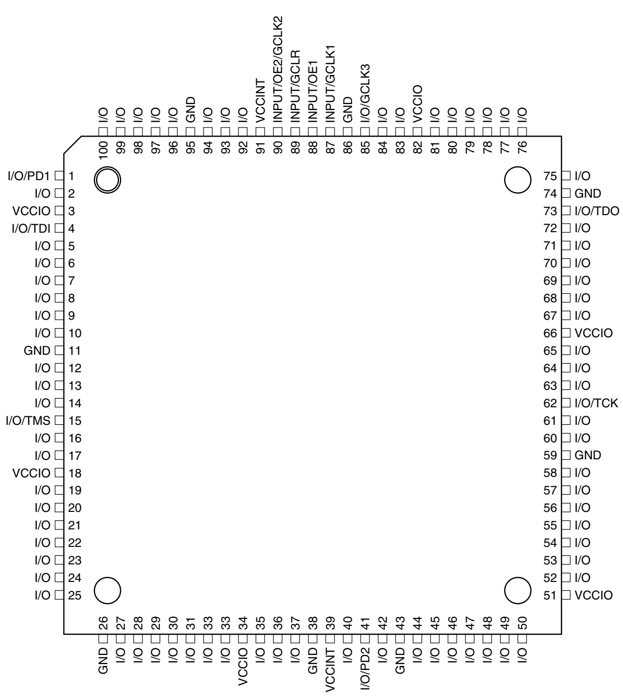
84-lead PLCC
Top View



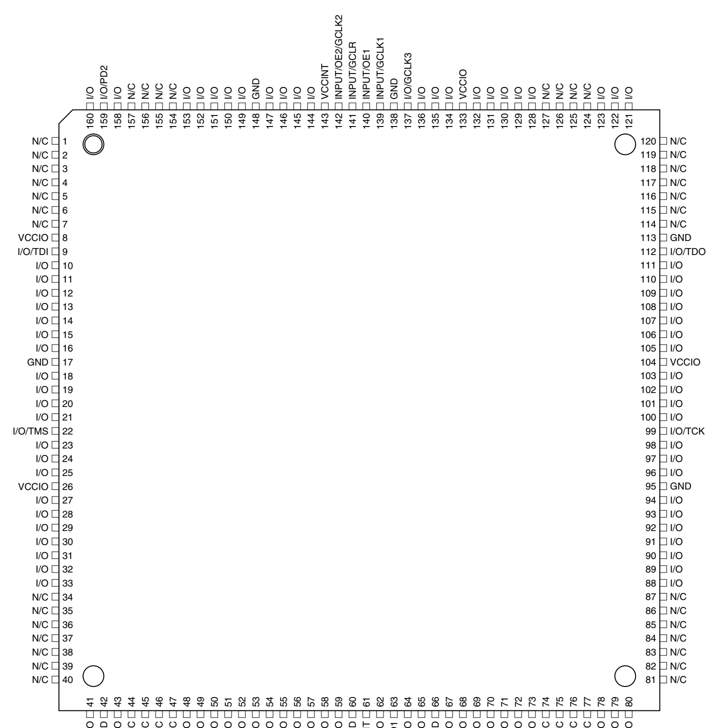
100-lead PQFP
Top View



100-lead TQFP
Top View



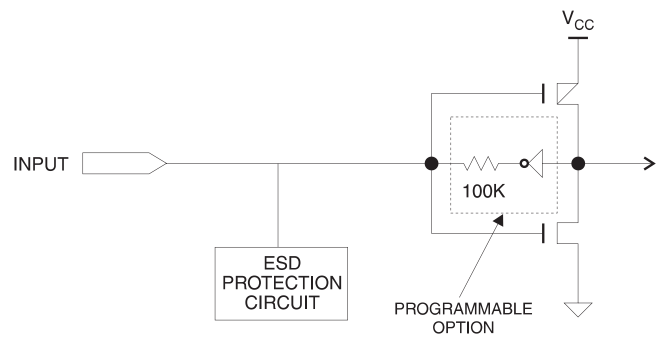
160-lead PQFP
Top View



Programmable Pin-keeper Option for Inputs and I/Os

The ATF1508ASV(L) offers the option of programming all input and I/O pins so that "pin-keeper" circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high- or low-level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Input Diagram

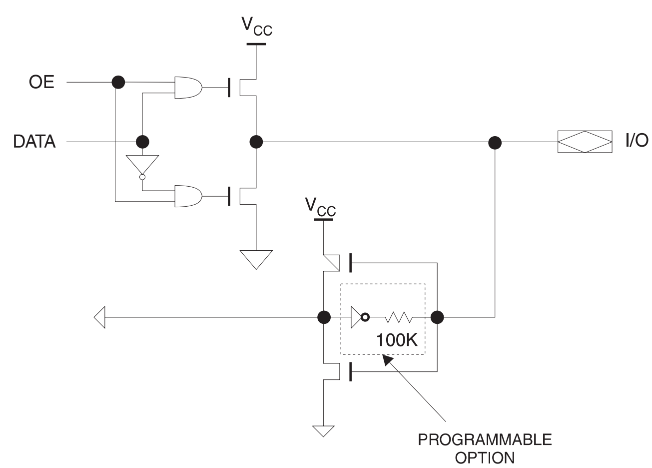


Speed/Power Management

The ATF1508ASV(L) has several built-in speed and power management features. The ATF1508ASV(L) contains circuitry that automatically puts the device into a low-power standby mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides proportional power-savings for most applications running at system speeds below 5 MHz.

To further reduce power, each ATF1508ASV(L) macrocell has a reduced-power bit feature. This feature allows individual macrocells to be configured for maximum power-savings. This feature may be selected as a design option.

I/O Diagram



All ATF1508 also have an optional power-down mode. In this mode, current drops to below 10 mA. When the power-down option is selected, either PD1 or PD2 pins (or both) can be used to power down the part. The power-down option is selected in the design source file. When enabled, the device goes into power-down when either PD1 or PD2 is high. In the power-down mode, all internal logic signals are latched and held, as are any enabled outputs.

All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output. However, the pin's macrocell may still be used to generate buried foldback and cascade logic signals.

All power-down AC characteristic parameters are computed from external input or I/O pins, with reduced-power bit turned on. For macrocells in reduced-power mode (reduced-power bit turned on), the reduced-power adder, t_{RPA}, must be added to the AC parameters, which include the data paths t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{ACH} and t_{SEXP}.

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching, and may be specified as fast switching in the design file.

Design Software Support

ATF1508ASV(L) designs are supported by several third-party tools. Automated fitters allow logic synthesis using a variety of high-level description languages and formats.

Power-up Reset

The ATF1508ASV is designed with a power-up reset, a feature critical for state machine initialization. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be initialized, and the state of each output will depend on the polarity of its buffer. However, due to the asynchronous nature of reset and uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and,
3. The clock must remain stable during T_D.

The ATF1508ASV has two options for the hysteresis about the reset level, V_{RST}, Small and Large. To ensure a robust operating environment in applications where the device is operated near 3.0V, Atmel recommends that during the fitting process users configure the device with the Power-up Reset hysteresis set to Large. For conversions, Atmel POF2JED users should include the flag "-power_reset" on the command line after "filename.POF". To allow the registers to be properly reinitialized with the Large hysteresis option selected, the following condition is added:

4. If V_{CC} falls below 2.0V, it must shut off completely before the device is turned on again.

When the Large hysteresis option is active, I_{CC} is reduced by several hundred microamps as well.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF1508ASV(L) fuse patterns. Once programmed, fuse verify is inhibited. However, User Signature and device ID remains accessible.

Programming

ATF1508ASV(L) devices are in-system programmable (ISP) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for programming and facilitates rapid design iterations and field changes.

Atmel provides ISP hardware and software to allow programming of the ATF1508ASV(L) via the PC. ISP is performed by using either a download cable, a comparable board tester or a simple microprocessor interface.

To allow ISP programming support by the Automated Test Equipment (ATE) vendors, Serial Vector Format (SVF) files can be created by the Atmel ISP software. Conversion to other ATE tester format beside SVF is also possible

ATF1508ASV(L) devices can also be programmed using standard third-party programmers. With third-party programmer, the JTAG ISP port can be disabled thereby allowing four additional I/O pins to be used for logic.

Contact your local Atmel representatives or Atmel PLD applications for details.

ISP Programming Protection

The ATF1508ASV(L) has a special feature that locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The inputs and I/O default to high-Z state during such a condition. In addition the pin-keeper option preserves the former state during device programming.

All ATF1508ASV(L) devices are initially shipped in the erased state thereby making them ready to use for ISP.

Note: For more information refer to the “Designing for In-System Programmability with Atmel CPLDs” application note.

DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient)	0°C - 70°C	-40°C - 85°C
V_{CC} (3.3V) Power Supply	3.0V - 3.6V	3.0V - 3.6V

DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$V_{IN} = V_{CC}$				-2	-10	µA
I_{IH}	Input or I/O High Leakage Current					2	10	µA
I_{OZ}	Tri-State Output Off-State Current	$V_O = V_{CC}$ or GND			-40		40	µA
I_{CC1}	Power Supply Current, Standby	V_{CC} = Max, $V_{IN} = 0$, V_{CC}	Std Mode	Com.		115		mA
				Ind.		135		mA
			"L" Mode	Com.		5		µA
				Ind.		5		µA
I_{CC2}	Power Supply Current, Power-down Mode	V_{CC} = Max, $V_{IN} = 0$, V_{CC}	"PD" Mode			0.1	5	mA
I_{CC3}[2]	Reduced-power Mode Supply Current, Standby	V_{CC} = Max, $V_{IN} = 0$, V_{CC}	Std Mode	Com.		60		mA
				Ind.		80		mA
V_{IL}	Input Low Voltage				-0.3		0.8	V
V_{IH}	Input High Voltage				1.7		V_{CCIO} + 0.3	V
V_{OL}	Output Low Voltage (TTL)	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min, I_{OL} = 8 mA		Com.			0.45	V
				Ind.			0.45	V
	Output Low Voltage (CMOS)	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min, I_{OL} = 0.1 mA		Com.			0.2	V
				Ind.			0.2	V
V_{OH}	Output High Voltage – 3.3V (TTL)	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min, I_{OH} = -2.0 mA			2.4			V
	Output High Voltage – 3.3V (CMOS)	$V_{IN} = V_{IH}$ or V_{IL}, V_{CCIO} = Min, I_{OH} = -0.1 mA			V_{CCIO} - 0.2			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. I_{CC3} refers to the current in the reduced-power mode when macrocell reduced-power is turned ON.

Pin Capacitance

	Typ	Max	Units	Conditions
C_{IN}		8	pF	V_{IN} = 0V; f = 1.0 MHz
$C_{I/O}$		8	pF	V_{OUT} = 0V; f = 1.0 MHz

Note: Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested. The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12 pF.

AC Characteristics[1]

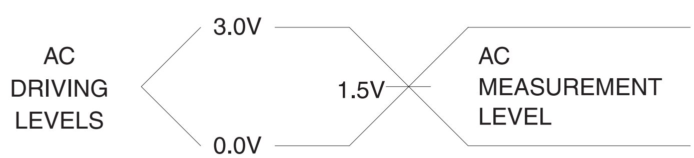
Symbol	Parameter	-15 Min	-15 Max	-20 Min	-20 Max	Units
t_{PD1}	Input or Feedback to Non-registered Output	3	15		20	ns
t_{PD2}	I/O Input or Feedback to Non-registered Feedback	3	12		16	ns
t_{SU}	Global Clock Setup Time	11		13.5		ns
t_H	Global Clock Hold Time	0		0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	3		3		ns
t_{FH}	Global Clock Hold Time of Fast Input	1.0		2.0		MHz
t_{COP}	Global Clock to Output Delay		9		12	ns
t_{CH}	Global Clock High Time	5		6		ns
t_{CL}	Global Clock Low Time	5		6		ns
t_{ASU}	Array Clock Setup Time	5		7		ns
t_{AH}	Array Clock Hold Time	4		4		ns
t_{ACOP}	Array Clock Output Delay		15		18.5	ns
t_{ACH}	Array Clock High Time	6		8		ns
t_{ACL}	Array Clock Low Time	6		8		ns
t_{CNT}	Minimum Clock Global Period		13		17	ns
f_{CNT}	Maximum Internal Global Clock Frequency	76.9		66		MHz
t_{ACNT}	Minimum Array Clock Period		13		17	ns
f_{ACNT}	Maximum Internal Array Clock Frequency	76.9		58.8		MHz
f_{MAX}	Maximum Clock Frequency	100		83.3		MHz
t_{IN}	Input Pad and Buffer Delay		2		2.5	ns
t_{IO}	I/O Input Pad and Buffer Delay		2		2.5	ns
t_{FIN}	Fast Input Delay		2		2	ns
t_{SEXP}	Foldback Term Delay		8		10	ns
t_{PEXP}	Cascade Logic Delay		1		1	ns
t_{LAD}	Logic Array Delay		6		8	ns
t_{LAC}	Logic Control Delay		3.5		4.5	ns
t_{IOE}	Internal Output Enable Delay		3		3	ns
t_{OD1}	Output Buffer and Pad Delay (Slow slew rate = OFF; V_{CCIO} = 5V; C_L = 35 pF)		3		4	ns
t_{OD2}	Output Buffer and Pad Delay (Slow slew rate = OFF; V_{CCIO} = 3.3V; C_L = 35 pF)		3		4	ns
t_{OD3}	Output Buffer and Pad Delay (Slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L = 35 pF)		5		6	ns
t_{ZX1}	Output Buffer Enable Delay (Slow slew rate = OFF; V_{CCIO} = 5.0V; C_L = 35 pF)		7		9	

AC Characteristics(1) (Continued)

Symbol	Parameter	-15 Min	-15 Max	-20 Min	-20 Max	Units
t_{ZX2}	Output Buffer Enable Delay (Slow slew rate = OFF; V_{CCIO} = 3.3V; C_L = 35 pF)		7		9	ns
t_{ZX3}	Output Buffer Enable Delay (Slow slew rate = ON; V_{CCIO} = 5.0V/3.3V; C_L = 35 pF)		10		11	ns
t_{XZ}	Output Buffer Disable Delay (C_L = 5 pF)		6		7	ns
t_{SU}	Register Setup Time	5		6		ns
t_H	Register Hold Time	4		5		ns
t_{FSU}	Register Setup Time of Fast Input	2		2		ns
t_{FH}	Register Hold Time of Fast Input	2		2		ns
t_{RD}	Register Delay		2		2.5	ns
t_{COMB}	Combinatorial Delay		2		3	ns
t_{IC}	Array Clock Delay		6		7	ns
t_{EN}	Register Enable Time		6		7	ns
t_{GLOB}	Global Control Delay		2		3	ns
t_{PRE}	Register Preset Time		4		5	ns
t_{CLR}	Register Clear Time		4		5	ns
t_{UIM}	Switch Matrix Delay		2		2.5	ns
t_{RPA}	Reduced-Power Adder(2)		10		13	ns

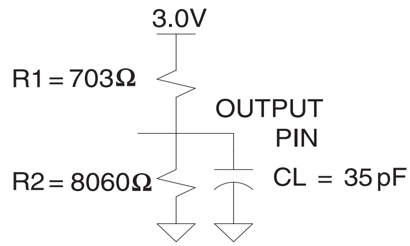
Notes: 1. See ordering information for valid part numbers.
2. The t_{RPA} parameter must be added to the t_{LAD}, t_{LAC},t_{TIC}, t_{ACL}, and t_{SEXP} parameters for macrocells running in the reduced-power mode.

Input Test Waveforms and Measurement Levels



t_R, t_F = 1.5 ns typical

Output AC Test Loads



Power-down Mode

The ATF1508ASV(L) includes two pins for optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin. When the PD1 and PD2 pin is high, the device supply current is reduced to less than 5 mA. During power-down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a high-Z state at the onset will remain at high-Z. During power-down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. The power-down pin feature is enabled in the logic design file. Designs using either power-down pin may not use the PD pin logic array input. However, buried logic resources in this macrocell may still be used.

Power Down AC Characteristics(1)(2)

Symbol	Parameter	-15		-20		Units
		Min	Max	Min	Max	
t_{IVDH}	Valid I, I/O before PD High	15		20		ns
t_{GVDH}	Valid OE(2) before PD High	15		20		ns
t_{CVDH}	Valid Clock(2) before PD High	15		20		ns
t_{DHIX}	I, I/O Don't Care after PD High		25		30	ns
t_{DHGX}	OE(2) Don't Care after PD High		25		30	ns
t_{DHCX}	Clock(2) Don't Care after PD High		25		30	ns
t_{DLIV}	PD Low to Valid I, I/O		1		1	µs
t_{DLGV}	PD Low to Valid OE (Pin or Term)		1		1	µs
t_{DLCV}	PD Low to Valid Clock (Pin or Term)		1		1	µs
t_{DLOV}	PD Low to Valid Output		1		1	µs

Notes: 1. For slow slew outputs, add t_{SSO}.
2. Pin or product term.

JTAG-BST Overview

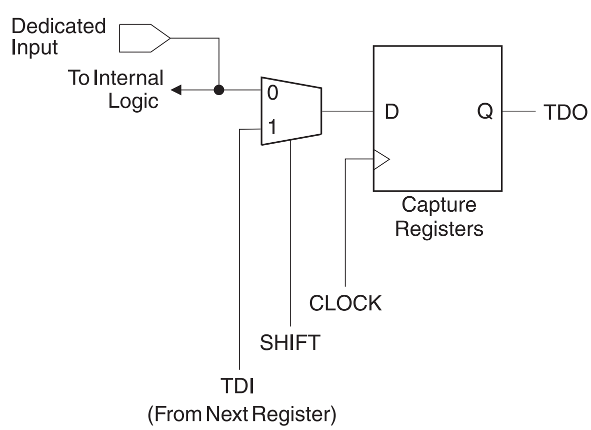
The JTAG-BST (JTAG boundary-scan testing) is controlled by the Test Access Port (TAP) controller in the ATF1508ASV(L). The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan cell) adjacent to each component so that signals at component boundaries can be controlled and observed using scan testing principles. Each input pin and I/O pin has its own Boundary-scan Cell (BSC) in order to support boundary-scan testing. The ATF1508ASV(L) does not currently include a Test Reset (TRST) input pin because the TAP controller is automatically reset at power-up. The six JTAG-BST modes supported include: SAMPLE/PRELOAD, EXTEST, BYPASS and IDCODE. BST on the ATF1508ASV(L) is implemented using the Boundary-scan Definition Language (BSDL) described in the JTAG specification (IEEE Standard 1149.1). Any third-party tool that supports the BSDL format can be used to perform BST on the ATF1508ASV(L).

The ATF1508ASV(L) also has the option of using four JTAG-standard I/O pins for in-system programming (ISP). The ATF1508ASV(L) is programmable through the four JTAG pins using programming-compatible with the IEEE JTAG Standard 1149.1. Programming is performed by using 5V TTL-level programming signals from the JTAG ISP interface. The JTAG feature is a programmable option. If JTAG (BST or ISP) is not needed, then the four JTAG control pins are available as I/O pins.

JTAG Boundary-scan Cell (BSC) Testing

The ATF1508ASV(L) contains up to 96 I/O pins and four input pins, depending on the device type and package type selected. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing as described in detail by IEEE Standard 1149.1. A typical BSC consists of three capture registers or scan registers and up to two update registers. There are two types of BSCs, one for input or I/O pin, and one for the macrocells. The BSCs in the device are chained together through the (BST) capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller. The BSC configuration for the input and I/O pins and macrocells are shown below.

BSC Configuration Pins and Macrocells (Except JTAG TAP Pins)



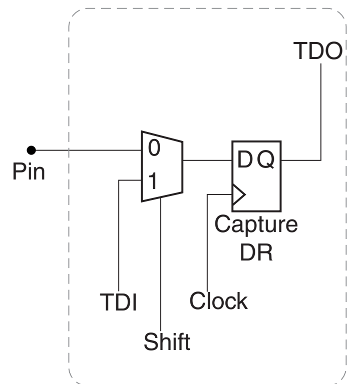
Note: The ATF1508ASV(L) has pull-up option on TMS and TDI pins. This feature is selected as a design option.

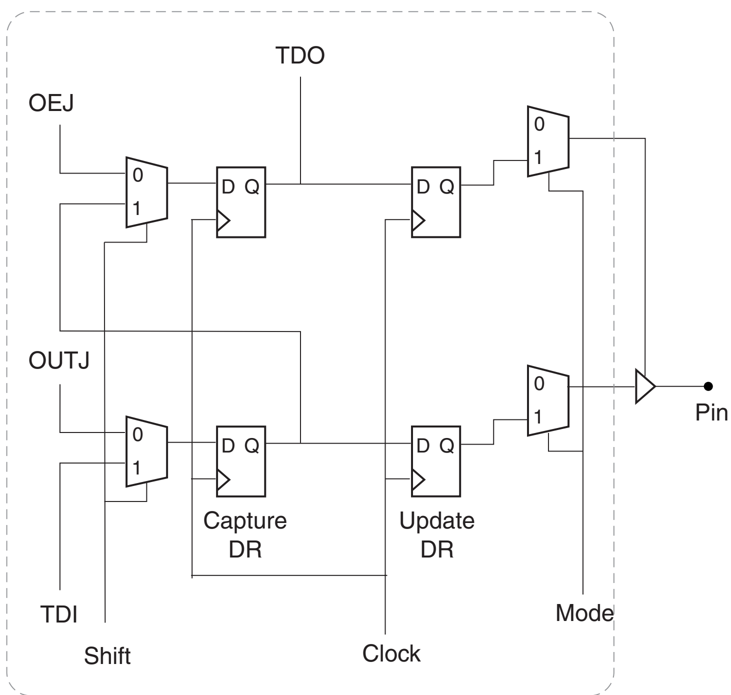
Boundary-scan Definition Language (BSDL) Models for the ATF1508

These are now available in all package types via the Atmel web site. These models can be used for Boundary-scan Test Operation in the ATF1508ASV(L) and have been scheduled to conform to the IEEE 1149.1 standard.

BSC Configuration for Macrocell

Pin BSC





Macrocell BSC

ATF1508ASV(L) Dedicated Pinouts

Dedicated Pin	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP
INPUT/OE2/GCLK2	2	92	90	142
INPUT/GCLR	1	91	89	141
INPUT/OE1	84	90	88	140
INPUT/GCLK1	83	89	87	139
I/O/GCLK3	81	87	85	137
I/O/PD (1, 2)	12,45	3,43	1,41	63,159
I/O/TDI(JTAG)	14	6	4	9
I/O/TMS(JTAG)	23	17	15	22
I/O/TCK(JTAG)	62	64	62	99
I/O/TDO(JTAG)	71	75	73	112
GND	7,19,32,42, 47,59,72,82	13,28,40,45, 61,76,88,97	11,26,38,43, 59,74,86,95	17,42,60,66,95, 113,138,148
VCC	3,13,26,38, 43,53,66,78	5,20,36,41, 53,68,84,93	3,18,34,39, 51,66,82,91	8,26,55,61,79,104,133,143
N/C	-	-	-	1,2,3,4,5,6,7,34,35,36, 37,38,39,40,44,45,46, 47,74,75,76,77,81,82, 83,84,85,86,87,114, 115,116,117,118,119, 120,124,125,126,127, 154,155,156,157
# of SIGNAL PINS	68	84	84	100
# USER I/O PINS	64	80	80	96

OE (1, 2)	Global OE pins
GCLR	Global Clear pin
GCLK (1, 2, 3)	Global Clock pins
PD (1, 2)	Power-down pins
TDI, TMS, TCK, TDO	JTAG pins used for boundary-scan testing or in-system programming
GND	Ground pins
VCC	VCC pins for the device

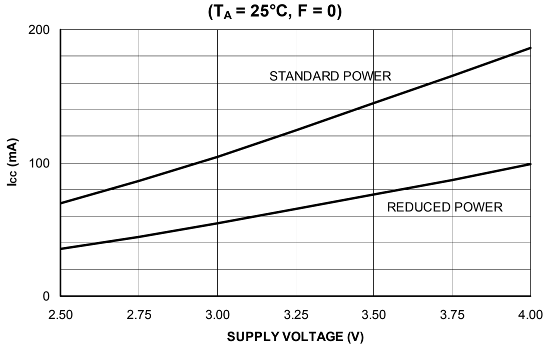
ATF1508ASV(L) I/O Pinouts

MC	PLB	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP	MC	PLB	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP
1	A	-	4	2	160	33	C	-	27	25	41
2	A	-	-	-	-	34	C	-	-	-	-
3	A/ **PD1**	12	3	1	159	35	C	31	26	24	33
4	A	-	-	-	158	36	C	-	-	-	32
5	A	11	2	100	153	37	C	30	25	23	31
6	A	10	1	99	152	38	C	29	24	22	30
7	A	-	-	-	-	39	C	-	-	-	-
8	A	9	100	98	151	40	C	28	23	21	29
9	A	-	99	97	150	41	C	-	22	20	28
10	A	-	-	-	-	42	C	-	-	-	-
11	A	8	98	96	149	43	C	27	21	19	27
12	A	-	-	-	147	44	C	-	-	-	25
13	A	6	96	94	146	45	C	25	19	17	24
14	A	5	95	93	145	46	C	24	18	16	23
15	A	-	-	-	-	47	C	-	-	-	-
16	A	4	94	92	144	48	C/ **TMS**	23	17	15	22
17	B	22	16	14	21	49	D	41	39	37	59
18	B	-	-	-	-	50	D	-	-	-	-
19	B	21	15	13	20	51	D	40	38	36	58
20	B	-	-	-	19	52	D	-	-	-	57
21	B	20	14	12	18	53	D	39	37	35	56
22	B	-	12	10	16	54	D	-	35	33	54
23	B	-	-	-	-	55	D	-	-	-	-
24	B	18	11	9	15	56	D	37	34	32	53
25	B	17	10	8	14	57	D	36	33	31	52
26	B	-	-	-	-	58	D	-	-	-	-
27	B	16	9	7	13	59	D	35	32	30	51
28	B	-	-	-	12	60	D	-	-	-	50
29	B	15	8	6	11	61	D	34	31	29	49
30	B	-	7	5	10	62	D	-	30	28	48
31	B	-	-	-	-	63	D	-	-	-	-
32	B/ **TDI**	14	6	4	9	64	D	33	29	27	43
65	E	44	42	40	62	97	G	63	65	63	100
66	E	-	-	-	-	98	G	-	-	-	-

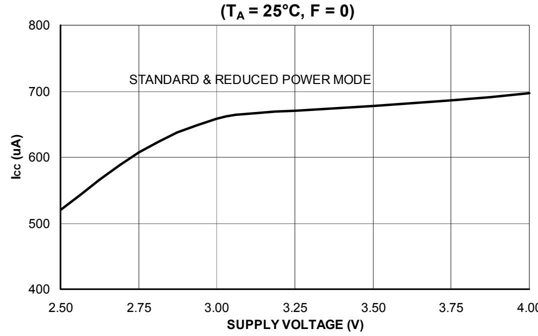
ATF1508ASV(L) I/O Pinouts (Continued)

MC	PLB	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP	MC	PLB	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP
67	E/ **PD2**	45	43	41	63	99	G	64	66	64	101
68	E	-	-	-	64	100	G	-	-	-	102
69	E	46	44	42	65	101	G	65	67	65	103
70	E	-	46	44	67	102	G	-	69	67	105
71	E	-	-	-	-	103	G	-	-	-	-
72	E	48	47	45	68	104	G	67	70	68	106
73	E	49	48	46	69	105	G	68	71	69	107
74	E	-	-	-	-	106	G	-	-	-	-
75	E	50	49	47	70	107	G	69	72	70	108
76	E	-	-	-	71	108	G	-	-	-	109
77	E	51	50	48	72	109	G	70	73	71	110
78	E	-	51	49	73	110	G	-	74	72	111
79	E	-	-	-	-	111	G	-	-	-	-
80	E	52	52	50	78	112	G/ **TDO**	71	75	73	112
81	F	-	54	52	80	113	H	-	77	75	121
82	F	-	-	-	-	114	H	-	-	-	-
83	F	54	55	53	88	115	H	73	78	76	122
84	F	-	-	-	89	116	H	-	-	-	123
85	F	55	56	54	90	117	H	74	79	77	128
86	F	56	57	55	91	118	H	75	80	78	129
87	F	-	-	-	-	119	H	-	-	-	-
88	F	57	58	56	92	120	H	76	81	79	130
89	F	-	59	57	93	121	H	-	82	80	131
90	F	-	-	-	-	122	H	-	-	-	-
91	F	58	60	58	94	123	H	77	83	81	132
92	F	-	-	-	96	124	H	-	-	-	134
93	F	60	62	60	97	125	H	79	85	83	135
94	F	61	63	61	98	126	H	80	86	84	136
95	F	-	-	-	-	127	H	-	-	-	-
96	F/ **TCK**	62	64	62	99	128	H/ **GCLK3**	81	87	85	137

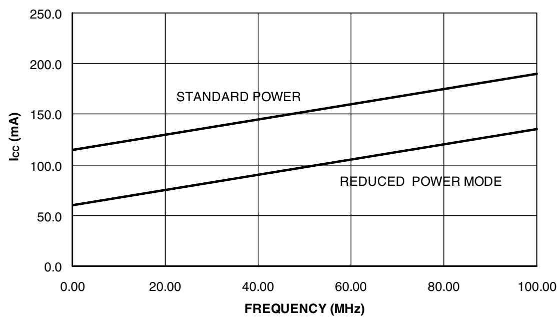
SUPPLY CURRENT VS. SUPPLY VOLTAGE
(T_A = 25°C, F = 0)



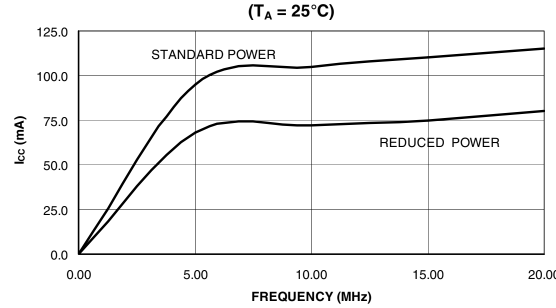
SUPPLY CURRENT VS. SUPPLY VOLTAGE
PIN-CONTROLLED POWER-DOWN MODE
(T_A = 25°C, F = 0)



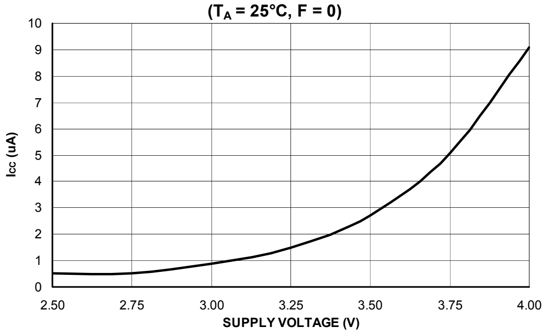
SUPPLY CURRENT VS. FREQUENCY
STANDARD POWER (T_A = 25°C)



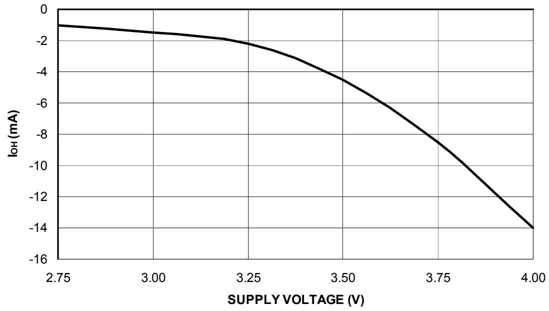
SUPPLY CURRENT VS. FREQUENCY
LOW-POWER ("L") VERSION
(T_A = 25°C)



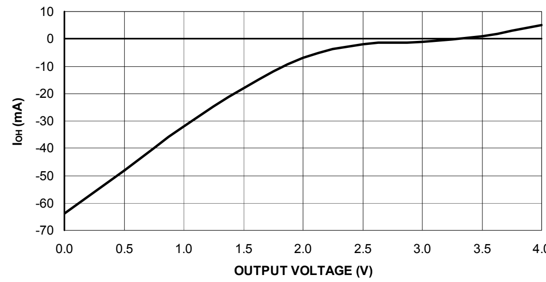
SUPPLY CURRENT VS. SUPPLY VOLTAGE
LOW POWER ("L") MODE
(T_A = 25°C, F = 0)



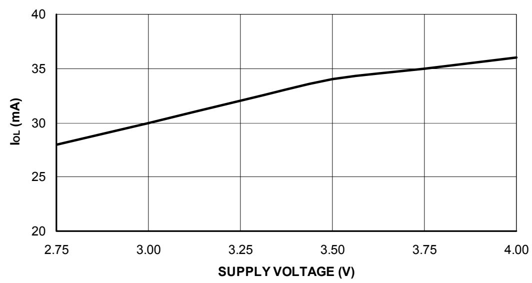
OUTPUT SOURCE CURRENT
VS. SUPPLY VOLTAGE (V_{OH} = 2.4V, T_A = 25°C)



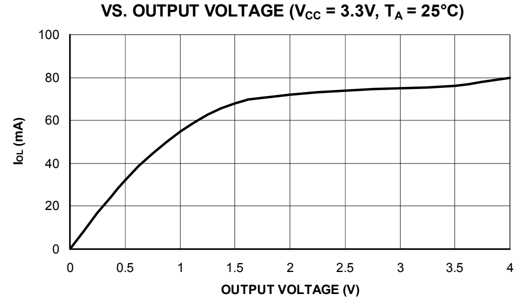
OUTPUT SOURCE CURRENT
VS. OUTPUT VOLTAGE (V_{CC} = 3.3V,T_A = 25°C)



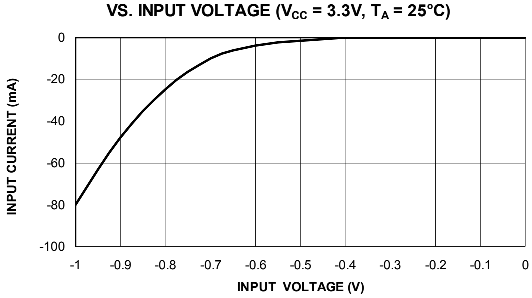
OUTPUT SINK CURRENT
VS. SUPPLY VOLTAGE (V_{OL} = 0.5V, T_A = 25°C)



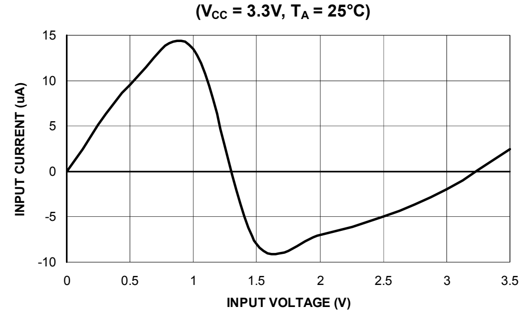
OUTPUT SINK CURRENT
VS. OUTPUT VOLTAGE (V_{CC} = 3.3V, T_A = 25°C)



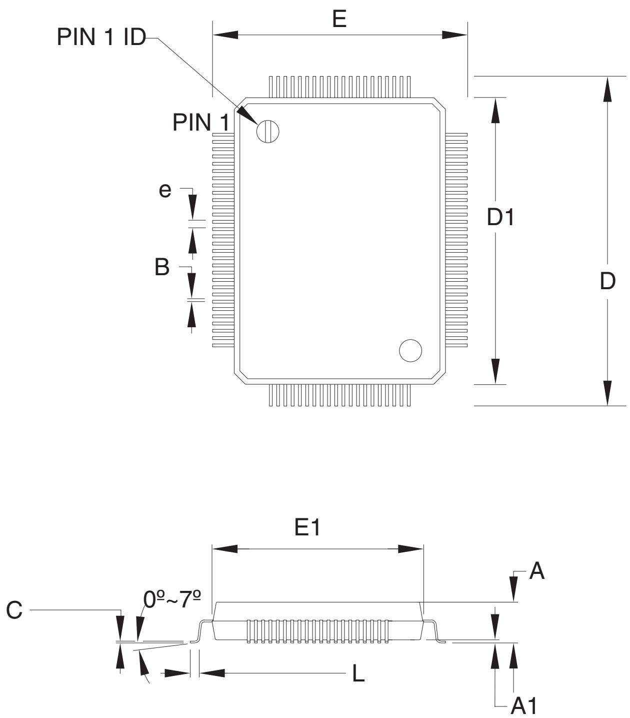
INPUT CLAMP CURRENT
VS. INPUT VOLTAGE (V_{CC} = 3.3V, T_A = 25°C)



INPUT CURRENT vs. INPUT VOLTAGE
(V_{CC} = 3.3V, T_A = 25°C)



100Q1 – PQFP



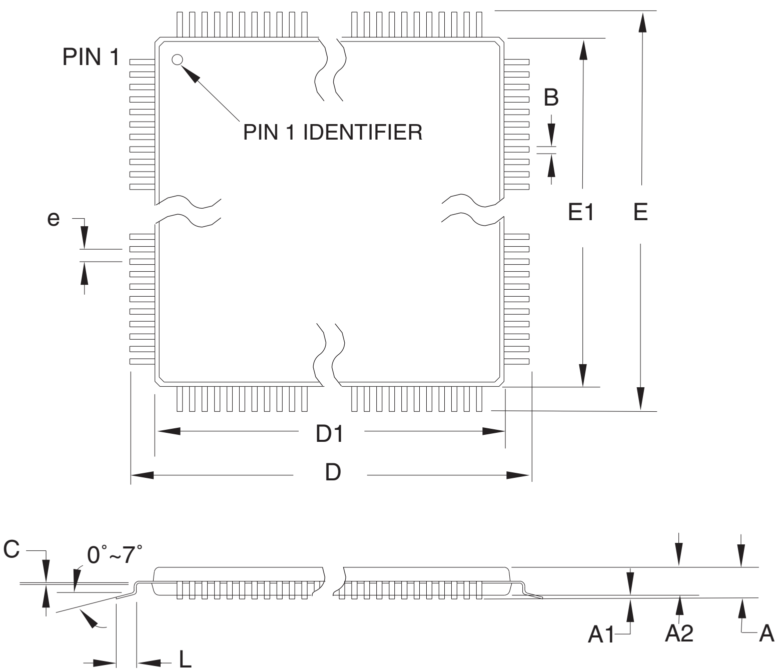
COMMON DIMENSIONS
(Unit of Measure = mm)
JEDEC STANDARD MS-022, GC-1

SYMBOL	MIN	NOM	MAX	NOTE
A	–	3.04	3.4	
A1	0.25	0.33	0.5	
D		23.20 BSC		
E		17.20 BSC		
E1		14.00 BSC		
B	0.22	–	0.40	
C	0.11	–	0.23	
D1		20 BSC		
L	0.73	–	1.03	
e		0.65 BSC		

07/6/2005

	TITLE	DRAWING NO.	REV.
ATMEL 2325 Orchard Parkway San Jose, CA 95131	**100Q1**, 100-lead, 14 x 20 mm Body, 3.2 mm Footprint, 0.65 mm Pitch, Plastic Quad Flat Package (PQFP)	100Q1	C

100A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.17	–	0.27	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.50 TYP			

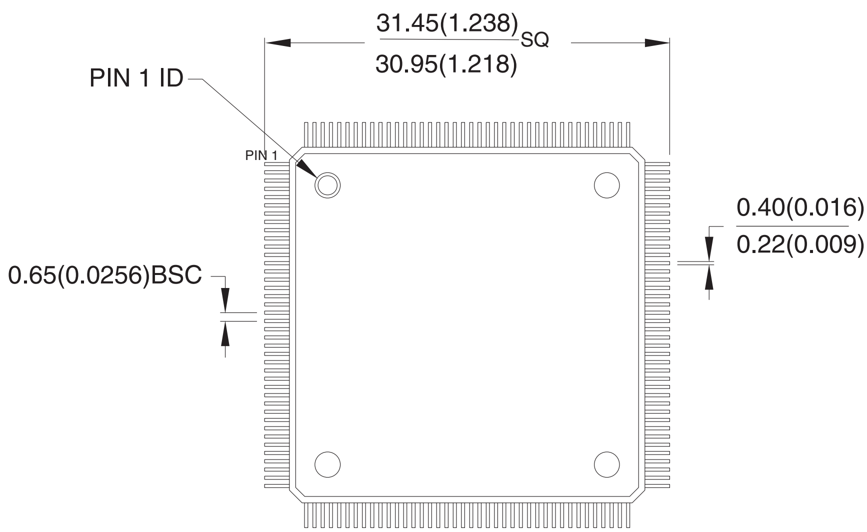
Notes:
1. This package conforms to JEDEC reference MS-026, Variation AED.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.08 mm maximum.

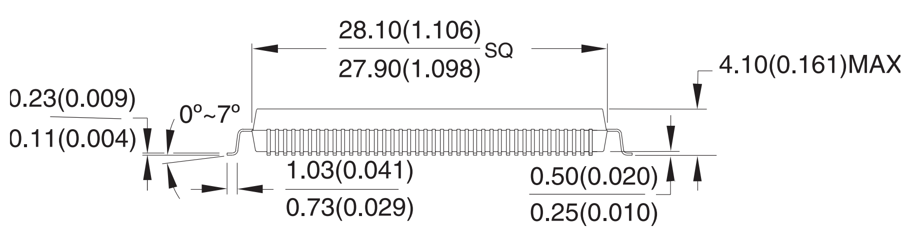
10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100A,** 100-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.5 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	100A	C

160Q – PQFP

Dimensions in Millimeters and (Inches).
Controlling dimension: Millimeters.
JEDEC Standard MS-022 DC-1





10/23/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**160Q**, 160-lead, 28 x 28 mm Body, 3.2 mm Footprint, 0.65 mm Pitch, Plastic Quad Flat Package (PQFP)	160Q	B

Revision History

Revision	Comments
1408H	Corrected list of last buy parts.
1408G	Green package options added.

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