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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

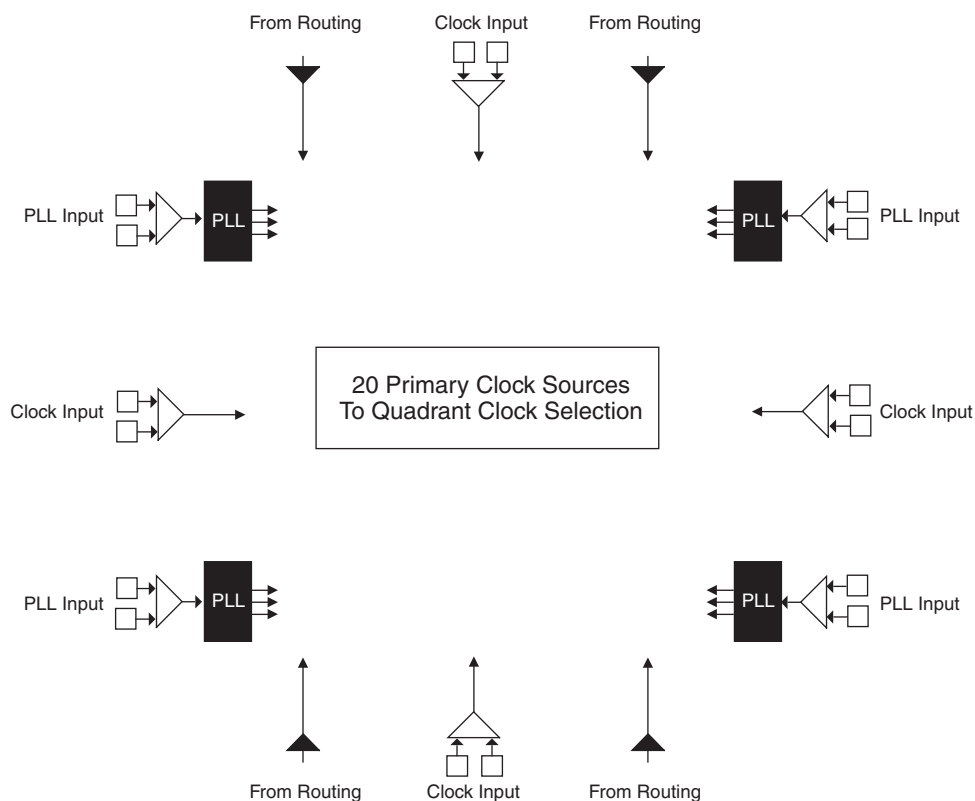
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10000
Total RAM Bits	221184
Number of I/O	244
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	388-BBGA
Supplier Device Package	388-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp10c-3f388c

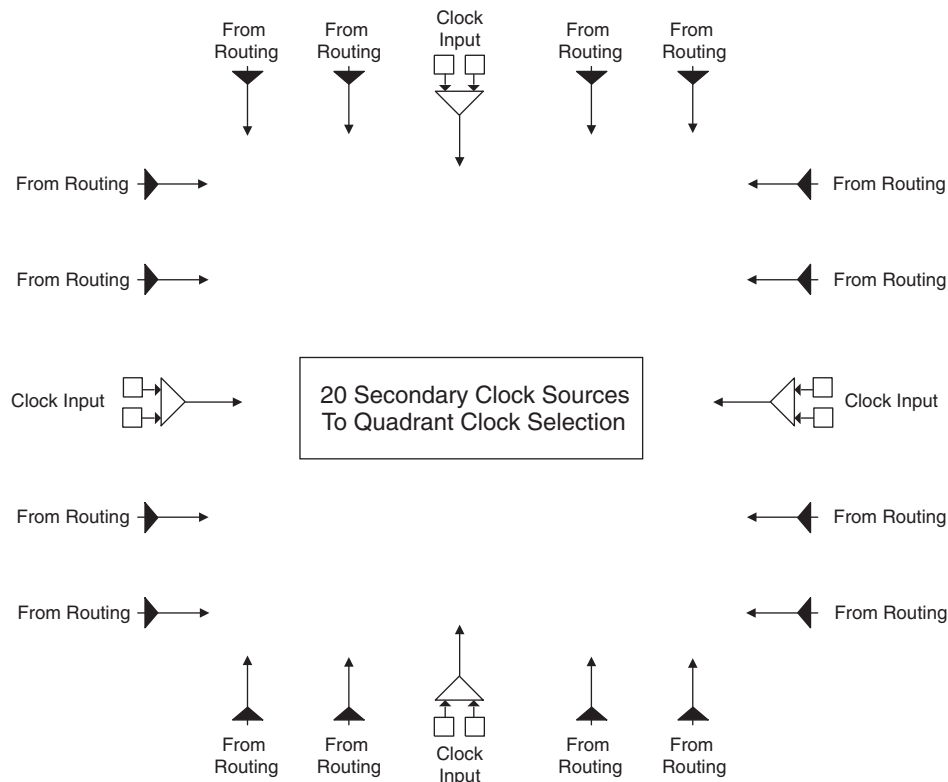
Figure 2-5. Primary Clock Sources

Note: Smaller devices have two PLLs.

Secondary Clock Sources

LatticeXP devices have four secondary clock resources per quadrant. The secondary clock branches are tapped at every PFU. These secondary clock networks can also be used for controls and high fanout data. These secondary clocks are derived from four clock input pads and 16 routing signals as shown in Figure 2-6.

Figure 2-6. Secondary Clock Sources



Clock Routing

The clock routing structure in LatticeXP devices consists of four Primary Clock lines and a Secondary Clock network per quadrant. The primary clocks are generated from MUXs located in each quadrant. Figure 2-7 shows this clock routing. The four secondary clocks are generated from MUXs located in each quadrant as shown in Figure 2-8. Each slice derives its clock from the primary clock lines, secondary clock lines and routing as shown in Figure 2-9.

Figure 2-7. Per Quadrant Primary Clock Selection

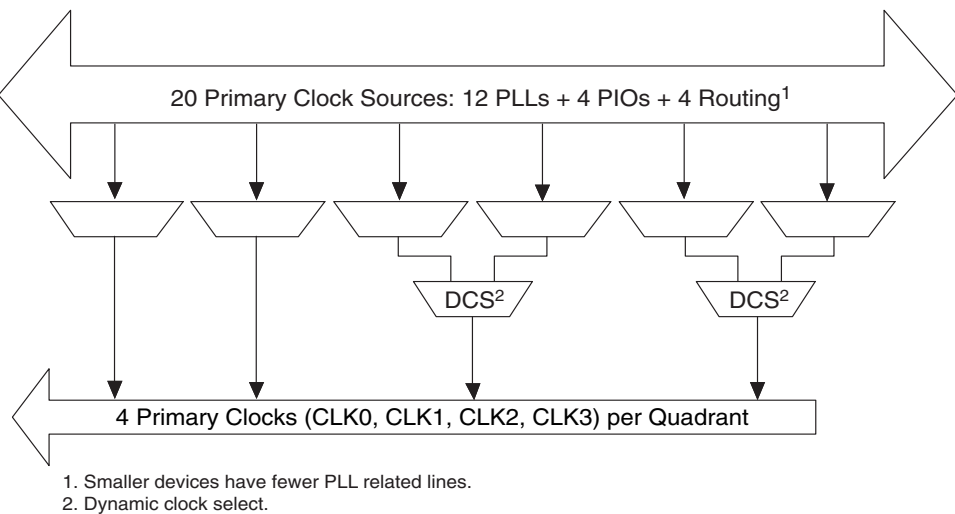
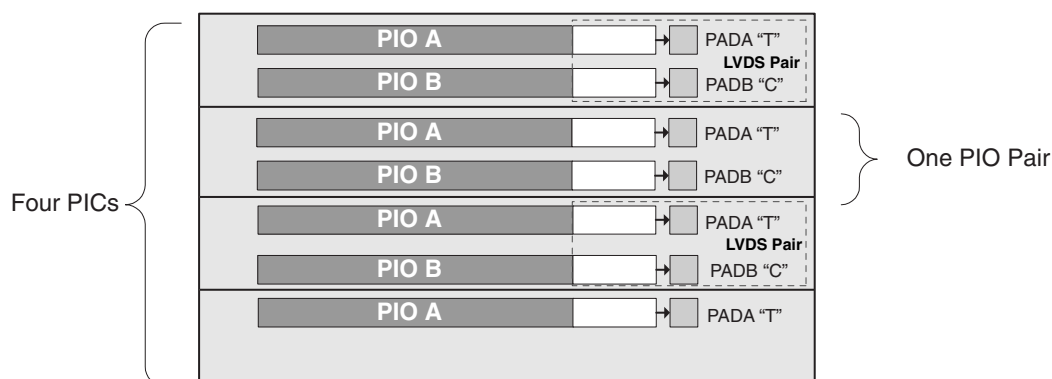
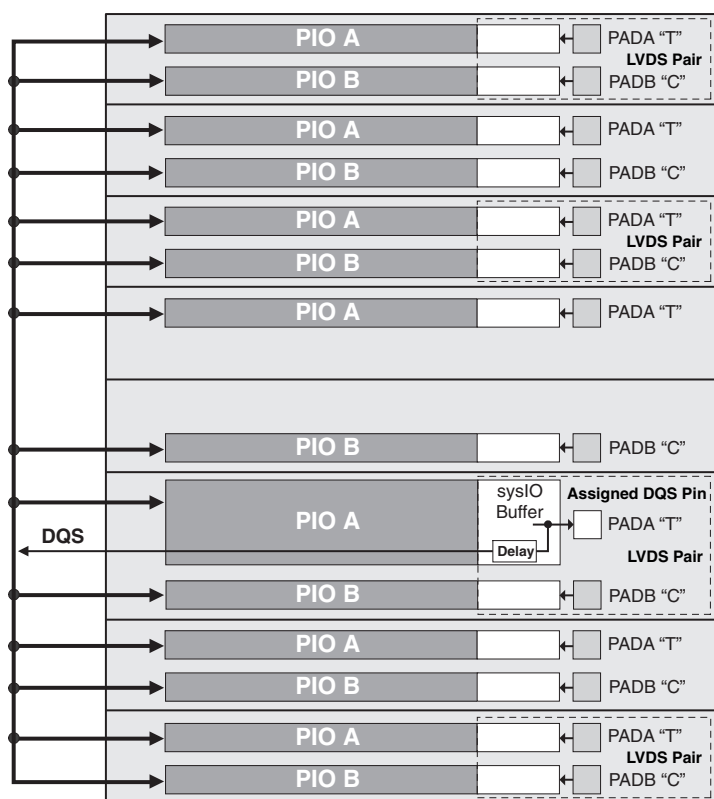


Figure 2-18. Group of Seven PIOs**Figure 2-19. DQS Routing**

PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for both single data rate (SDR) and double data rate (DDR) operation along with the necessary clock and selection logic. Programmable delay lines used to shift incoming clock and data signals are also included in these blocks.

Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-20 shows the diagram of the input register block.

Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and

Table 2-8. Supported Output Standards

Output Standard	Drive	V _{CCIO} (Nom.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVC MOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVC MOS25	4mA, 8mA, 12mA 16mA, 20mA	2.5
LVC MOS18	4mA, 8mA, 12mA 16mA	1.8
LVC MOS15	4mA, 8mA	1.5
LVC MOS12	2mA, 6mA	1.2
LVC MOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVC MOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVC MOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVC MOS15, Open Drain	4mA, 8mA	—
LVC MOS12, Open Drain	2mA, 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II, III	N/A	1.8
HSTL15 Class I, III	N/A	1.5
SSTL3 Class I, II	N/A	3.3
SSTL2 Class I, II	N/A	2.5
SSTL18 Class I	N/A	1.8
Differential Interfaces		
Differential SSTL3, Class I, II	N/A	3.3
Differential SSTL2, Class I, II	N/A	2.5
Differential SSTL18, Class I	N/A	1.8
Differential HSTL18, Class I, II, III	N/A	1.8
Differential HSTL15, Class I, III	N/A	1.5
LVDS	N/A	2.5
BLVDS ¹	N/A	2.5
LVPECL ¹	N/A	3.3

1. Emulated with external resistors.

Hot Socketing

The LatticeXP devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits, which allows easy integration with the rest of the system. These capabilities make the LatticeXP ideal for many multiple power supply and hot-swap applications.

Sleep Mode

The LatticeXP “C” devices (V_{CC} = 1.8/2.5/3.3V) have a sleep mode that allows standby current to be reduced by up to three orders of magnitude during periods of system inactivity. Entry and exit to Sleep Mode is controlled by the SLEEPN pin.

During Sleep Mode, the FPGA logic is non-operational, registers and EBR contents are not maintained and I/Os are tri-stated. Do not enter Sleep Mode during device programming or configuration operation. In Sleep Mode, power supplies can be maintained in their normal operating range, eliminating the need for external switching of power supplies. Table 2-9 compares the characteristics of Normal, Off and Sleep Modes.

Figure 2-29 provides a pictorial representation of the different programming ports and modes available in the LatticeXP devices.

On power-up, the FPGA SRAM is ready to be configured with the sysCONFIG port active. The IEEE 1149.1 serial mode can be activated any time after power-up by sending the appropriate command through the TAP port.

Leave Alone I/O

When using 1532 mode for non-volatile memory programming, users may specify I/Os as high, low, tristated or held at current value. This provides excellent flexibility for implementing systems where reprogramming occurs on-the-fly.

TransFR (Transparent Field Reconfiguration)

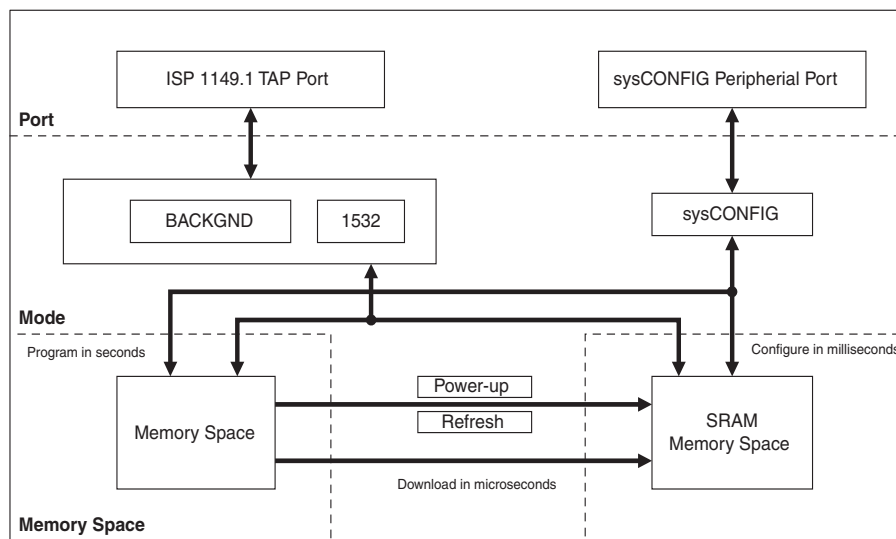
TransFR (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. See Lattice technical note #TN1087, *Minimizing System Interruption During Configuration Using TransFR Technology*, for details.

Security

The LatticeXP devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile memory spaces. Once set, the only way to clear security bits is to erase the memory space.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

Figure 2-29. ispXP Block Diagram



Internal Logic Analyzer Capability (ispTRACY)

All LatticeXP devices support an internal logic analyzer diagnostic feature. The diagnostic features provide capabilities similar to an external logic analyzer, such as programmable event and trigger condition and deep trace memory. This feature is enabled by Lattice's ispTRACY. The ispTRACY utility is added into the user design at compile time.

For more information on ispTRACY, please see information regarding additional technical documentation at the end of this data sheet.

Oscillator

Every LatticeXP device has an internal CMOS oscillator which is used to derive a master serial clock for configuration. The oscillator and the master serial clock run continuously in the configuration mode. The default value of the

Typical Building Block Function Performance¹**Pin-to-Pin Performance (LVCMOS25 12 mA Drive)**

Function	-5 Timing	Units
Basic Functions		
16-bit decoder	6.1	ns
32-bit decoder	7.3	ns
64-bit decoder	8.2	ns
4:1 MUX	4.9	ns
8:1 MUX	5.3	ns
16:1 MUX	5.7	ns
32:1 MUX	6.3	ns

Register to Register Performance

Function	-5 Timing	Units
Basic Functions		
16-bit decoder	351	MHz
32-bit decoder	248	MHz
64-bit decoder	237	MHz
4:1 MUX	590	MHz
8:1 MUX	523	MHz
16:1 MUX	434	MHz
32:1 MUX	355	MHz
8-bit adder	343	MHz
16-bit adder	292	MHz
64-bit adder	130	MHz
16-bit counter	388	MHz
32-bit counter	295	MHz
64-bit counter	200	MHz
64-bit accumulator	164	MHz
Embedded Memory Functions		
Single Port RAM 256x36 bits	254	MHz
True-Dual Port RAM 512x18 bits	254	MHz
Distributed Memory Functions		
16x2 SP RAM	434	MHz
64x2 SP RAM	332	MHz
128x4 SP RAM	235	MHz
32x2 PDP RAM	322	MHz
64x4 PDP RAM	291	MHz

1. These timing numbers were generated using the ispLEVER design tool. Exact performance may vary with design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Timing v.F0.11

sysCLOCK PLL Timing**Over Recommended Operating Conditions**

Parameter	Descriptions	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		25	—	375	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		25	—	375	MHz
f_{OUT2}	K-Divider Output Frequency (CLKOK)		0.195	—	187.5	MHz
f_{VCO}	PLL VCO Frequency		375	—	750	MHz
f_{PFD}	Phase Detector Input Frequency		25	—	—	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default duty cycle elected ³	45	50	55	%
t_{PH}^4	Output Phase Accuracy		—	—	0.05	UI
t_{OPJIT}^1	Output Clock Period Jitter	$f_{OUT} \geq 100\text{MHz}$	—	—	+/- 125	ps
		$f_{OUT} < 100\text{MHz}$	—	—	0.02	UIPP
t_{SK}	Input Clock to Output Clock Skew	Divider ratio = integer	—	—	+/- 200	ps
t_W	Output Clock Pulse Width	At 90% or 10% ³	1	—	—	ns
t_{LOCK}^2	PLL Lock-in Time		—	—	150	us
t_{PA}	Programmable Delay Unit		100	250	400	ps
t_{IPJIT}	Input Clock Period Jitter		—	—	+/- 200	ps
t_{FBKDLy}	External Feedback Delay		—	—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t_{RST}	RST Pulse Width		10	—	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

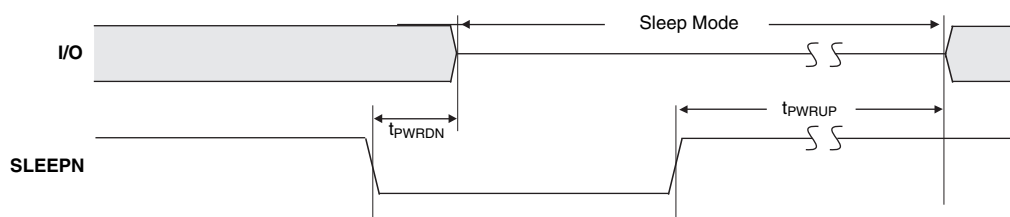
3. Using LVDS output buffers.

4. As compared to CLKOP output.

Timing v.F0.11

LatticeXP “C” Sleep Mode Timing

Parameter	Descriptions	Min.	Typ.	Max.	Units
t_{PWRDN}	SLEEPN Low to I/O Tristate	—	20	32	ns
t_{PWRUP}	SLEEPN High to Power Up	LFXP3	—	1.4	ms
		LFXP6	—	1.7	ms
		LFXP10	—	1.1	ms
		LFXP15	—	1.4	ms
		LFXP20	—	1.7	ms
$t_{WSLEEPN}$	SLEEPN Pulse Width to Initiate Sleep Mode	400	—	—	ns
t_{WAWAKE}	SLEEPN Pulse Rejection	—	—	120	ns



Flash Download Time

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{REFRESH}	PROGRAMN Low-to-High. Transition to Done High.	—	1.1	1.7	ms
	LFXP3	—	1.1	1.7	ms
	LFXP6	—	1.4	2.0	ms
	LFXP10	—	0.9	1.5	ms
	LFXP15	—	1.1	1.7	ms
	LFXP20	—	1.3	1.9	ms

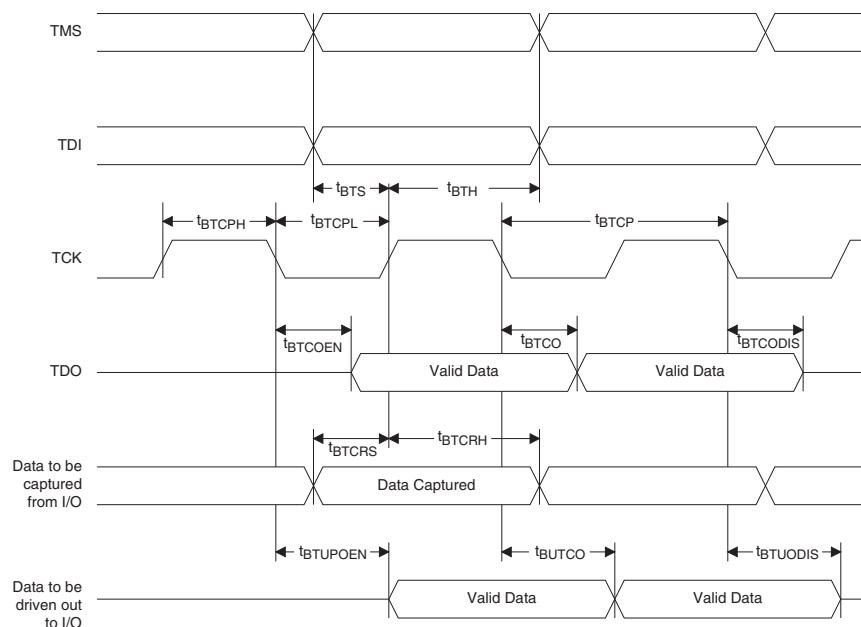
JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f_{MAX}		—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t_{BTCODIS}	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
t_{BTUODIS}	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
t_{BTUPOEN}	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Timing v.F0.11

Figure 3-12. JTAG Port Timing Waveforms



Pin Information Summary¹ (Cont.)

Pin Type		XP10		XP15			XP20		
		256 fpBGA	388 fpBGA	256 fpBGA	388 fpBGA	484 fpBGA	256 fpBGA	388 fpBGA	484 fpBGA
Single Ended User I/O		188	244	188	268	300	188	268	340
Differential Pair User I/O ²		76	104	76	112	128	76	112	144
Configuration	Dedicated	11	11	11	11	11	11	11	11
	Muxed	14	14	14	14	14	14	14	14
TAP		5	5	5	5	5	5	5	5
Dedicated (total without supplies)		6	6	6	6	6	6	6	6
V _{CC}		8	14	8	14	28	8	14	28
V _{CCAUX}		4	4	4	4	12	4	4	12
V _{CCPLL}		2	2	2	2	2	2	2	2
V _{CCIO}	Bank0	2	5	2	5	4	2	5	4
	Bank1	2	5	2	5	4	2	5	4
	Bank2	2	4	2	4	4	2	4	4
	Bank3	2	4	2	4	4	2	4	4
	Bank4	2	5	2	5	4	2	5	4
	Bank5	2	5	2	5	4	2	5	4
	Bank6	2	4	2	4	4	2	4	4
	Bank7	2	4	2	4	4	2	4	4
GND		24	50	24	50	56	24	50	56
GND _{PLL}		2	2	2	2	2	2	2	2
NC		0	24	0	0	40	0	0	0
Single Ended/ Differential I/O per Bank ²	Bank0	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank1	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank2	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank3	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank4	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank5	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank6	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank7	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
V _{CCJ}		1	1	1	1	1	1	1	1

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
2. The differential I/O per bank includes both dedicated LVDS and emulated LVDS pin pairs. Please see the Logic Signal Connections table for more information.

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
185	PT13A	0	T	CS1N	PT16A	0	T	CS1N
186	PT12B	0	C	PCLKC0_0	PT15B	0	C	PCLKC0_0
187	PT12A	0	T	PCLKT0_0	PT15A	0	T	PCLKT0_0
188	PT11B	0	C	-	PT14B	0	C	-
189	VCCIO0	0	-	-	VCCIO0	0	-	-
190	PT11A	0	T	DQS	PT14A	0	T	DQS
191	PT10B	0	-	-	PT13B	0	-	-
192	PT9A	0	-	DOUT	PT12A	0	-	DOUT
193	PT8B	0	C	-	PT11B	0	C	-
194	GNDIO0	0	-	-	GNDIO0	0	-	-
195	PT8A	0	T	WRITEN	PT11A	0	T	WRITEN
196	PT7B	0	C	-	PT10B	0	C	-
197	PT7A	0	T	VREF1_0	PT10A	0	T	VREF1_0
198	PT6B	0	C	-	PT9B	0	C	-
199	VCCIO0	0	-	-	VCCIO0	0	-	-
200	PT6A	0	T	DI	PT9A	0	T	DI
201	PT5B	0	C	-	PT8B	0	C	-
202	PT5A	0	T	CSN	PT8A	0	T	CSN
203	PT4B	0	C	-	PT7B	0	C	-
204	PT4A	0	T	-	PT7A	0	T	-
205	PT3B	0	-	VREF2_0	PT6B	0	-	VREF2_0
206	PT2B	0	-	-	PT5B	0	-	-
207	GND	-	-	-	GND	-	-	-
208	CFG0	0	-	-	CFG0	0	-	-

1. Applies to LFXP "C" only.
2. Applies to LFXP "E" only.
3. Supports dedicated LVDS outputs.

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP6				LFXP10			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
E16	TDO	-	-	-	TDO	-	-	-
D16	VCCJ	-	-	-	VCCJ	-	-	-
D14	TDI	-	-	-	TDI	-	-	-
C14	TMS	-	-	-	TMS	-	-	-
B14	TCK	-	-	-	TCK	-	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
A15	PT31B	1	C	-	PT35B	1	C	-
B15	PT31A	1	T	-	PT35A	1	T	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
D12	PT28A	1	-	VREF1_1	PT34B	1	C	VREF1_1
C11	PT30A	1	T	DQS	PT34A	1	T	DQS
A14	PT29B	1	-	-	PT33B	1	-	-
B13	PT30B	1	C	-	PT32A	1	-	-
F12	PT27B	1	C	-	PT31B	1	C	-
E11	PT27A	1	T	-	PT31A	1	T	-
A13	PT26B	1	C	-	PT30B	1	C	-
C13	PT26A	1	T	D0	PT30A	1	T	D0
-	GNDIO1	1	-	-	GNDIO1	1	-	-
C10	PT25B	1	C	D1	PT29B	1	C	D1
E10	PT25A	1	T	VREF2_1	PT29A	1	T	VREF2_1
A12	PT24B	1	C	-	PT28B	1	C	-
B12	PT24A	1	T	D2	PT28A	1	T	D2
C12	PT23B	1	C	D3	PT27B	1	C	D3
A11	PT23A	1	T	-	PT27A	1	T	-
B11	PT22B	1	C	-	PT26B	1	C	-
D11	PT22A	1	T	DQS	PT26A	1	T	DQS
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B9	PT21B	1	-	-	PT25B	1	-	-
D9	PT20A	1	-	D4	PT24A	1	-	D4
A10	PT19B	1	C	-	PT23B	1	C	-
B10	PT19A	1	T	D5	PT23A	1	T	D5
D10	PT18B	1	C	D6	PT22B	1	C	D6
A9	PT18A	1	T	-	PT22A	1	T	-
C9	PT17B	1	C	D7	PT21B	1	C	D7
C8	PT17A	1	T	-	PT21A	1	T	-
E9	PT16B	0	C	BUSY	PT20B	0	C	BUSY
-	GNDIO0	0	-	-	GNDIO0	0	-	-
B8	PT16A	0	T	CS1N	PT20A	0	T	CS1N
A8	PT15B	0	C	PCLKC0_0	PT19B	0	C	PCLKC0_0
A7	PT15A	0	T	PCLKT0_0	PT19A	0	T	PCLKT0_0
B7	PT14B	0	C	-	PT18B	0	C	-
C7	PT14A	0	T	DQS	PT18A	0	T	DQS

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
C2	PROGRAMN	7	-	-	PROGRAMN	7	-	-
C1	CCLK	7	-	-	CCLK	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
D2	PL7A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A
D3	PL7B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A
D1	PL9A	7	-	-	PL9A	7	-	-
E2	PL10B	7	-	VREF1_7	PL10B	7	-	VREF1_7
E1	PL11A	7	T ³	DQS	PL11A	7	T ³	DQS
F1	PL11B	7	C ³	-	PL11B	7	C ³	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
E3	PL12A	7	T	-	PL12A	7	T	-
F4	PL12B	7	C	-	PL12B	7	C	-
F3	PL13A	7	T ³	-	PL13A	7	T ³	-
F2	PL13B	7	C ³	-	PL13B	7	C ³	-
G1	PL15B	7	-	-	PL15B	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
G3	PL16A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A
G2	PL16B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A
H1	PL17A	7	T ³	-	PL17A	7	T ³	-
H2	PL17B	7	C ³	-	PL17B	7	C ³	-
G4	PL18A	7	-	VREF2_7	PL18A	7	-	VREF2_7
G5	PL19B	7	-	-	PL19B	7	-	-
J1	PL20A	7	T ³	DQS	PL20A	7	T ³	DQS
-	GNDIO7	7	-	-	GNDIO7	7	-	-
J2	PL20B	7	C ³	-	PL20B	7	C ³	-
H3	PL22A	7	T ³	-	PL22A	7	T ³	-
J3	PL22B	7	C ³	-	PL22B	7	C ³	-
H4	VCCP0	-	-	-	VCCP0	-	-	-
H5	GNDP0	-	-	-	GNDP0	-	-	-
K1	PL24A	6	T	PCLKT6_0	PL28A	6	T	PCLKT6_0
-	GNDIO6	6	-	-	GNDIO6	6	-	-
K2	PL24B	6	C	PCLKC6_0	PL28B	6	C	PCLKC6_0
J4	PL26A	6	-	-	PL30A	6	-	-
J5	PL27B	6	-	VREF1_6	PL31B	6	-	VREF1_6
L1	PL28A	6	T ³	DQS	PL32A	6	T ³	DQS
L2	PL28B	6	C ³	-	PL32B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
M1	PL29A	6	T	LLM0_PLLT_IN_A	PL33A	6	T	LLM0_PLLT_IN_A
M2	PL29B	6	C	LLM0_PLLC_IN_A	PL33B	6	C	LLM0_PLLC_IN_A
K3	PL30A	6	T ³	-	PL34A	6	T ³	-
L3	PL30B	6	C ³	-	PL34B	6	C ³	-

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L7	VCCIO5	5	-	-	VCCIO5	5	-	-
L8	VCCIO5	5	-	-	VCCIO5	5	-	-
J6	VCCIO6	6	-	-	VCCIO6	6	-	-
K6	VCCIO6	6	-	-	VCCIO6	6	-	-
G6	VCCIO7	7	-	-	VCCIO7	7	-	-
H6	VCCIO7	7	-	-	VCCIO7	7	-	-

1. Applies to LFXP "C" only.
2. Applies to LFXP "E" only.
3. Supports dedicated LVDS outputs.

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
AA20	PB36B	4	C	-	PB41B	4	C	-	PB45B	4	C	-
AB21	PB37A	4	T	-	PB42A	4	T	-	PB46A	4	T	-
AA21	PB37B	4	C	-	PB42B	4	C	-	PB46B	4	C	-
AA22	PB38A	4	T	-	PB43A	4	T	-	PB47A	4	T	-
Y21	PB38B	4	C	-	PB43B	4	C	-	PB47B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
W16	PB39A	4	-	-	PB44A	4	T	-	PB48A	4	T	-
W17	-	-	-	-	PB44B	4	C	-	PB48B	4	C	-
Y15	-	-	-	-	PB45A	4	-	-	PB49A	4	-	-
Y16	-	-	-	-	PB46B	4	-	-	PB50B	4	-	-
W19	-	-	-	-	PB47A	4	T	DQS	PB51A	4	T	DQS
W18	-	-	-	-	PB47B	4	C	-	PB51B	4	C	-
W20	-	-	-	-	PB48A	4	-	-	PB52A	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
T20	PR35B	3	C ³	-	PR39B	3	C ³	-	PR43B	3	C ³	-
T19	PR35A	3	T ³	-	PR39A	3	T ³	-	PR43A	3	T ³	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
U19	PR34B	3	C	RLM0_PLLC_FB_A	PR38B	3	C	RLM0_PLLC_FB_A	PR42B	3	C	RLM0_PLLC_FB_A
U20	PR34A	3	T	RLM0_PLLT_FB_A	PR38A	3	T	RLM0_PLLT_FB_A	PR42A	3	T	RLM0_PLLT_FB_A
V19	PR33B	3	C ³	-	PR37B	3	C ³	-	PR41B	3	C ³	-
V20	PR33A	3	T ³	DQS	PR37A	3	T ³	DQS	PR41A	3	T ³	DQS
R19	PR32B	3	-	-	PR36B	3	-	-	PR40B	3	-	-
R20	PR31A	3	-	VREF1_3	PR35A	3	-	VREF1_3	PR39A	3	-	VREF1_3
W21	PR30B	3	C ³	-	PR34B	3	C ³	-	PR38B	3	C ³	-
Y22	PR30A	3	T ³	-	PR34A	3	T ³	-	PR38A	3	T ³	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
P19	PR29B	3	C	-	PR33B	3	C	-	PR37B	3	C	-
P20	PR29A	3	T	-	PR33A	3	T	-	PR37A	3	T	-
V21	PR28B	3	C ³	-	PR32B	3	C ³	-	PR36B	3	C ³	-
W22	PR28A	3	T ³	-	PR32A	3	T ³	-	PR36A	3	T ³	-
U21	PR26B	3	C ³	-	PR30B	3	C ³	-	PR34B	3	C ³	-
V22	PR26A	3	T ³	-	PR30A	3	T ³	-	PR34A	3	T ³	-
T21	PR25B	3	C	RLM0_PLLC_IN_A	PR29B	3	C	RLM0_PLLC_IN_A	PR33B	3	C	RLM0_PLLC_IN_A
U22	PR25A	3	T	RLM0_PLLT_IN_A	PR29A	3	T	RLM0_PLLT_IN_A	PR33A	3	T	RLM0_PLLT_IN_A
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
R21	PR24B	3	C ³	-	PR28B	3	C ³	-	PR32B	3	C ³	-
T22	PR24A	3	T ³	DQS	PR28A	3	T ³	DQS	PR32A	3	T ³	DQS
N19	PR23B	3	-	-	PR27B	3	-	-	PR31B	3	-	-
N20	PR22A	3	-	VREF2_3	PR26A	3	-	VREF2_3	PR30A	3	-	VREF2_3
R22	PR21B	3	C ³	-	PR25B	3	C ³	-	PR29B	3	C ³	-
P22	PR21A	3	T ³	-	PR25A	3	T ³	-	PR29A	3	T ³	-
P21	PR20B	3	C	-	PR24B	3	C	-	PR28B	3	C	-
N21	PR20A	3	T	-	PR24A	3	T	-	PR28A	3	T	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
M20	PR19B	3	C ³	-	PR23B	3	C ³	-	PR27B	3	C ³	-
M19	PR19A	3	T ³	-	PR23A	3	T ³	-	PR27A	3	T ³	-
N22	GNDP1	-	-	-	GNDP1	-	-	-	GNDP1	-	-	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
A7	PT13A	0	T	DI	PT18A	0	T	DI	PT22A	0	T	DI
B7	PT12B	0	C	-	PT17B	0	C	-	PT21B	0	C	-
C6	PT12A	0	T	CSN	PT17A	0	T	CSN	PT21A	0	T	CSN
C10	PT11B	0	C	-	PT16B	0	C	-	PT20B	0	C	-
C9	PT11A	0	T	-	PT16A	0	T	-	PT20A	0	T	-
A6	PT10B	0	C	VREF2_0	PT15B	0	C	VREF2_0	PT19B	0	C	VREF2_0
B6	PT10A	0	T	DQS	PT15A	0	T	DQS	PT19A	0	T	DQS
A5	PT9B	0	-	-	PT14B	0	-	-	PT18B	0	-	-
B5	PT8A	0	-	-	PT13A	0	-	-	PT17A	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C5	PT7B	0	C	-	PT12B	0	C	-	PT16B	0	C	-
A4	PT7A	0	T	-	PT12A	0	T	-	PT16A	0	T	-
D9	PT6B	0	C	-	PT11B	0	C	-	PT15B	0	C	-
D8	PT6A	0	T	-	PT11A	0	T	-	PT15A	0	T	-
B4	PT5B	0	C	-	PT10B	0	C	-	PT14B	0	C	-
A2	PT5A	0	T	-	PT10A	0	T	-	PT14A	0	T	-
A3	PT4B	0	C	-	PT9B	0	C	-	PT13B	0	C	-
B3	PT4A	0	T	-	PT9A	0	T	-	PT13A	0	T	-
C4	PT3B	0	C	-	PT8B	0	C	-	PT12B	0	C	-
C3	PT3A	0	T	-	PT8A	0	T	-	PT12A	0	T	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C2	-	-	-	-	PT7B	0	C	-	PT11B	0	C	-
D3	PT2A	0	-	-	PT7A	0	T	DQS	PT11A	0	T	DQS
D7	-	-	-	-	PT6B	0	-	-	PT10B	0	-	-
D6	-	-	-	-	PT5A	0	-	-	PT9A	0	-	-
E4	-	-	-	-	PT4B	0	C	-	PT8B	0	C	-
D4	-	-	-	-	PT4A	0	T	-	PT8A	0	T	-
D5	-	-	-	-	PT3B	0	-	-	PT7B	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C1	CFG0	0	-	-	CFG0	0	-	-	CFG0	0	-	-
B2	CFG1	0	-	-	CFG1	0	-	-	CFG1	0	-	-
B1	DONE	0	-	-	DONE	0	-	-	DONE	0	-	-
A1	GND	-	-	-	GND	-	-	-	GND	-	-	-
A22	GND	-	-	-	GND	-	-	-	GND	-	-	-
AB1	GND	-	-	-	GND	-	-	-	GND	-	-	-
AB22	GND	-	-	-	GND	-	-	-	GND	-	-	-
H10	GND	-	-	-	GND	-	-	-	GND	-	-	-
H11	GND	-	-	-	GND	-	-	-	GND	-	-	-
H12	GND	-	-	-	GND	-	-	-	GND	-	-	-
H13	GND	-	-	-	GND	-	-	-	GND	-	-	-
H14	GND	-	-	-	GND	-	-	-	GND	-	-	-
J10	GND	-	-	-	GND	-	-	-	GND	-	-	-
J11	GND	-	-	-	GND	-	-	-	GND	-	-	-
J12	GND	-	-	-	GND	-	-	-	GND	-	-	-
J13	GND	-	-	-	GND	-	-	-	GND	-	-	-
J14	GND	-	-	-	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-	GND	-	-	-
K10	GND	-	-	-	GND	-	-	-	GND	-	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
D18	-	-	-	-	PT55B	1	C	-
E18	-	-	-	-	PT55A	1	T	-
C19	-	-	-	-	PT54B	1	C	-
C18	-	-	-	-	PT54A	1	T	-
C21	-	-	-	-	PT53B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B21	-	-	-	-	PT53A	1	T	-
E17	PT48B	1	C	-	PT52B	1	C	-
E16	PT48A	1	T	-	PT52A	1	T	-
C17	PT47B	1	C	-	PT51B	1	C	-
D17	PT47A	1	T	DQS	PT51A	1	T	DQS
F17	PT46B	1	-	-	PT50B	1	-	-
F16	PT45A	1	-	-	PT49A	1	-	-
C16	PT44B	1	C	-	PT48B	1	C	-
D16	PT44A	1	T	-	PT48A	1	T	-
A20	PT43B	1	C	-	PT47B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B20	PT43A	1	T	-	PT47A	1	T	-
A19	PT42B	1	C	-	PT46B	1	C	-
B19	PT42A	1	T	-	PT46A	1	T	-
C15	PT41B	1	C	-	PT45B	1	C	-
D15	PT41A	1	T	-	PT45A	1	T	-
A18	PT40B	1	C	-	PT44B	1	C	-
B18	PT40A	1	T	-	PT44A	1	T	-
F15	PT39B	1	C	VREF1_1	PT43B	1	C	VREF1_1
-	GNDIO1	1	-	-	GNDIO1	1	-	-
E15	PT39A	1	T	DQS	PT43A	1	T	DQS
A17	PT38B	1	-	-	PT42B	1	-	-
B17	PT37A	1	-	-	PT41A	1	-	-
E14	PT36B	1	C	-	PT40B	1	C	-
F14	PT36A	1	T	-	PT40A	1	T	-
D14	PT35B	1	C	-	PT39B	1	C	-
C14	PT35A	1	T	D0	PT39A	1	T	D0
A16	PT34B	1	C	D1	PT38B	1	C	D1
B16	PT34A	1	T	VREF2_1	PT38A	1	T	VREF2_1
A15	PT33B	1	C	-	PT37B	1	C	-
B15	PT33A	1	T	D2	PT37A	1	T	D2
-	GNDIO1	1	-	-	GNDIO1	1	-	-
E13	PT32B	1	C	D3	PT36B	1	C	D3
D13	PT32A	1	T	-	PT36A	1	T	-
C13	PT31B	1	C	-	PT35B	1	C	-
B13	PT31A	1	T	DQS	PT35A	1	T	DQS

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
A14	PT30B	1	-	-	PT34B	1	-	-
B14	PT29A	1	-	D4	PT33A	1	-	D4
C12	PT28B	1	C	-	PT32B	1	C	-
B12	PT28A	1	T	D5	PT32A	1	T	D5
-	GNDIO1	1	-	-	GNDIO1	1	-	-
D12	PT27B	1	C	D6	PT31B	1	C	D6
E12	PT27A	1	T	-	PT31A	1	T	-
A13	PT26B	1	C	D7	PT30B	1	C	D7
A12	PT26A	1	T	-	PT30A	1	T	-
A11	PT25B	0	C	BUSY	PT29B	0	C	BUSY
-	GNDIO0	0	-	-	GNDIO0	0	-	-
A10	PT25A	0	T	CS1N	PT29A	0	T	CS1N
D11	PT24B	0	C	PCLKC0_0	PT28B	0	C	PCLKC0_0
E11	PT24A	0	T	PCLKT0_0	PT28A	0	T	PCLKT0_0
B11	PT23B	0	C	-	PT27B	0	C	-
C11	PT23A	0	T	DQS	PT27A	0	T	DQS
B9	PT22B	0	-	-	PT26B	0	-	-
A9	PT21A	0	-	DOUT	PT25A	0	-	DOUT
B8	PT20B	0	C	-	PT24B	0	C	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
A8	PT20A	0	T	WRITEN	PT24A	0	T	WRITEN
E10	PT19B	0	C	-	PT23B	0	C	-
D10	PT19A	0	T	VREF1_0	PT23A	0	T	VREF1_0
C10	PT18B	0	C	-	PT22B	0	C	-
B10	PT18A	0	T	DI	PT22A	0	T	DI
B7	PT17B	0	C	-	PT21B	0	C	-
A7	PT17A	0	T	CSN	PT21A	0	T	CSN
C9	PT16B	0	C	-	PT20B	0	C	-
D9	PT16A	0	T	-	PT20A	0	T	-
B6	PT15B	0	C	VREF2_0	PT19B	0	C	VREF2_0
A6	PT15A	0	T	DQS	PT19A	0	T	DQS
F9	PT14B	0	-	-	PT18B	0	-	-
E9	PT13A	0	-	-	PT17A	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
B5	PT12B	0	C	-	PT16B	0	C	-
A5	PT12A	0	T	-	PT16A	0	T	-
C8	PT11B	0	C	-	PT15B	0	C	-
D8	PT11A	0	T	-	PT15A	0	T	-
B4	PT10B	0	C	-	PT14B	0	C	-
A4	PT10A	0	T	-	PT14A	0	T	-
F8	PT9B	0	C	-	PT13B	0	C	-
E8	PT9A	0	T	-	PT13A	0	T	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
H13	VCCIO1	1	-	-	VCCIO1	1	-	-
K15	VCCIO2	2	-	-	VCCIO2	2	-	-
L15	VCCIO2	2	-	-	VCCIO2	2	-	-
L16	VCCIO2	2	-	-	VCCIO2	2	-	-
L17	VCCIO2	2	-	-	VCCIO2	2	-	-
M15	VCCIO3	3	-	-	VCCIO3	3	-	-
M16	VCCIO3	3	-	-	VCCIO3	3	-	-
M17	VCCIO3	3	-	-	VCCIO3	3	-	-
N15	VCCIO3	3	-	-	VCCIO3	3	-	-
R12	VCCIO4	4	-	-	VCCIO4	4	-	-
R13	VCCIO4	4	-	-	VCCIO4	4	-	-
T12	VCCIO4	4	-	-	VCCIO4	4	-	-
U12	VCCIO4	4	-	-	VCCIO4	4	-	-
R10	VCCIO5	5	-	-	VCCIO5	5	-	-
R11	VCCIO5	5	-	-	VCCIO5	5	-	-
T11	VCCIO5	5	-	-	VCCIO5	5	-	-
U11	VCCIO5	5	-	-	VCCIO5	5	-	-
M6	VCCIO6	6	-	-	VCCIO6	6	-	-
M7	VCCIO6	6	-	-	VCCIO6	6	-	-
M8	VCCIO6	6	-	-	VCCIO6	6	-	-
N8	VCCIO6	6	-	-	VCCIO6	6	-	-
K8	VCCIO7	7	-	-	VCCIO7	7	-	-
L6	VCCIO7	7	-	-	VCCIO7	7	-	-
L7	VCCIO7	7	-	-	VCCIO7	7	-	-
L8	VCCIO7	7	-	-	VCCIO7	7	-	-

1. Applies to LFXP "C" only.

2. Applies to LFXP "E" only.

3. Supports dedicated LVDS outputs.

Conventional Packaging**Commercial**

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3C-3Q208C	136	1.8/2.5/3.3V	-3	PQFP	208	COM	3.1K
LFXP3C-4Q208C	136	1.8/2.5/3.3V	-4	PQFP	208	COM	3.1K
LFXP3C-5Q208C	136	1.8/2.5/3.3V	-5	PQFP	208	COM	3.1K
LFXP3C-3T144C	100	1.8/2.5/3.3V	-3	TQFP	144	COM	3.1K
LFXP3C-4T144C	100	1.8/2.5/3.3V	-4	TQFP	144	COM	3.1K
LFXP3C-5T144C	100	1.8/2.5/3.3V	-5	TQFP	144	COM	3.1K
LFXP3C-3T100C	62	1.8/2.5/3.3V	-3	TQFP	100	COM	3.1K
LFXP3C-4T100C	62	1.8/2.5/3.3V	-4	TQFP	100	COM	3.1K
LFXP3C-5T100C	62	1.8/2.5/3.3V	-5	TQFP	100	COM	3.1K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6C-3F256C	188	1.8/2.5/3.3V	-3	fpBGA	256	COM	5.8K
LFXP6C-4F256C	188	1.8/2.5/3.3V	-4	fpBGA	256	COM	5.8K
LFXP6C-5F256C	188	1.8/2.5/3.3V	-5	fpBGA	256	COM	5.8K
LFXP6C-3Q208C	142	1.8/2.5/3.3V	-3	PQFP	208	COM	5.8K
LFXP6C-4Q208C	142	1.8/2.5/3.3V	-4	PQFP	208	COM	5.8K
LFXP6C-5Q208C	142	1.8/2.5/3.3V	-5	PQFP	208	COM	5.8K
LFXP6C-3T144C	100	1.8/2.5/3.3V	-3	TQFP	144	COM	5.8K
LFXP6C-4T144C	100	1.8/2.5/3.3V	-4	TQFP	144	COM	5.8K
LFXP6C-5T144C	100	1.8/2.5/3.3V	-5	TQFP	144	COM	5.8K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10C-3F388C	244	1.8/2.5/3.3V	-3	fpBGA	388	COM	9.7K
LFXP10C-4F388C	244	1.8/2.5/3.3V	-4	fpBGA	388	COM	9.7K
LFXP10C-5F388C	244	1.8/2.5/3.3V	-5	fpBGA	388	COM	9.7K
LFXP10C-3F256C	188	1.8/2.5/3.3V	-3	fpBGA	256	COM	9.7K
LFXP10C-4F256C	188	1.8/2.5/3.3V	-4	fpBGA	256	COM	9.7K
LFXP10C-5F256C	188	1.8/2.5/3.3V	-5	fpBGA	256	COM	9.7K

Revision History

Date	Version	Section	Change Summary
February 2005	01.0	—	Initial release.
April 2005	01.1	Architecture	EBR memory support section updated with clarification.
May 2005	01.2	Introduction	Added TransFR Reconfiguration to Features section.
		Architecture	Added TransFR section.
June 2005	01.3	Pinout Information	Added pinout information for LFXP3, LFXP6, LFXP15 and LFXP20.
July 2005	02.0	Introduction	Updated XP6, XP15 and XP20 EBR SRAM Bits and Block numbers.
		Architecture	Updated Per Quadrant Primary Clock Selection figure.
			Added Typical I/O Behavior During Power-up section.
			Updated Device Configuration section under Configuration and Testing.
		DC and Switching Characteristics	Clarified Hot Socketing Specification
			Updated Supply Current (Standby) Table
			Updated Initialization Supply Current Table
			Added Programming and Erase Flash Supply Current table
			Added LVDS Emulation section. Updated LVDS25E Output Termination Example figure and LVDS25E DC Conditions table.
			Updated Differential LVPECL diagram and LVPECL DC Conditions table.
			Deleted 5V Tolerant Input Buffer section. Updated RSDS figure and RSDS DC Conditions table.
			Updated sysCONFIG Port Timing Specifications
			Updated JTAG Port Timing Specifications. Added Flash Download Time table.
		Pinout Information	Updated Signal Descriptions table.
			Updated Logic Signal Connections Dual Function column.
		Ordering Information	Added lead-free ordering part numbers.
July 2005	02.1	DC and Switching Characteristics	Clarification of Flash Programming Junction Temperature
August 2005	02.2	Introduction	Added Sleep Mode feature.
		Architecture	Added Sleep Mode section.
		DC and Switching Characteristics	Added Sleep Mode Supply Current Table
			Added Sleep Mode Timing section
		Pinout Information	Added SLEEPN and TOE signal names, descriptions and footnotes.
			Added SLEEPN and TOE to pinout information and footnotes.
September 2005	03.0	Architecture	Added footnote 3 to Logic Signal Connections tables for clarification on emulated LVDS output.
			Added clarification of PCI clamp.
		DC and Switching Characteristics	Added clarification to SLEEPN Pin Characteristics section.
			DC Characteristics, added footnote 4 for clarification. Updated Supply Current (Sleep Mode), Supply Current (Standby), Initialization Supply Current, and Programming and Erase Flash Supply Current typical numbers.