Lattice Semiconductor Corporation - LFXP10C-3FN256C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10000
Total RAM Bits	221184
Number of I/O	188
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp10c-3fn256c

Slice

Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from adjacent slice or PFU). There are 7 outputs: 6 to routing and one to carry-chain (to adjacent PFU). Table 2-1 lists the signals associated with each slice.

Figure 2-3. Slice Diagram

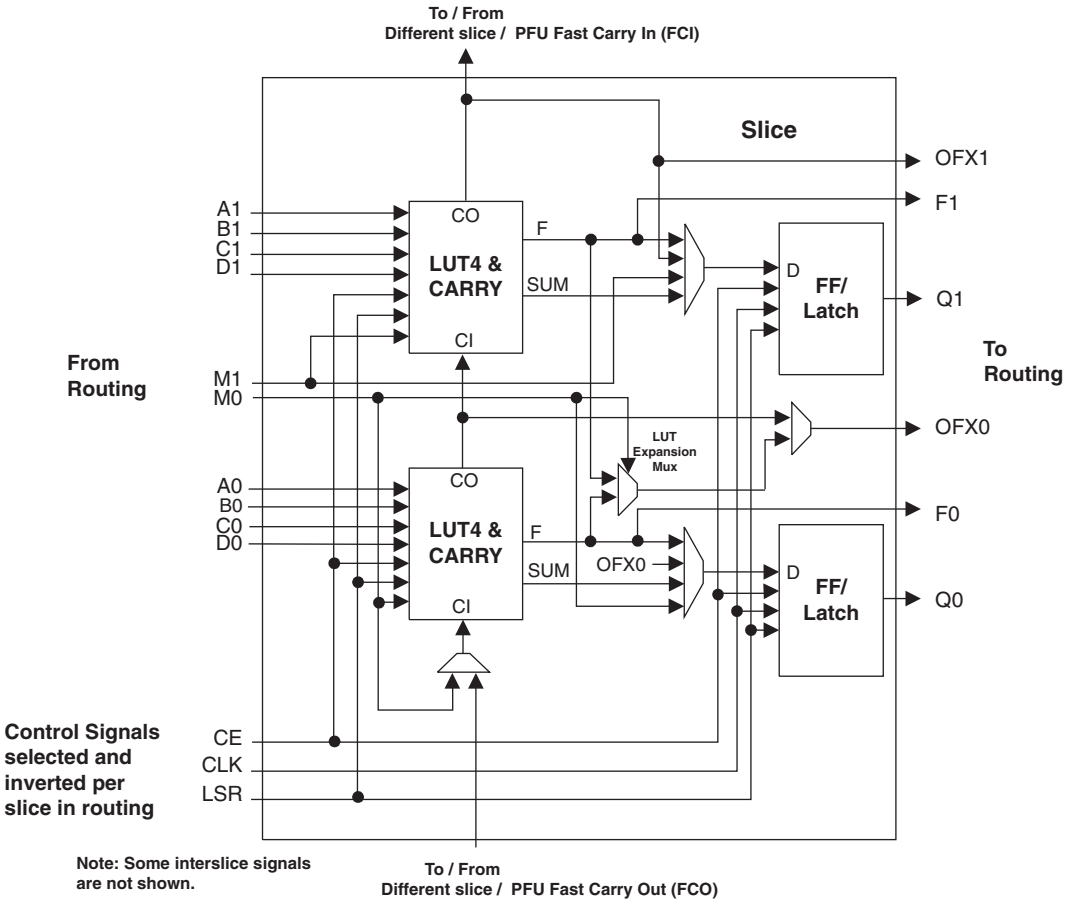


Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output[1]

1. See Figure 2-2 for connection details.
2. Requires two PFUs.

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SP 16x2	ROM 16x1 x 2
PFF Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	N/A	ROM 16x1 x 2

Logic Mode: In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other Slices.

Ripple Mode: Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two additional signals: Carry Generate and Carry Propagate are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode: In this mode, distributed RAM can be constructed using each LUT block as a 16x1-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved irrespective of where the select signal is toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-12 illustrates the DCS Block Macro.

Figure 2-12. DCS Block Primitive

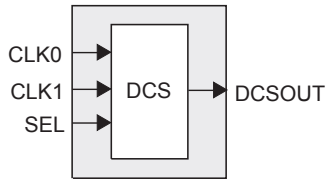
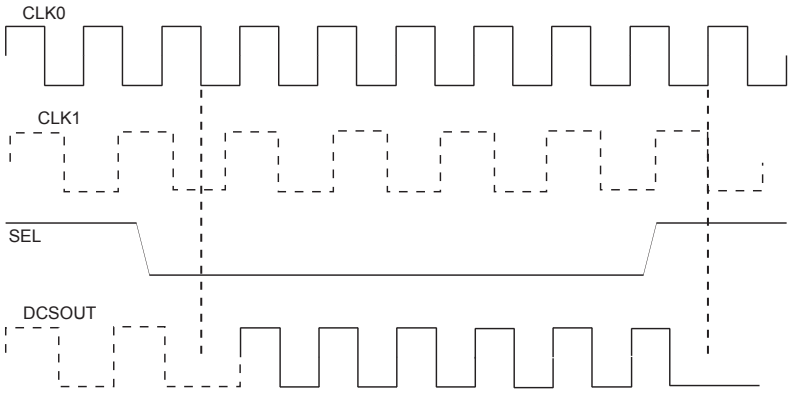


Figure 2-13 shows timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information on the DCS, please see details of additional technical documentation at the end of this data sheet.

Figure 2-13. DCS Waveforms



sysMEM Memory

The LatticeXP family of devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-6.

Figure 2-21. Input Register DDR Waveforms

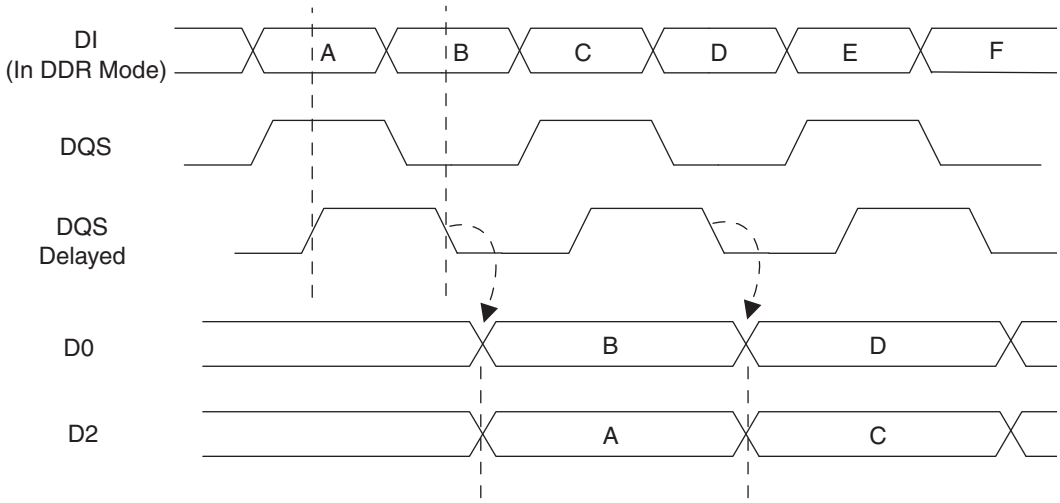
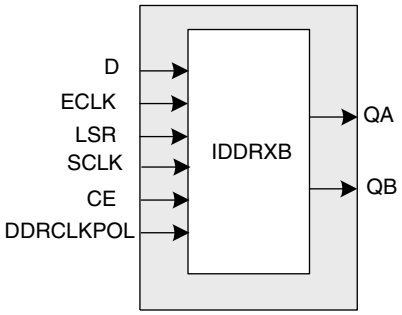


Figure 2-22. INDDRXB Primitive



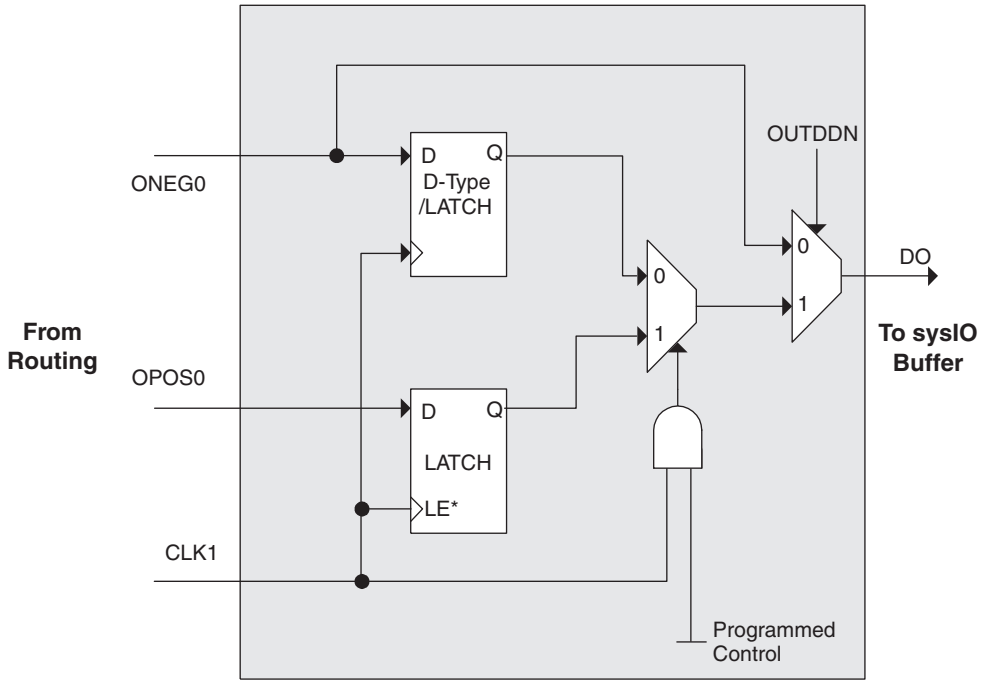
Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-23 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or as a latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

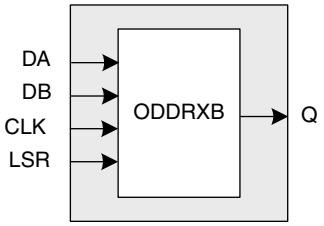
Figure 2-24 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

Figure 2-23. Output Register Block



*Latch is transparent when input is low.

Figure 2-24. ODDRXB Primitive



Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-25 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 3-2. BLVDS Multi-point Output Example

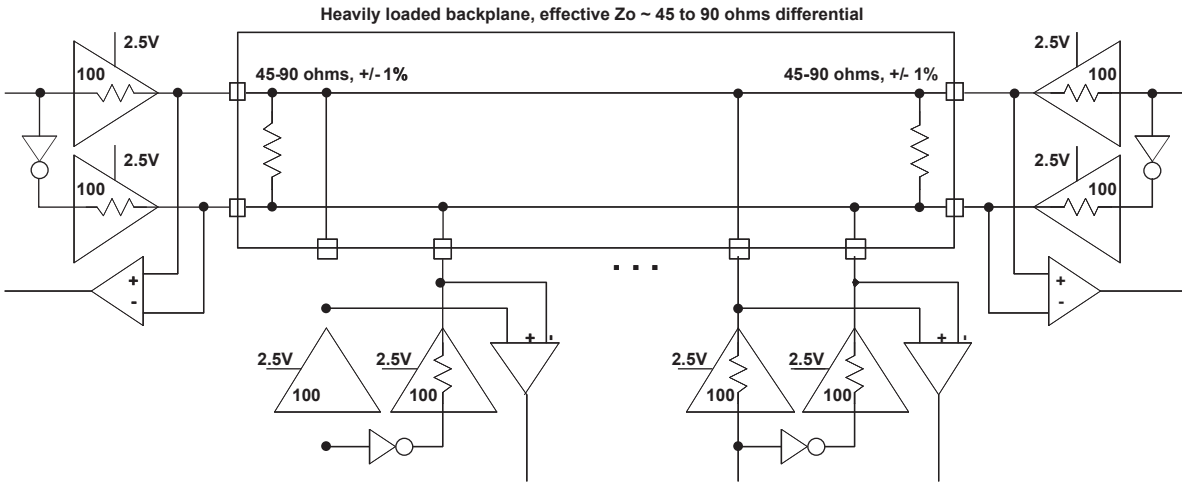


Table 3-2. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Typical		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	100	100	ohms
R_{TLEFT}	Left end termination	45	90	ohms
R_{TRIGHT}	Right end termination	45	90	ohms
V_{OH}	Output high voltage	1.375	1.48	V
V_{OL}	Output low voltage	1.125	1.02	V
V_{OD}	Output differential voltage	0.25	0.46	V
V_{CM}	Output common mode voltage	1.25	1.25	V
I_{DC}	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

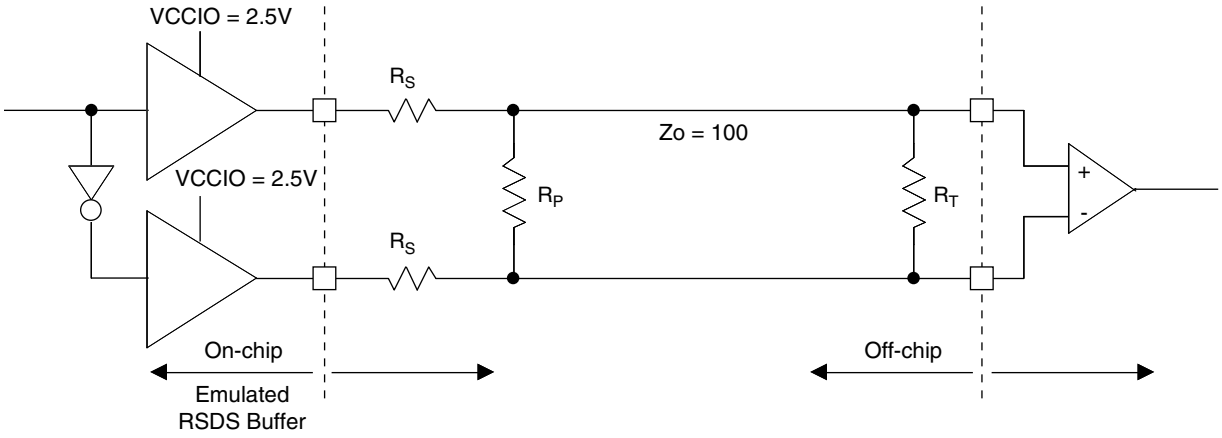


Table 3-4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	ohms
R_S	Driver series resistor	300	ohms
R_P	Driver parallel resistor	121	ohms
R_T	Receiver termination	100	ohms
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	ohms
I_{DC}	DC output current	3.66	mA

Typical Building Block Function Performance[1]

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	-5 Timing	Units
Basic Functions		
16-bit decoder	6.1	ns
32-bit decoder	7.3	ns
64-bit decoder	8.2	ns
4:1 MUX	4.9	ns
8:1 MUX	5.3	ns
16:1 MUX	5.7	ns
32:1 MUX	6.3	ns

Register to Register Performance

Function	-5 Timing	Units
Basic Functions		
16-bit decoder	351	MHz
32-bit decoder	248	MHz
64-bit decoder	237	MHz
4:1 MUX	590	MHz
8:1 MUX	523	MHz
16:1 MUX	434	MHz
32:1 MUX	355	MHz
8-bit adder	343	MHz
16-bit adder	292	MHz
64-bit adder	130	MHz
16-bit counter	388	MHz
32-bit counter	295	MHz
64-bit counter	200	MHz
64-bit accumulator	164	MHz
Embedded Memory Functions		
Single Port RAM 256x36 bits	254	MHz
True-Dual Port RAM 512x18 bits	254	MHz
Distributed Memory Functions		
16x2 SP RAM	434	MHz
64x2 SP RAM	332	MHz
128x4 SP RAM	235	MHz
32x2 PDP RAM	322	MHz
64x4 PDP RAM	291	MHz

1. These timing numbers were generated using the ispLEVER design tool. Exact performance may vary with design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Timing v.F0.11

Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions
Test and Programming (Dedicated pins. Pull-up is enabled on input pins during configuration.)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data in pin, used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence).
TDO	O	Output pin -Test Data out pin used to shift data out of device using 1149.1.
V_{CCJ}	—	V_{CCJ} - The power supply pin for JTAG Test Access Port.
Configuration Pads (used during sysCONFIG)		
CFG[1:0]	I	Mode pins used to specify configuration modes values latched on rising edge of INITN. During configuration, a pull-up is enabled.
INITN	I/O	Open Drain pin - Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. If CFG1 and CFG0 are high (SDM) then this pin is pulled low.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
DONE	I/O	Open Drain pin - Indicates that the configuration sequence is complete, and the startup sequence is in progress.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
BUSY	I/O	Generally not used. After configuration it is a user-programmable I/O pin.
CSN	I	sysCONFIG chip select (Active low). During configuration, a pull-up is enabled. After configuration it is user a programmable I/O pin.
CS1N	I	sysCONFIG chip select (Active Low). During configuration, a pull-up is enabled. After configuration it is user programmable I/O pin
WRITEN	I	Write Data on Parallel port (Active low). After configuration it is a user programmable I/O pin
D[7:0]	I/O	sysCONFIG Port Data I/O. After configuration these are user programmable I/O pins.
DOUT, CSON	O	Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port. After configuration, it is a user-programmable I/O pin.
DI	I	Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. After configuration it is a user-programmable I/O pin.
SLEEPN[2]	I	Sleep Mode pin - Active low sleep pin.þ When this pin is held high, the device operates normally.þ When driven low, the device moves into Sleep Mode after a specified time.This pin has a weak internal pull-up, but when not used an external pull-up to V_{CC} is recommended.
TOE[3]	I	Test Output Enable tri-states all I/O pins when driven low. This pin has a weak internal pull-up, but when not used an external pull-up to V_{CC} is recommended.

1. Applies toþ LFXP10, LFXP15 and LFXP20 only.
2. Applies to LFXP “C” devices only.
3. Applies to LFXP “E” devices only.

PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO within PIC	Polarity	DDR Strobe (DQS) and Data (DQ) Pins
P[Edge] [n-4]	A	True	DQ
	B	Complement	DQ
P[Edge] [n-3]	A	True	DQ
	B	Complement	DQ
P[Edge] [n-2]	A	True	DQ
	B	Complement	DQ
P[Edge] [n-1]	A	True	DQ
P[Edge] [n]			
	B	Complement	DQ
P[Edge] [n+1]	A	True	[Edge]DQSn
	B	Complement	DQ
P[Edge] [n+2]	A	True	DQ
	B	Complement	DQ
P[Edge] [n+3]	A	True	DQ
	B	Complement	DQ

Notes:
1. “n” is a row/column PIC number.
2. The DDR interface is designed for memories that support one DQS strobe per eight bits of data. In some packages, all the potential DDR data (DQ) pins may not be available.
3. The definition of the PIC numbering is provided in the Signal Names column of the Signal Descriptions table in this data sheet.

Pin Information Summary[1]

Pin Type		XP3			XP6		
		100 TQFP	144 TQFP	208 PQFP	144 TQFP	208 PQFP	256 fpBGA
Single Ended User I/O		62	100	136	100	142	188
Differential Pair User I/O[2]		19	35	56	35	58	80
Configuration	Dedicated	11	11	11	11	11	11
	Muxed	14	14	14	14	14	14
TAP		5	5	5	5	5	5
Dedicated (total without supplies)		6	6	6	6	6	6
V_{CC}		2	4	8	4	8	8
V_{CCAUX}		2	2	2	2	2	4
V_{CCPLL}		2	2	2	2	2	2
V_{CCIO}	Bank0	1	1	2	1	2	2
	Bank1	1	1	2	1	2	2
	Bank2	1	1	2	1	2	2
	Bank3	1	1	2	1	2	2
	Bank4	1	2	2	2	2	2
	Bank5	1	1	2	1	2	2
	Bank6	1	1	2	1	2	2
	Bank7	1	1	2	1	2	2
GND		10	13	24	13	24	24
GND_{PLL}		2	2	2	2	2	2
NC		0	0	6	0	0	0
Single Ended/Differential I/O per Bank[2]	Bank0	8/2	12/3	20/8	12/3	20/8	26/11
	Bank1	9/0	12/2	18/6	12/2	18/6	26/11
	Bank2	8/3	12/5	14/6	12/5	17/7	21/9
	Bank3	6/2	13/5	14/6	13/5	14/6	21/9
	Bank4	5/2	14/6	21/9	14/6	21/9	26/11
	Bank5	12/4	12/4	21/9	12/4	21/9	26/11
	Bank6	4/2	13/5	14/6	13/5	17/7	21/9
	Bank7	10/4	12/5	14/6	12/5	14/6	21/9
V_{CCJ}		1	1	1	1	1	1

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
2. The differential I/O per bank includes both dedicated LVDS and emulated LVDS pin pairs. Please see the Logic Signal Connections table for more information.

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP6				LFXP10			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
R8	PB16A	5	T	-	PB20A	5	T	-
T9	PB16B	5	C	-	PB20B	5	C	-
R9	PB17A	4	T	-	PB21A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
P9	PB17B	4	C	-	PB21B	4	C	-
T10	PB18A	4	T	PCLKT4_0	PB22A	4	T	PCLKT4_0
T11	PB18B	4	C	PCLKC4_0	PB22B	4	C	PCLKC4_0
R10	PB19A	4	T	-	PB23A	4	T	-
P10	PB19B	4	C	-	PB23B	4	C	-
N9	PB20A	4	-	-	PB24A	4	-	-
M9	PB21B	4	-	-	PB25B	4	-	-
R12	PB22A	4	T	DQS	PB26A	4	T	DQS
-	GNDIO4	4	-	-	GNDIO4	4	-	-
T12	PB22B	4	C	VREF1_4	PB26B	4	C	VREF1_4
P13	PB23A	4	T	-	PB27A	4	T	-
R13	PB23B	4	C	-	PB27B	4	C	-
M11	PB24A	4	T	-	PB28A	4	T	-
N11	PB24B	4	C	-	PB28B	4	C	-
N10	PB25A	4	T	-	PB29A	4	T	-
M10	PB25B	4	C	-	PB29B	4	C	-
T13	PB26A	4	T	-	PB30A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
P14	PB26B	4	C	-	PB30B	4	C	-
R11	PB27A	4	T	VREF2_4	PB31A	4	T	VREF2_4
P12	PB27B	4	C	-	PB31B	4	C	-
T14	PB28A	4	-	-	PB32A	4	-	-
R14	PB29B	4	-	-	PB33B	4	-	-
P11	PB30A	4	T	DQS	PB34A	4	T	DQS
N12	PB30B	4	C	-	PB34B	4	C	-
T15	PB31A	4	T	-	PB35A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
R15	PB31B	4	C	-	PB35B	4	C	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
P15	PR26B	3	C[3]	-	PR34B	3	C	RLM0_PLLC_FB_A
N15	PR26A	3	T[3]	-	PR34A	3	T	RLM0_PLLT_FB_A
P16	PR24B	3	C[3]	-	PR33B	3	C[3]	-
R16	PR24A	3	T[3]	DQS	PR33A	3	T[3]	DQS
M15	PR15B	3	-	-	PR32B	3	-	-
N14	PR23B	3	-	VREF1_3	PR31A	3	-	VREF1_3
-	GNDIO3	3	-	-	GNDIO3	3	-	-
M14	PR25B	3	C	-	PR29B	3	C	-
L13	PR25A	3	T	-	PR29A	3	T	-

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L4	PL32A	6	-	-	PL36A	6	-	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
K4	PL33A	6	T	-	PL37A	6	T	-
K5	PL33B	6	C	-	PL37B	6	C	-
N1	PL35A	6	-	VREF2_6	PL39A	6	-	VREF2_6
N2	PL36B	6	-	-	PL40B	6	-	-
P1	PL37A	6	T[3]	DQS	PL41A	6	T[3]	DQS
P2	PL37B	6	C[3]	-	PL41B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
L5	PL38A	6	T	LLM0_PLLT_FB_A	PL42A	6	T	LLM0_PLLT_FB_A
M6	PL38B	6	C	LLM0_PLLC_FB_A	PL42B	6	C	LLM0_PLLC_FB_A
M3	PL39A	6	T[3]	-	PL43A	6	T[3]	-
N3	PL39B	6	C[3]	-	PL43B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
P4	SLEEPN[1]/TOE[2]	-	-	-	SLEEPN[1]/TOE[2]	-	-	-
P3	INITN	5	-	-	INITN	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
R4	PB11A	5	T	-	PB15A	5	T	-
N5	PB11B	5	C	-	PB15B	5	C	-
P5	PB12A	5	T	VREF1_5	PB16A	5	T	VREF1_5
-	GNDIO5	5	-	-	GNDIO5	5	-	-
R1	PB12B	5	C	-	PB16B	5	C	-
N6	PB13A	5	-	-	PB17A	5	-	-
M7	PB14B	5	-	-	PB18B	5	-	-
R2	PB15A	5	T	DQS	PB19A	5	T	DQS
T2	PB15B	5	C	-	PB19B	5	C	-
R3	PB16A	5	T	-	PB20A	5	T	-
T3	PB16B	5	C	-	PB20B	5	C	-
T4	PB17A	5	T	-	PB21A	5	T	-
R5	PB17B	5	C	VREF2_5	PB21B	5	C	VREF2_5
N7	PB18A	5	T	-	PB22A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
M8	PB18B	5	C	-	PB22B	5	C	-
T5	PB19A	5	T	-	PB23A	5	T	-
P6	PB19B	5	C	-	PB23B	5	C	-
T6	PB20A	5	T	-	PB24A	5	T	-
R6	PB20B	5	C	-	PB24B	5	C	-
P7	PB21A	5	-	-	PB25A	5	-	-
N8	PB22B	5	-	-	PB26B	5	-	-
R7	PB23A	5	T	DQS	PB27A	5	T	DQS

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
-	GNDIO2	2	-	-	GNDIO2	2	-	-
F15	PR10B	2	-	-	PR10B	2	-	-
E15	PR9A	2	-	VREF2_2	PR9A	2	-	VREF2_2
F14	PR8B	2	C[3]	-	PR8B	2	C[3]	-
E14	PR8A	2	T[3]	-	PR8A	2	T[3]	-
D15	PR7B	2	C	RUM0_PLLC_FB_A	PR7B	2	C	RUM0_PLLC_FB_A
C15	PR7A	2	T	RUM0_PLLT_FB_A	PR7A	2	T	RUM0_PLLT_FB_A
-	GNDIO2	2	-	-	GNDIO2	2	-	-
E16	TDO	-	-	-	TDO	-	-	-
D16	VCCJ	-	-	-	VCCJ	-	-	-
D14	TDI	-	-	-	TDI	-	-	-
C14	TMS	-	-	-	TMS	-	-	-
B14	TCK	-	-	-	TCK	-	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
A15	PT40B	1	C	-	PT44B	1	C	-
B15	PT40A	1	T	-	PT44A	1	T	-
D12	PT39B	1	C	VREF1_1	PT43B	1	C	VREF1_1
-	GNDIO1	1	-	-	GNDIO1	1	-	-
C11	PT39A	1	T	DQS	PT43A	1	T	DQS
A14	PT38B	1	-	-	PT42B	1	-	-
B13	PT37A	1	-	-	PT41A	1	-	-
F12	PT36B	1	C	-	PT40B	1	C	-
E11	PT36A	1	T	-	PT40A	1	T	-
A13	PT35B	1	C	-	PT39B	1	C	-
C13	PT35A	1	T	D0	PT39A	1	T	D0
C10	PT34B	1	C	D1	PT38B	1	C	D1
E10	PT34A	1	T	VREF2_1	PT38A	1	T	VREF2_1
A12	PT33B	1	C	-	PT37B	1	C	-
B12	PT33A	1	T	D2	PT37A	1	T	D2
-	GNDIO1	1	-	-	GNDIO1	1	-	-
C12	PT32B	1	C	D3	PT36B	1	C	D3
A11	PT32A	1	T	-	PT36A	1	T	-
B11	PT31B	1	C	-	PT35B	1	C	-
D11	PT31A	1	T	DQS	PT35A	1	T	DQS
B9	PT30B	1	-	-	PT34B	1	-	-
D9	PT29A	1	-	D4	PT33A	1	-	D4
A10	PT28B	1	C	-	PT32B	1	C	-
B10	PT28A	1	T	D5	PT32A	1	T	D5
-	GNDIO1	1	-	-	GNDIO1	1	-	-
D10	PT27B	1	C	D6	PT31B	1	C	D6

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
Y10	PB11B	5	C	-	PB16B	5	C	-	PB20B	5	C	-
AA7	PB12A	5	T	-	PB17A	5	T	-	PB21A	5	T	-
AB7	PB12B	5	C	VREF2_5	PB17B	5	C	VREF2_5	PB21B	5	C	VREF2_5
Y7	PB13A	5	T	-	PB18A	5	T	-	PB22A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
AA8	PB13B	5	C	-	PB18B	5	C	-	PB22B	5	C	-
AB8	PB14A	5	T	-	PB19A	5	T	-	PB23A	5	T	-
Y8	PB14B	5	C	-	PB19B	5	C	-	PB23B	5	C	-
AB9	PB15A	5	T	-	PB20A	5	T	-	PB24A	5	T	-
AA9	PB15B	5	C	-	PB20B	5	C	-	PB24B	5	C	-
W10	PB16A	5	-	-	PB21A	5	-	-	PB25A	5	-	-
W11	PB17B	5	-	-	PB22B	5	-	-	PB26B	5	-	-
AB10	PB18A	5	T	DQS	PB23A	5	T	DQS	PB27A	5	T	DQS
AA10	PB18B	5	C	-	PB23B	5	C	-	PB27B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
AA11	PB19A	5	T	-	PB24A	5	T	-	PB28A	5	T	-
AB11	PB19B	5	C	-	PB24B	5	C	-	PB28B	5	C	-
Y11	PB20A	5	T	-	PB25A	5	T	-	PB29A	5	T	-
Y12	PB20B	5	C	-	PB25B	5	C	-	PB29B	5	C	-
AB12	PB21A	4	T	-	PB26A	4	T	-	PB30A	4	T	-
AA12	PB21B	4	C	-	PB26B	4	C	-	PB30B	4	C	-
AB13	PB22A	4	T	PCLKT4_0	PB27A	4	T	PCLKT4_0	PB31A	4	T	PCLKT4_0
AA13	PB22B	4	C	PCLKC4_0	PB27B	4	C	PCLKC4_0	PB31B	4	C	PCLKC4_0
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA14	PB23A	4	T	-	PB28A	4	T	-	PB32A	4	T	-
AB14	PB23B	4	C	-	PB28B	4	C	-	PB32B	4	C	-
W12	PB24A	4	-	-	PB29A	4	-	-	PB33A	4	-	-
W13	PB25B	4	-	-	PB30B	4	-	-	PB34B	4	-	-
AA15	PB26A	4	T	DQS	PB31A	4	T	DQS	PB35A	4	T	DQS
AB15	PB26B	4	C	VREF1_4	PB31B	4	C	VREF1_4	PB35B	4	C	VREF1_4
AA16	PB27A	4	T	-	PB32A	4	T	-	PB36A	4	T	-
AB16	PB27B	4	C	-	PB32B	4	C	-	PB36B	4	C	-
Y17	PB28A	4	T	-	PB33A	4	T	-	PB37A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA17	PB28B	4	C	-	PB33B	4	C	-	PB37B	4	C	-
Y13	PB29A	4	T	-	PB34A	4	T	-	PB38A	4	T	-
Y14	PB29B	4	C	-	PB34B	4	C	-	PB38B	4	C	-
AB17	PB30A	4	T	-	PB35A	4	T	-	PB39A	4	T	-
Y18	PB30B	4	C	-	PB35B	4	C	-	PB39B	4	C	-
AA18	PB31A	4	T	VREF2_4	PB36A	4	T	VREF2_4	PB40A	4	T	VREF2_4
AB18	PB31B	4	C	-	PB36B	4	C	-	PB40B	4	C	-
Y19	PB32A	4	-	-	PB37A	4	-	-	PB41A	4	-	-
AB19	PB33B	4	-	-	PB38B	4	-	-	PB42B	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA19	PB34A	4	T	DQS	PB39A	4	T	DQS	PB43A	4	T	DQS
Y20	PB34B	4	C	-	PB39B	4	C	-	PB43B	4	C	-
W14	PB35A	4	T	-	PB40A	4	T	-	PB44A	4	T	-
W15	PB35B	4	C	-	PB40B	4	C	-	PB44B	4	C	-
AB20	PB36A	4	T	-	PB41A	4	T	-	PB45A	4	T	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L1	-	-	-	-	PL23A	7	T[3]	-
M1	-	-	-	-	PL23B	7	C[3]	-
M2	-	-	-	-	PL24A	7	-	-
L5	VCCP0	-	-	-	VCCP0	-	-	-
N2	GNDP0	-	-	-	GNDP0	-	-	-
N1	-	-	-	-	PL25B	6	-	-
P2	-	-	-	-	PL26A	6	T[3]	-
P1	-	-	-	-	PL26B	6	C[3]	-
M4	PL23A	6	T[3]	-	PL27A	6	T[3]	-
M3	PL23B	6	C[3]	-	PL27B	6	C[3]	-
R2	PL24A	6	T	PCLKT6_0	PL28A	6	T	PCLKT6_0
-	GNDIO6	6	-	-	GNDIO6	6	-	-
R1	PL24B	6	C	PCLKC6_0	PL28B	6	C	PCLKC6_0
N3	PL25A	6	T[3]	-	PL29A	6	T[3]	-
N4	PL25B	6	C[3]	-	PL29B	6	C[3]	-
M5	PL26A	6	-	-	PL30A	6	-	-
N5	PL27B	6	-	VREF1_6	PL31B	6	-	VREF1_6
T2	PL28A	6	T[3]	DQS	PL32A	6	T[3]	DQS
T1	PL28B	6	C[3]	-	PL32B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
U2	PL29A	6	T	LLM0_PLLT_IN_A	PL33A	6	T	LLM0_PLLT_IN_A
U1	PL29B	6	C	LLM0_PLLC_IN_A	PL33B	6	C	LLM0_PLLC_IN_A
P3	PL30A	6	T[3]	-	PL34A	6	T[3]	-
P4	PL30B	6	C[3]	-	PL34B	6	C[3]	-
P6	PL32A	6	T[3]	-	PL36A	6	T[3]	-
P5	PL32B	6	C[3]	-	PL36B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
V2	PL33A	6	T	-	PL37A	6	T	-
V1	PL33B	6	C	-	PL37B	6	C	-
W2	PL34A	6	T[3]	-	PL38A	6	T[3]	-
W1	PL34B	6	C[3]	-	PL38B	6	C[3]	-
R3	PL35A	6	-	VREF2_6	PL39A	6	-	VREF2_6
R4	PL36B	6	-	-	PL40B	6	-	-
R6	PL37A	6	T[3]	DQS	PL41A	6	T[3]	DQS
R5	PL37B	6	C[3]	-	PL41B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
Y2	PL38A	6	T	LLM0_PLLT_FB_A	PL42A	6	T	LLM0_PLLT_FB_A
Y1	PL38B	6	C	LLM0_PLLC_FB_A	PL42B	6	C	LLM0_PLLC_FB_A
T3	PL39A	6	T[3]	-	PL43A	6	T[3]	-
T4	PL39B	6	C[3]	-	PL43B	6	C[3]	-
W3	PL40A	6	T[3]	-	PL44A	6	T[3]	-
V3	PL40B	6	C[3]	-	PL44B	6	C[3]	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
D18	-	-	-	-	PT55B	1	C	-
E18	-	-	-	-	PT55A	1	T	-
C19	-	-	-	-	PT54B	1	C	-
C18	-	-	-	-	PT54A	1	T	-
C21	-	-	-	-	PT53B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B21	-	-	-	-	PT53A	1	T	-
E17	PT48B	1	C	-	PT52B	1	C	-
E16	PT48A	1	T	-	PT52A	1	T	-
C17	PT47B	1	C	-	PT51B	1	C	-
D17	PT47A	1	T	DQS	PT51A	1	T	DQS
F17	PT46B	1	-	-	PT50B	1	-	-
F16	PT45A	1	-	-	PT49A	1	-	-
C16	PT44B	1	C	-	PT48B	1	C	-
D16	PT44A	1	T	-	PT48A	1	T	-
A20	PT43B	1	C	-	PT47B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B20	PT43A	1	T	-	PT47A	1	T	-
A19	PT42B	1	C	-	PT46B	1	C	-
B19	PT42A	1	T	-	PT46A	1	T	-
C15	PT41B	1	C	-	PT45B	1	C	-
D15	PT41A	1	T	-	PT45A	1	T	-
A18	PT40B	1	C	-	PT44B	1	C	-
B18	PT40A	1	T	-	PT44A	1	T	-
F15	PT39B	1	C	VREF1_1	PT43B	1	C	VREF1_1
-	GNDIO1	1	-	-	GNDIO1	1	-	-
E15	PT39A	1	T	DQS	PT43A	1	T	DQS
A17	PT38B	1	-	-	PT42B	1	-	-
B17	PT37A	1	-	-	PT41A	1	-	-
E14	PT36B	1	C	-	PT40B	1	C	-
F14	PT36A	1	T	-	PT40A	1	T	-
D14	PT35B	1	C	-	PT39B	1	C	-
C14	PT35A	1	T	D0	PT39A	1	T	D0
A16	PT34B	1	C	D1	PT38B	1	C	D1
B16	PT34A	1	T	VREF2_1	PT38A	1	T	VREF2_1
A15	PT33B	1	C	-	PT37B	1	C	-
B15	PT33A	1	T	D2	PT37A	1	T	D2
-	GNDIO1	1	-	-	GNDIO1	1	-	-
E13	PT32B	1	C	D3	PT36B	1	C	D3
D13	PT32A	1	T	-	PT36A	1	T	-
C13	PT31B	1	C	-	PT35B	1	C	-
B13	PT31A	1	T	DQS	PT35A	1	T	DQS

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
J15	GND	-	-	-	GND	-	-	-
J8	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-
K10	GND	-	-	-	GND	-	-	-
K11	GND	-	-	-	GND	-	-	-
K12	GND	-	-	-	GND	-	-	-
K13	GND	-	-	-	GND	-	-	-
K14	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-
L10	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-
L12	GND	-	-	-	GND	-	-	-
L13	GND	-	-	-	GND	-	-	-
L14	GND	-	-	-	GND	-	-	-
L9	GND	-	-	-	GND	-	-	-
M10	GND	-	-	-	GND	-	-	-
M11	GND	-	-	-	GND	-	-	-
M12	GND	-	-	-	GND	-	-	-
M13	GND	-	-	-	GND	-	-	-
M14	GND	-	-	-	GND	-	-	-
M9	GND	-	-	-	GND	-	-	-
N10	GND	-	-	-	GND	-	-	-
N11	GND	-	-	-	GND	-	-	-
N12	GND	-	-	-	GND	-	-	-
N13	GND	-	-	-	GND	-	-	-
N14	GND	-	-	-	GND	-	-	-
N9	GND	-	-	-	GND	-	-	-
P10	GND	-	-	-	GND	-	-	-
P11	GND	-	-	-	GND	-	-	-
P12	GND	-	-	-	GND	-	-	-
P13	GND	-	-	-	GND	-	-	-
P14	GND	-	-	-	GND	-	-	-
P15	GND	-	-	-	GND	-	-	-
P8	GND	-	-	-	GND	-	-	-
P9	GND	-	-	-	GND	-	-	-
R14	GND	-	-	-	GND	-	-	-
R9	GND	-	-	-	GND	-	-	-
F10	VCC	-	-	-	VCC	-	-	-
F13	VCC	-	-	-	VCC	-	-	-
G10	VCC	-	-	-	VCC	-	-	-
G13	VCC	-	-	-	VCC	-	-	-
G14	VCC	-	-	-	VCC	-	-	-

Commercial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6E-3F256C	188	1.2V	-3	fpBGA	256	COM	5.8K
LFXP6E-4F256C	188	1.2V	-4	fpBGA	256	COM	5.8K
LFXP6E-5F256C	188	1.2V	-5	fpBGA	256	COM	5.8K
LFXP6E-3Q208C	142	1.2V	-3	PQFP	208	COM	5.8K
LFXP6E-4Q208C	142	1.2V	-4	PQFP	208	COM	5.8K
LFXP6E-5Q208C	142	1.2V	-5	PQFP	208	COM	5.8K
LFXP6E-3T144C	100	1.2V	-3	TQFP	144	COM	5.8K
LFXP6E-4T144C	100	1.2V	-4	TQFP	144	COM	5.8K
LFXP6E-5T144C	100	1.2V	-5	TQFP	144	COM	5.8K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10E-3F388C	244	1.2V	-3	fpBGA	388	COM	9.7K
LFXP10E-4F388C	244	1.2V	-4	fpBGA	388	COM	9.7K
LFXP10E-5F388C	244	1.2V	-5	fpBGA	388	COM	9.7K
LFXP10E-3F256C	188	1.2V	-3	fpBGA	256	COM	9.7K
LFXP10E-4F256C	188	1.2V	-4	fpBGA	256	COM	9.7K
LFXP10E-5F256C	188	1.2V	-5	fpBGA	256	COM	9.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15E-3F484C	300	1.2V	-3	fpBGA	484	COM	15.5K
LFXP15E-4F484C	300	1.2V	-4	fpBGA	484	COM	15.5K
LFXP15E-5F484C	300	1.2V	-5	fpBGA	484	COM	15.5K
LFXP15E-3F388C	268	1.2V	-3	fpBGA	388	COM	15.5K
LFXP15E-4F388C	268	1.2V	-4	fpBGA	388	COM	15.5K
LFXP15E-5F388C	268	1.2V	-5	fpBGA	388	COM	15.5K
LFXP15E-3F256C	188	1.2V	-3	fpBGA	256	COM	15.5K
LFXP15E-4F256C	188	1.2V	-4	fpBGA	256	COM	15.5K
LFXP15E-5F256C	188	1.2V	-5	fpBGA	256	COM	15.5K

Industrial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15C-3F484I	300	1.8/2.5/3.3V	-3	fpBGA	484	IND	15.5K
LFXP15C-4F484I	300	1.8/2.5/3.3V	-4	fpBGA	484	IND	15.5K
LFXP15C-3F388I	268	1.8/2.5/3.3V	-3	fpBGA	388	IND	15.5K
LFXP15C-4F388I	268	1.8/2.5/3.3V	-4	fpBGA	388	IND	15.5K
LFXP15C-3F256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	15.5K
LFXP15C-4F256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	15.5K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20C-3F484I	340	1.8/2.5/3.3V	-3	fpBGA	484	IND	19.7K
LFXP20C-4F484I	340	1.8/2.5/3.3V	-4	fpBGA	484	IND	19.7K
LFXP20C-3F388I	268	1.8/2.5/3.3V	-3	fpBGA	388	IND	19.7K
LFXP20C-4F388I	268	1.8/2.5/3.3V	-4	fpBGA	388	IND	19.7K
LFXP20C-3F256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	19.7K
LFXP20C-4F256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	19.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3E-3Q208I	136	1.2V	-3	PQFP	208	IND	3.1K
LFXP3E-4Q208I	136	1.2V	-4	PQFP	208	IND	3.1K
LFXP3E-3T144I	100	1.2V	-3	TQFP	144	IND	3.1K
LFXP3E-4T144I	100	1.2V	-4	TQFP	144	IND	3.1K
LFXP3E-3T100I	62	1.2V	-3	TQFP	100	IND	3.1K
LFXP3E-4T100I	62	1.2V	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6E-3F256I	188	1.2V	-3	fpBGA	256	IND	5.8K
LFXP6E-4F256I	188	1.2V	-4	fpBGA	256	IND	5.8K
LFXP6E-3Q208I	142	1.2V	-3	PQFP	208	IND	5.8K
LFXP6E-4Q208I	142	1.2V	-4	PQFP	208	IND	5.8K
LFXP6E-3T144I	100	1.2V	-3	TQFP	144	IND	5.8K
LFXP6E-4T144I	100	1.2V	-4	TQFP	144	IND	5.8K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10E-3F388I	244	1.2V	-3	fpBGA	388	IND	9.7K
LFXP10E-4F388I	244	1.2V	-4	fpBGA	388	IND	9.7K
LFXP10E-3F256I	188	1.2V	-3	fpBGA	256	IND	9.7K
LFXP10E-4F256I	188	1.2V	-4	fpBGA	256	IND	9.7K