# Lattice Semiconductor Corporation - LFXP10C-3FN388C Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

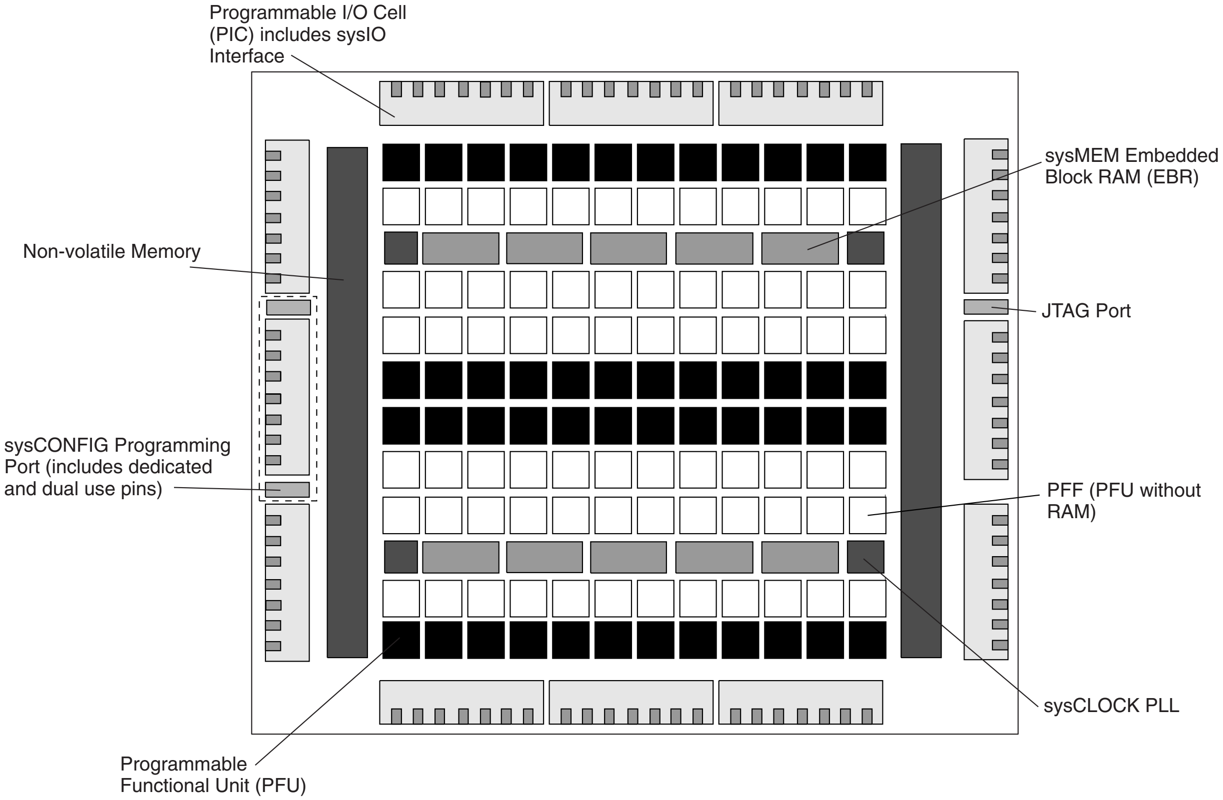
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 10000 |
| Total RAM Bits | 221184 |
| Number of I/O | 244 |
| Number of Gates | - |
| Voltage - Supply | 1.71V ~ 3.465V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 388-BBGA |
| Supplier Device Package | 388-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp10c-3fn388c |

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

*Figure 2-1. LatticeXP Top Level Block Diagram*



## PFU and PFF Blocks

The core of the LatticeXP devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of the data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-2. All the interconnections to and from PFU blocks are from routing. There are 53 inputs and 25 outputs associated with each PFU block.

*Figure 2-2. PFU Diagram*

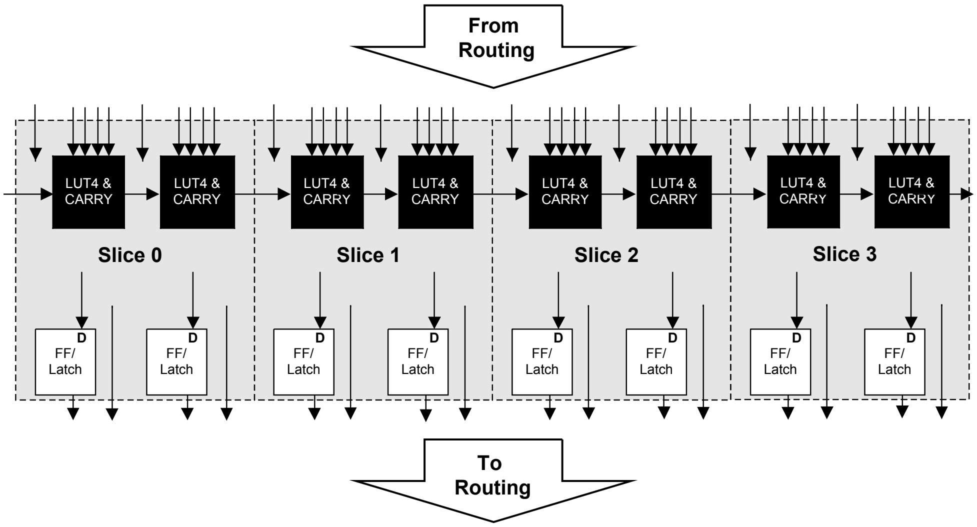


*Figure 2-10. PLL Diagram*

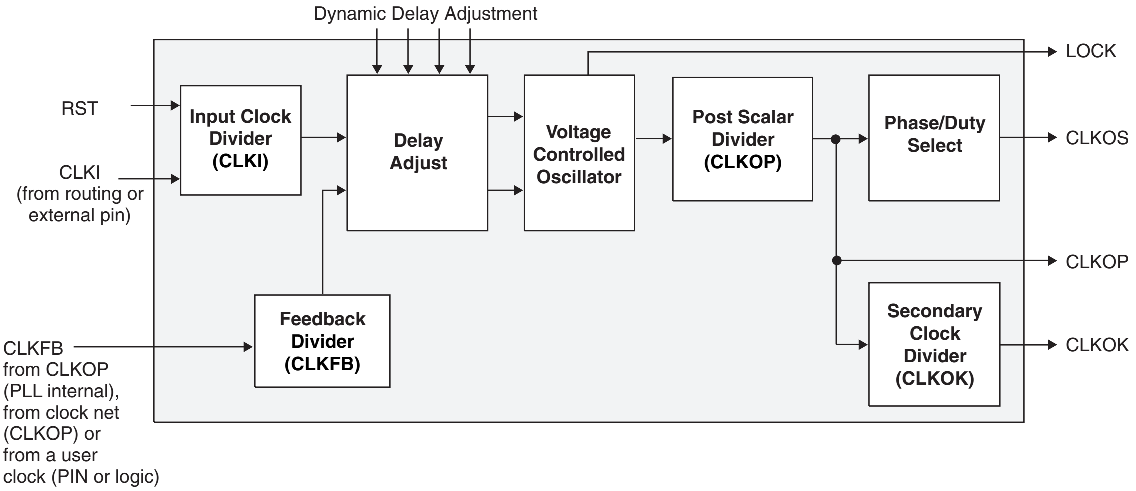


Figure 2-11 shows the available macros for the PLL. Table 2-11 provides signal description of the PLL Block.

*Figure 2-11. PLL Primitive*

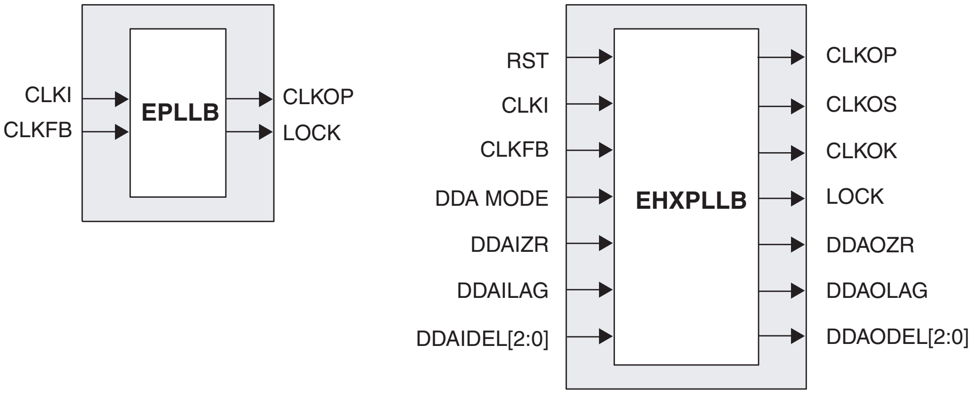


*Table 2-5. PLL Signal Descriptions*

| Signal | I/O | Description |
|---|---|---|
| CLKI | I | Clock input from external pin or routing |
| CLKFB | I | PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic) |
| RST | I | “1” to reset input clock divider |
| CLKOS | O | PLL output clock to clock tree (phase shifted/duty cycle changed) |
| CLKOP | O | PLL output clock to clock tree (No phase shift) |
| CLKOK | O | PLL output to clock tree through secondary clock divider |
| LOCK | O | “1” indicates PLL LOCK to CLKI |
| DDAMODE | I | Dynamic Delay Enable. “1” Pin control (dynamic), “0”: Fuse Control (static) |
| DDAIZR | I | Dynamic Delay Zero. “1”: delay = 0, “0”: delay = on |
| DDAILAG | I | Dynamic Delay Lag/Lead. “1”: Lag, “0”: Lead |
| DDAIDEL[2:0] | I | Dynamic Delay Input |
| DDAOZR | O | Dynamic Delay Zero Output |
| DDAOLAG | O | Dynamic Delay Lag/Lead Output |
| DDAODEL[2:0] | O | Dynamic Delay Output |

For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

## Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved irrespective of where the select signal is toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-12 illustrates the DCS Block Macro.

*Figure 2-12. DCS Block Primitive*

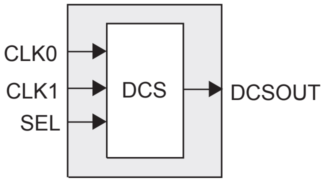
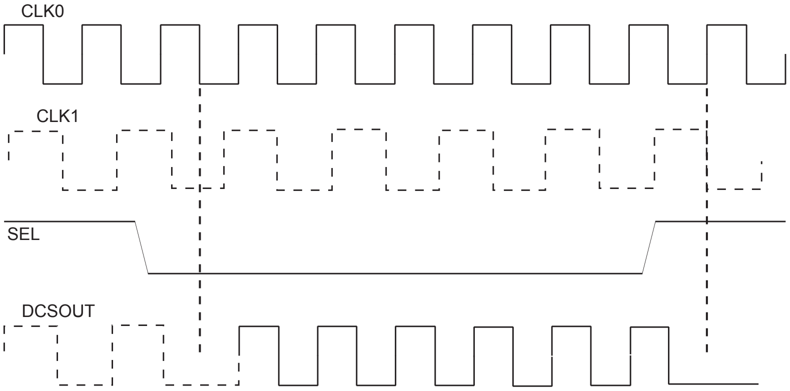


Figure 2-13 shows timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information on the DCS, please see details of additional technical documentation at the end of this data sheet.

*Figure 2-13. DCS Waveforms*



## sysMEM Memory

The LatticeXP family of devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers.

### sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-6.

*Figure 2-18. Group of Seven PIOs*

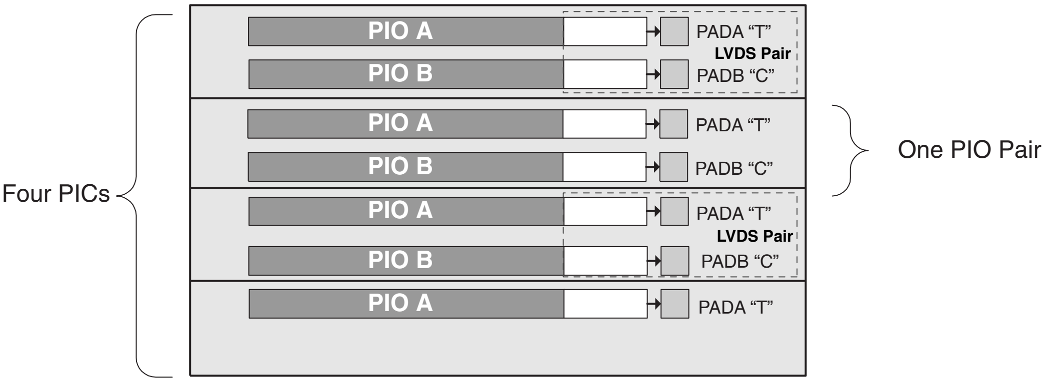
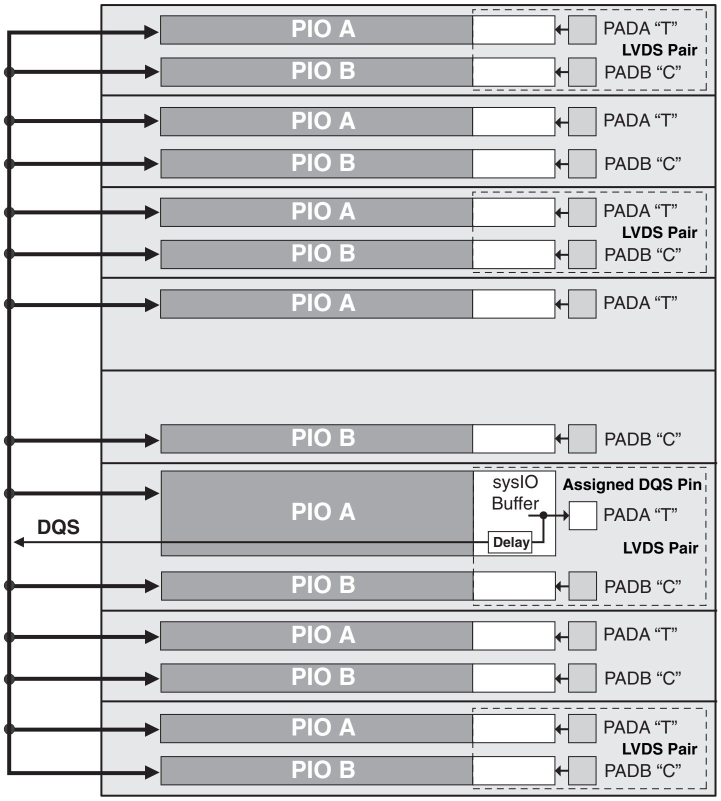


*Figure 2-19. DQS Routing*



## PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for both single data rate (SDR) and double data rate (DDR) operation along with the necessary clock and selection logic. Programmable delay lines used to shift incoming clock and data signals are also included in these blocks.

### Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-20 shows the diagram of the input register block.

Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and

*Figure 2-21. Input Register DDR Waveforms*

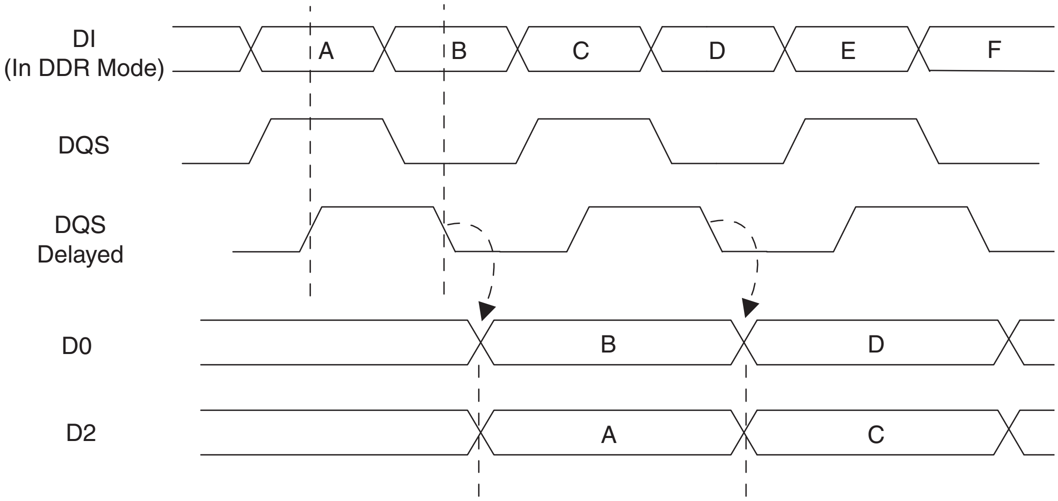
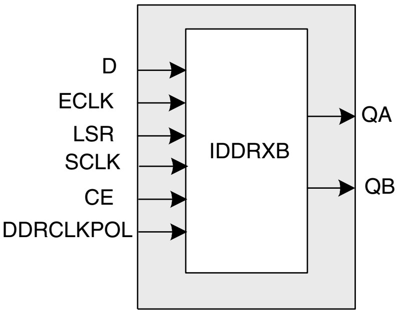


*Figure 2-22. INDDRXB Primitive*



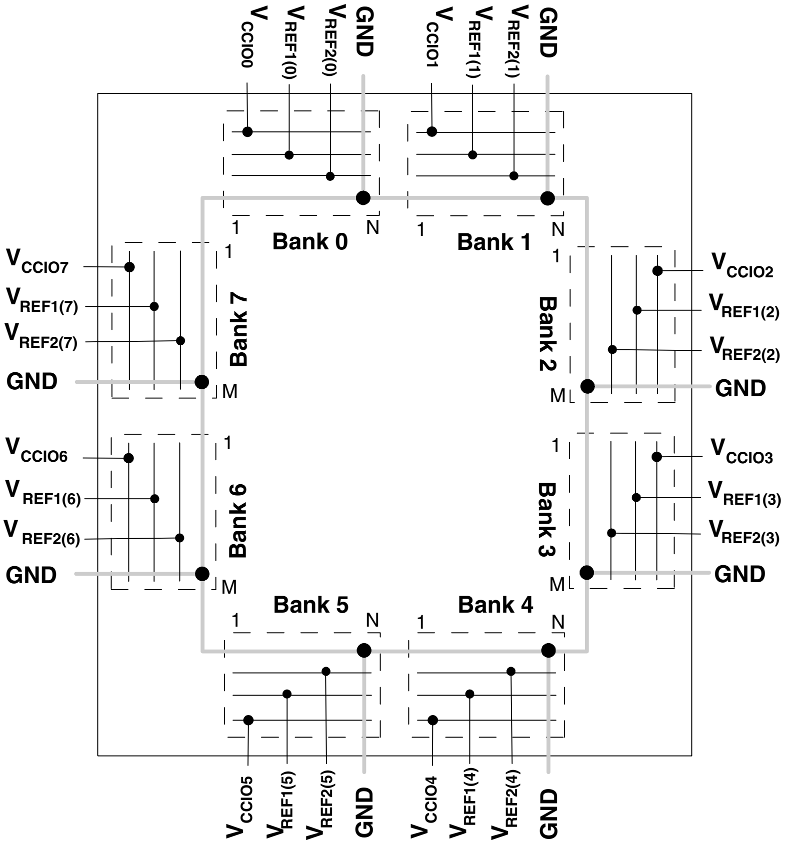
**Output Register Block**

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-23 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or as a latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-24 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

*Figure 2-28. LatticeXP Banks*



Note: N and M are the maximum number of I/Os per bank.

LatticeXP devices contain two types of sysIO buffer pairs.

1. **Top and Bottom sysIO Buffer Pair (Single-Ended Outputs Only)**
   The sysIO buffer pairs in the top and bottom banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

   Only the I/Os on the top and bottom banks have PCI clamps. Note that the PCI clamp is enabled after $V_{CC,}$ $V_{CCAUX}$ and $V_{CCIO}$ are at valid operating levels and the device has been configured.

2. **Left and Right sysIO Buffer Pair (Differential and Single-Ended Outputs)**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. The referenced input buffer can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

   Select I/Os in the left and right banks have LVDS differential output drivers. Refer to the Logic Signal Connections tables for more information.

*Table 2-8. Supported Output Standards*

| Output Standard | Drive | $V_{CCIO}$ (Nom.) |
|---|---|---|
| **Single-ended Interfaces** | | |
| LVTTL | 4mA, 8mA, 12mA, 16mA, 20mA | 3.3 |
| LVCMOS33 | 4mA, 8mA, 12mA 16mA, 20mA | 3.3 |
| LVCMOS25 | 4mA, 8mA, 12mA 16mA, 20mA | 2.5 |
| LVCMOS18 | 4mA, 8mA, 12mA 16mA | 1.8 |
| LVCMOS15 | 4mA, 8mA | 1.5 |
| LVCMOS12 | 2mA, 6mA | 1.2 |
| LVCMOS33, Open Drain | 4mA, 8mA, 12mA 16mA, 20mA | — |
| LVCMOS25, Open Drain | 4mA, 8mA, 12mA 16mA, 20mA | — |
| LVCMOS18, Open Drain | 4mA, 8mA, 12mA 16mA | — |
| LVCMOS15, Open Drain | 4mA, 8mA | — |
| LVCMOS12, Open Drain | 2mA. 6mA | — |
| PCI33 | N/A | 3.3 |
| HSTL18 Class I, II, III | N/A | 1.8 |
| HSTL15 Class I, III | N/A | 1.5 |
| SSTL3 Class I, II | N/A | 3.3 |
| SSTL2 Class I, II | N/A | 2.5 |
| SSTL18 Class I | N/A | 1.8 |
| **Differential Interfaces** | | |
| Differential SSTL3, Class I, II | N/A | 3.3 |
| Differential SSTL2, Class I, II | N/A | 2.5 |
| Differential SSTL18, Class I | N/A | 1.8 |
| Differential HSTL18, Class I, II, III | N/A | 1.8 |
| Differential HSTL15, Class I, III | N/A | 1.5 |
| LVDS | N/A | 2.5 |
| BLVDS[1] | N/A | 2.5 |
| LVPECL[1] | N/A | 3.3 |

1. Emulated with external resistors.

## Hot Socketing

The LatticeXP devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits, which allows easy integration with the rest of the system. These capabilities make the LatticeXP ideal for many multiple power supply and hot-swap applications.

# Sleep Mode

The LatticeXP "C" devices ($V_{CC}$ = 1.8/2.5/3.3V) have a sleep mode that allows standby current to be reduced by up to three orders of magnitude during periods of system inactivity. Entry and exit to Sleep Mode is controlled by the SLEEPN pin.

During Sleep Mode, the FPGA logic is non-operational, registers and EBR contents are not maintained and I/Os are tri-stated. Do not enter Sleep Mode during device programming or configuration operation. In Sleep Mode, power supplies can be maintained in their normal operating range, eliminating the need for external switching of power supplies. Table 2-9 compares the characteristics of Normal, Off and Sleep Modes.

master serial clock is 2.5MHz. Table 2-10 lists all the available Master Serial Clock frequencies. When a different Master Serial Clock is selected during the design process, the following sequence takes place:

1. User selects a different Master Serial Clock frequency for configuration.
2. During configuration the device starts with the default (2.5MHz) Master Serial Clock frequency.
3. The clock configuration settings are contained in the early configuration bit stream.
4. The Master Serial Clock frequency changes to the selected frequency once the clock configuration bits are received.

For further information on the use of this oscillator for configuration, please see details of additional technical documentation at the end of this data sheet.

***Table 2-10. Selectable Master Serial Clock (CCLK) Frequencies During Configuration***

| CCLK (MHz) | CCLK (MHz) | CCLK (MHz) |
|---|---|---|
| 2.5[1] | 13 | 45 |
| 4.3 | 15 | 51 |
| 5.4 | 20 | 55 |
| 6.9 | 26 | 60 |
| 8.1 | 30 | 130 |
| 9.2 | 34 | — |
| 10.0 | 41 | — |

[1] Default

## Density Shifting

The LatticeXP family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

## DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1, 2, 4] | Input or I/O Leakage | $0 \le V_{IN} \le (V_{CCIO} - 0.2V)$ | — | — | 10 | µA |
| | | $(V_{CCIO} - 0.2V) < V_{IN} \le 3.6V$ | — | — | 40 | µA |
| $I_{PU}$ | I/O Active Pull-up Current | $0 \le V_{IN} \le 0.7\ V_{CCIO}$ | -30 | — | -150 | µA |
| $I_{PD}$ | I/O Active Pull-down Current | $V_{IL}$ (MAX) $\le V_{IN} \le V_{IH}$ (MAX) | 30 | — | 150 | µA |
| $I_{BHLS}$ | Bus Hold Low sustaining current | $V_{IN} = V_{IL}$ (MAX) | 30 | — | — | µA |
| $I_{BHHS}$ | Bus Hold High sustaining current | $V_{IN} = 0.7V_{CCIO}$ | -30 | — | — | µA |
| $I_{BHLO}$ | Bus Hold Low Overdrive current | $0 \le V_{IN} \le V_{IH}$ (MAX) | — | — | 150 | µA |
| $I_{BHHO}$ | Bus Hold High Overdrive current | $0 \le V_{IN} \le V_{IH}$ (MAX) | — | — | -150 | µA |
| $V_{BHT}$ | Bus Hold trip Points | $0 \le V_{IN} \le V_{IH}$ (MAX) | $V_{IL}$ (MAX) | — | $V_{IH}$ (MIN) | V |
| C1 | I/O Capacitance[3] | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,<br>$V_{CC}$ = 1.2V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 8 | — | pf |
| C2 | Dedicated Input Capacitance[3] | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,<br>$V_{CC}$ = 1.2V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 8 | — | pf |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. Not applicable to SLEEPN/TOE pin.
3. $T_A$ 25°C, f = 1.0MHz
4. When $V_{IH}$ is higher than $V_{CCIO}$, a transient current typically of 30ns in duration or less with a peak current of 6mA can be expected on the high-to-low transition.

## Supply Current (Sleep Mode)[1, 2, 3]

| Symbol | Parameter | Device | Typ.[4] | Max | Units |
|---|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LFXP3C | 12 | 65 | µA |
| | | LFXP6C | 14 | 75 | µA |
| | | LFXP10C | 16 | 85 | µA |
| | | LFXP15C | 18 | 95 | µA |
| | | LFXP20C | 20 | 105 | µA |
| $I_{CCP}$ | PLL Power Supply (per PLL) | All LFXP ‘C’ Devices | 1 | 5 | µA |
| $I_{CCAUX}$ | Auxiliary Power Supply | LFXP3C | 2 | 90 | µA |
| | | LFXP6C | 2 | 100 | µA |
| | | LFXP10C | 2 | 110 | µA |
| | | LFXP15C | 3 | 120 | µA |
| | | LFXP20C | 4 | 130 | µA |
| $I_{CCIO}$ | Bank Power Supply[5] | LFXP3C | 2 | 20 | µA |
| | | LFXP6C | 2 | 22 | µA |
| | | LFXP10C | 2 | 24 | µA |
| | | LFXP15C | 3 | 27 | µA |
| | | LFXP20C | 4 | 30 | µA |
| $I_{CCJ}$ | VCCJ Power Supply | All LFXP ‘C’ Devices | 1 | 5 | µA |

1. Assumes all inputs are configured as LVCMOS and held at the VCCIO or GND.
2. Frequency 0MHz.
3. User pattern: blank.
4. $T_A$=25°C, power supplies at nominal voltage.
5. Per bank.

# Programming and Erase Flash Supply Current[1, 2, 3, 4, 5]

| Symbol | Parameter | Device | Typ.[6] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LFXP3E | 30 | mA |
| | | LFXP6E | 40 | mA |
| | | LFXP10E | 50 | mA |
| | | LFXP15E | 60 | mA |
| | | LFXP20E | 70 | mA |
| | | LFXP3C | 50 | mA |
| | | LFXP6C | 60 | mA |
| | | LFXP10C | 90 | mA |
| | | LFXP15C | 100 | mA |
| | | LFXP20C | 110 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply $V_{CCAUX}$ = 3.3V | LFXP3E/C | 50 | mA |
| | | LFXP6E/C | 60 | mA |
| | | LFXP10E/C | 90 | mA |
| | | LFXP15E/C | 110 | mA |
| | | LFXP20E/C | 130 | mA |
| $I_{CCJ}$ | $V_{CCJ}$ Power Supply[7] | All | 2 | mA |

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
3. Blank user pattern; typical Flash pattern.
4. Bypass or decoupling capacitor across the supply.
5. JTAG programming is at 1MHz.
6. $T_A$=25°C, power supplies at nominal voltage.
7. When programming via JTAG.

## LatticeXP Family Timing Adders[1]

**Over Recommended Operating Conditions**

| Buffer Type | Description | -5 | -4 | -3 | Units |
|---|---|---|---|---|---|
| **Input Adjusters** | | | | | |
| LVDS25E | LVDS 2.5 Emulated | 0.5 | 0.5 | 0.5 | ns |
| LVDS25 | LVDS | 0.4 | 0.4 | 0.4 | ns |
| BLVDS25 | BLVDS | 0.5 | 0.5 | 0.5 | ns |
| LVPECL33 | LVPECL | 0.6 | 0.6 | 0.6 | ns |
| HSTL18_I | HSTL_18 class I | 0.4 | 0.4 | 0.4 | ns |
| HSTL18_II | HSTL_18 class II | 0.4 | 0.4 | 0.4 | ns |
| HSTL18_III | HSTL_18 class III | 0.4 | 0.4 | 0.4 | ns |
| HSTL18D_I | Differential HSTL 18 class I | 0.4 | 0.4 | 0.4 | ns |
| HSTL18D_II | Differential HSTL 18 class II | 0.4 | 0.4 | 0.4 | ns |
| HSTL18D_III | Differential HSTL 18 class III | 0.4 | 0.4 | 0.4 | ns |
| HSTL15_I | HSTL_15 class I | 0.5 | 0.5 | 0.5 | ns |
| HSTL15_III | HSTL_15 class III | 0.5 | 0.5 | 0.5 | ns |
| HSTL15D_I | Differential HSTL 15 class I | 0.5 | 0.5 | 0.5 | ns |
| HSTL15D_III | Differential HSTL 15 class III | 0.5 | 0.5 | 0.5 | ns |
| SSTL33_I | SSTL_3 class I | 0.6 | 0.6 | 0.6 | ns |
| SSTL33_II | SSTL_3 class II | 0.6 | 0.6 | 0.6 | ns |
| SSTL33D_I | Differential SSTL_3 class I | 0.6 | 0.6 | 0.6 | ns |
| SSTL33D_II | Differential SSTL_3 class II | 0.6 | 0.6 | 0.6 | ns |
| SSTL25_I | SSTL_2 class I | 0.5 | 0.5 | 0.5 | ns |
| SSTL25_II | SSTL_2 class II | 0.5 | 0.5 | 0.5 | ns |
| SSTL25D_I | Differential SSTL_2 class I | 0.5 | 0.5 | 0.5 | ns |
| SSTL25D_II | Differential SSTL_2 class II | 0.5 | 0.5 | 0.5 | ns |
| SSTL18_I | SSTL_18 class I | 0.5 | 0.5 | 0.5 | ns |
| SSTL18D_I | Differential SSTL_18 class I | 0.5 | 0.5 | 0.5 | ns |
| LVTTL33 | LVTTL | 0.2 | 0.2 | 0.2 | ns |
| LVCMOS33 | LVCMOS 3.3 | 0.2 | 0.2 | 0.2 | ns |
| LVCMOS25 | LVCMOS 2.5 | 0.0 | 0.0 | 0.0 | ns |
| LVCMOS18 | LVCMOS 1.8 | 0.1 | 0.1 | 0.1 | ns |
| LVCMOS15 | LVCMOS 1.5 | 0.1 | 0.1 | 0.1 | ns |
| LVCMOS12 | LVCMOS 1.2 | 0.1 | 0.1 | 0.1 | ns |
| PCI33 | PCI | 0.2 | 0.2 | 0.2 | ns |
| **Output Adjusters** | | | | | |
| LVDS25E | LVDS 2.5 Emulated | 0.3 | 0.3 | 0.3 | ns |
| LVDS25 | LVDS 2.5 | 0.3 | 0.3 | 0.3 | ns |
| BLVDS25 | BLVDS 2.5 | 0.3 | 0.3 | 0.3 | ns |
| LVPECL33 | LVPECL 3.3 | 0.1 | 0.1 | 0.1 | ns |
| HSTL18_I | HSTL_18 class I | 0.1 | 0.1 | 0.1 | ns |
| HSTL18_II | HSTL_18 class II | 0.1 | 0.1 | 0.1 | ns |
| HSTL18_III | HSTL_18 class III | 0.2 | 0.2 | 0.2 | ns |
| HSTL18D_I | Differential HSTL 18 class I | 0.1 | 0.1 | 0.1 | ns |
| HSTL18D_II | Differential HSTL 18 class II | -0.1 | -0.1 | -0.1 | ns |
| HSTL18D_III | Differential HSTL 18 class III | 0.2 | 0.2 | 0.2 | ns |

# PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

| PICs Associated with DQS Strobe | PIO within PIC | Polarity | DDR Strobe (DQS) and Data (DQ) Pins |
|---|---|---|---|
| P[Edge] [n-4] | A | True | DQ |
| | B | Complement | DQ |
| P[Edge] [n-3] | A | True | DQ |
| | B | Complement | DQ |
| P[Edge] [n-2] | A | True | DQ |
| | B | Complement | DQ |
| P[Edge] [n-1] | A | True | DQ |
| | | | |
| P[Edge] [n] | | | |
| | B | Complement | DQ |
| P[Edge] [n+1] | A | True | [Edge]DQSn |
| | B | Complement | DQ |
| P[Edge] [n+2] | A | True | DQ |
| | B | Complement | DQ |
| P[Edge] [n+3] | A | True | DQ |
| | B | Complement | DQ |

Notes:

1. “n” is a row/column PIC number.
2. The DDR interface is designed for memories that support one DQS strobe per eight bits of data. In some packages, all the potential DDR data (DQ) pins may not be available.
3. The definition of the PIC numbering is provided in the Signal Names column of the Signal Descriptions table in this data sheet.

## LFXP3 Logic Signal Connections: 100 TQFP (Cont.)

| Pin Number | Pin Function | Bank | Differential | Dual Function |
|---|---|---|---|---|
| 88 | PT14B | 1 | - | D7 |
| 89 | PT13B | 0 | C | BUSY |
| 90 | GNDIO0 | 0 | - | - |
| 91 | PT13A | 0 | T | CS1N |
| 92 | PT12B | 0 | C | PCLKC0_0 |
| 93 | PT12A | 0 | T | PCLKT0_0 |
| 94 | VCCIO0 | 0 | - | - |
| 95 | PT9A | 0 | - | DOUT |
| 96 | PT8A | 0 | - | WRITEN |
| 97 | PT6A | 0 | - | DI |
| 98 | PT5A | 0 | - | CSN |
| 99 | GND | - | - | - |
| 100 | CFG0 | 0 | - | - |

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

# LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP

| Pin Number | LFXP3 | | | | LFXP6 | | | |
|---|---|---|---|---|---|---|---|---|
| | **Pin Function** | **Bank** | **Differential** | **Dual Function** | **Pin Function** | **Bank** | **Differential** | **Dual Function** |
| 1 | PROGRAMN | 7 | - | - | PROGRAMN | 7 | - | - |
| 2 | CCLK | 7 | - | - | CCLK | 7 | - | - |
| 3 | GND | - | - | - | GND | - | - | - |
| 4 | PL2A | 7 | T[3] | - | PL2A | 7 | T[3] | - |
| 5 | PL2B | 7 | C[3] | - | PL2B | 7 | C[3] | - |
| 6 | PL3A | 7 | T | LUM0_PLLT_FB_A | PL3A | 7 | T | LUM0_PLLT_FB_A |
| 7 | PL3B | 7 | C | LUM0_PLLC_FB_A | PL3B | 7 | C | LUM0_PLLC_FB_A |
| 8 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| 9 | PL5A | 7 | - | VREF1_7 | PL5A | 7 | - | VREF1_7 |
| 10 | PL6B | 7 | - | VREF2_7 | PL6B | 7 | - | VREF2_7 |
| 11 | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| 12 | PL7A | 7 | T[3] | DQS | PL7A | 7 | T[3] | DQS |
| 13 | PL7B | 7 | C[3] | - | PL7B | 7 | C[3] | - |
| 14 | VCC | - | - | - | VCC | - | - | - |
| 15 | PL8A | 7 | T | LUM0_PLLT_IN_A | PL8A | 7 | T | LUM0_PLLT_IN_A |
| 16 | PL8B | 7 | C | LUM0_PLLC_IN_A | PL8B | 7 | C | LUM0_PLLC_IN_A |
| 17 | PL9A | 7 | T[3] | - | PL9A | 7 | T[3] | - |
| 18 | PL9B | 7 | C[3] | - | PL9B | 7 | C[3] | - |
| 19 | VCCP0 | - | - | - | VCCP0 | - | - | - |
| 20 | GNDP0 | - | - | - | GNDP0 | - | - | - |
| 21 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| 22 | PL11A | 6 | T[3] | - | PL16A | 6 | T[3] | - |
| 23 | PL11B | 6 | C[3] | - | PL16B | 6 | C[3] | - |
| 24 | PL12A | 6 | T | PCLKT6_0 | PL17A | 6 | T | PCLKT6_0 |
| 25 | PL12B | 6 | C | PCLKC6_0 | PL17B | 6 | C | PCLKC6_0 |
| 26 | PL13A | 6 | T[3] | - | PL18A | 6 | T[3] | - |
| 27 | PL13B | 6 | C[3] | - | PL18B | 6 | C[3] | - |
| 28 | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| 29 | PL14A | 6 | - | VREF1_6 | PL22A | 6 | - | VREF1_6 |
| 30 | PL15B | 6 | - | VREF2_6 | PL23B | 6 | - | VREF2_6 |
| 31 | PL16A | 6 | T[3] | DQS | PL24A | 6 | T[3] | DQS |
| 32 | PL16B | 6 | C[3] | - | PL24B | 6 | C[3] | - |
| 33 | PL17A | 6 | - | - | PL25A | 6 | - | - |
| 34 | PL18A | 6 | T[3] | - | PL26A | 6 | T[3] | - |
| 35 | PL18B | 6 | C[3] | - | PL26B | 6 | C[3] | - |
| 36 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| 37 | SLEEPN[1]/TOE[2] | - | - | - | SLEEPN[1]/TOE[2] | - | - | - |
| 38 | INITN | 5 | - | - | INITN | 5 | - | - |
| 39 | VCC | - | - | - | VCC | - | - | - |
| 40 | PB2B | 5 | - | VREF1_5 | PB5B | 5 | - | VREF1_5 |
| 41 | PB5B | 5 | - | VREF2_5 | PB8B | 5 | - | VREF2_5 |
| 42 | PB7A | 5 | T | - | PB10A | 5 | T | - |
| 43 | PB7B | 5 | C | - | PB10B | 5 | C | - |
| 44 | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| 45 | PB9A | 5 | - | - | PB12A | 5 | - | - |
| 46 | PB10B | 5 | - | - | PB13B | 5 | - | - |

# LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

| | LFXP6 | | | | LFXP10 | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| K4 | PL20A | 6 | T | - | PL29A | 6 | T | - |
| K5 | PL20B | 6 | C | - | PL29B | 6 | C | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| N1 | PL23B | 6 | - | VREF2_6 | PL31A | 6 | - | VREF2_6 |
| N2 | PL21B | 6 | C[3] | - | PL32B | 6 | - | - |
| P1 | PL24A | 6 | T[3] | DQS | PL33A | 6 | T[3] | DQS |
| P2 | PL24B | 6 | C[3] | - | PL33B | 6 | C[3] | - |
| L5 | PL25A | 6 | T | - | PL34A | 6 | T | LLM0_PLLT_FB_A |
| M6 | PL25B | 6 | C | - | PL34B | 6 | C | LLM0_PLLC_FB_A |
| M3 | PL26A | 6 | T[3] | - | PL35A | 6 | T[3] | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| N3 | PL26B | 6 | C[3] | - | PL35B | 6 | C[3] | - |
| P4 | SLEEPN[1]/TOE[2] | - | - | - | SLEEPN[1]/TOE[2] | - | - | - |
| P3 | INITN | 5 | - | - | INITN | 5 | - | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| R4 | PB2A | 5 | T | - | PB6A | 5 | T | - |
| N5 | PB2B | 5 | C | - | PB6B | 5 | C | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| P5 | PB5B | 5 | - | VREF1_5 | PB7A | 5 | T | VREF1_5 |
| R1 | PB3B | 5 | C | - | PB7B | 5 | C | - |
| N6 | PB4A | 5 | - | - | PB8A | 5 | - | - |
| M7 | PB3A | 5 | T | - | PB9B | 5 | - | - |
| R2 | PB6A | 5 | T | DQS | PB10A | 5 | T | DQS |
| T2 | PB6B | 5 | C | - | PB10B | 5 | C | - |
| R3 | PB7A | 5 | T | - | PB11A | 5 | T | - |
| T3 | PB7B | 5 | C | - | PB11B | 5 | C | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| T4 | PB8A | 5 | T | - | PB12A | 5 | T | - |
| R5 | PB8B | 5 | C | VREF2_5 | PB12B | 5 | C | VREF2_5 |
| N7 | PB9A | 5 | T | - | PB13A | 5 | T | - |
| M8 | PB9B | 5 | C | - | PB13B | 5 | C | - |
| T5 | PB10A | 5 | T | - | PB14A | 5 | T | - |
| P6 | PB10B | 5 | C | - | PB14B | 5 | C | - |
| T6 | PB11A | 5 | T | - | PB15A | 5 | T | - |
| R6 | PB11B | 5 | C | - | PB15B | 5 | C | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| P7 | PB12A | 5 | - | - | PB16A | 5 | - | - |
| N8 | PB13B | 5 | - | - | PB17B | 5 | - | - |
| R7 | PB14A | 5 | T | DQS | PB18A | 5 | T | DQS |
| T7 | PB14B | 5 | C | - | PB18B | 5 | C | - |
| P8 | PB15A | 5 | T | - | PB19A | 5 | T | - |
| T8 | PB15B | 5 | C | - | PB19B | 5 | C | - |

## LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA

| | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| C2 | PROGRAMN | 7 | - | - | PROGRAMN | 7 | - | - |
| C1 | CCLK | 7 | - | - | CCLK | 7 | - | - |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| D2 | PL7A | 7 | T | LUM0_PLLT_FB_A | PL7A | 7 | T | LUM0_PLLT_FB_A |
| D3 | PL7B | 7 | C | LUM0_PLLC_FB_A | PL7B | 7 | C | LUM0_PLLC_FB_A |
| D1 | PL9A | 7 | - | - | PL9A | 7 | - | - |
| E2 | PL10B | 7 | - | VREF1_7 | PL10B | 7 | - | VREF1_7 |
| E1 | PL11A | 7 | T[3] | DQS | PL11A | 7 | T[3] | DQS |
| F1 | PL11B | 7 | C[3] | - | PL11B | 7 | C[3] | - |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| E3 | PL12A | 7 | T | - | PL12A | 7 | T | - |
| F4 | PL12B | 7 | C | - | PL12B | 7 | C | - |
| F3 | PL13A | 7 | T[3] | - | PL13A | 7 | T[3] | - |
| F2 | PL13B | 7 | C[3] | - | PL13B | 7 | C[3] | - |
| G1 | PL15B | 7 | - | - | PL15B | 7 | - | - |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| G3 | PL16A | 7 | T | LUM0_PLLT_IN_A | PL16A | 7 | T | LUM0_PLLT_IN_A |
| G2 | PL16B | 7 | C | LUM0_PLLC_IN_A | PL16B | 7 | C | LUM0_PLLC_IN_A |
| H1 | PL17A | 7 | T[3] | - | PL17A | 7 | T[3] | - |
| H2 | PL17B | 7 | C[3] | - | PL17B | 7 | C[3] | - |
| G4 | PL18A | 7 | - | VREF2_7 | PL18A | 7 | - | VREF2_7 |
| G5 | PL19B | 7 | - | - | PL19B | 7 | - | - |
| J1 | PL20A | 7 | T[3] | DQS | PL20A | 7 | T[3] | DQS |
| - | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| J2 | PL20B | 7 | C[3] | - | PL20B | 7 | C[3] | - |
| H3 | PL22A | 7 | T[3] | - | PL22A | 7 | T[3] | - |
| J3 | PL22B | 7 | C[3] | - | PL22B | 7 | C[3] | - |
| H4 | VCCP0 | - | - | - | VCCP0 | - | - | - |
| H5 | GNDP0 | - | - | - | GNDP0 | - | - | - |
| K1 | PL24A | 6 | T | PCLKT6_0 | PL28A | 6 | T | PCLKT6_0 |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| K2 | PL24B | 6 | C | PCLKC6_0 | PL28B | 6 | C | PCLKC6_0 |
| J4 | PL26A | 6 | - | - | PL30A | 6 | - | - |
| J5 | PL27B | 6 | - | VREF1_6 | PL31B | 6 | - | VREF1_6 |
| L1 | PL28A | 6 | T[3] | DQS | PL32A | 6 | T[3] | DQS |
| L2 | PL28B | 6 | C[3] | - | PL32B | 6 | C[3] | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| M1 | PL29A | 6 | T | LLM0_PLLT_IN_A | PL33A | 6 | T | LLM0_PLLT_IN_A |
| M2 | PL29B | 6 | C | LLM0_PLLC_IN_A | PL33B | 6 | C | LLM0_PLLC_IN_A |
| K3 | PL30A | 6 | T[3] | - | PL34A | 6 | T[3] | - |
| L3 | PL30B | 6 | C[3] | - | PL34B | 6 | C[3] | - |

## LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

| | LFXP10 | | | | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function |
| M21 | VCCP1 | - | - | - | VCCP1 | - | - | - | VCCP1 | - | - | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| M22 | PR18B | 2 | C[3] | - | PR22B | 2 | C[3] | - | PR22B | 2 | C[3] | - |
| L22 | PR18A | 2 | T[3] | - | PR22A | 2 | T[3] | - | PR22A | 2 | T[3] | - |
| K22 | PR17B | 2 | C | PCLKC2_0 | PR21B | 2 | C | PCLKC2_0 | PR21B | 2 | C | PCLKC2_0 |
| K21 | PR17A | 2 | T | PCLKT2_0 | PR21A | 2 | T | PCLKT2_0 | PR21A | 2 | T | PCLKT2_0 |
| L19 | PR16B | 2 | C[3] | - | PR20B | 2 | C[3] | - | PR20B | 2 | C[3] | - |
| K20 | PR16A | 2 | T[3] | DQS | PR20A | 2 | T[3] | DQS | PR20A | 2 | T[3] | DQS |
| L20 | PR15B | 2 | - | - | PR19B | 2 | - | - | PR19B | 2 | - | - |
| L21 | PR14A | 2 | - | VREF1_2 | PR18A | 2 | - | VREF1_2 | PR18A | 2 | - | VREF1_2 |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| J22 | PR13B | 2 | C[3] | - | PR17B | 2 | C[3] | - | PR17B | 2 | C[3] | - |
| J21 | PR13A | 2 | T[3] | - | PR17A | 2 | T[3] | - | PR17A | 2 | T[3] | - |
| H22 | PR12B | 2 | C | RUM0_PLLC_IN_A | PR16B | 2 | C | RUM0_PLLC_IN_A | PR16B | 2 | C | RUM0_PLLC_IN_A |
| H21 | PR12A | 2 | T | RUM0_PLLT_IN_A | PR16A | 2 | T | RUM0_PLLT_IN_A | PR16A | 2 | T | RUM0_PLLT_IN_A |
| K19 | PR11B | 2 | C[3] | - | PR15B | 2 | C[3] | - | PR15B | 2 | C[3] | - |
| J19 | PR11A | 2 | T[3] | - | PR15A | 2 | T[3] | - | PR15A | 2 | T[3] | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| J20 | PR9B | 2 | C[3] | - | PR13B | 2 | C[3] | - | PR13B | 2 | C[3] | - |
| H20 | PR9A | 2 | T[3] | - | PR13A | 2 | T[3] | - | PR13A | 2 | T[3] | - |
| H19 | PR8B | 2 | C | - | PR12B | 2 | C | - | PR12B | 2 | C | - |
| G19 | PR8A | 2 | T | - | PR12A | 2 | T | - | PR12A | 2 | T | - |
| G22 | PR7B | 2 | C[3] | - | PR11B | 2 | C[3] | - | PR11B | 2 | C[3] | - |
| G21 | PR7A | 2 | T[3] | DQS | PR11A | 2 | T[3] | DQS | PR11A | 2 | T[3] | DQS |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| F20 | PR6B | 2 | - | - | PR10B | 2 | - | - | PR10B | 2 | - | - |
| G20 | PR5A | 2 | - | VREF2_2 | PR9A | 2 | - | VREF2_2 | PR9A | 2 | - | VREF2_2 |
| F22 | PR4B | 2 | C[3] | - | PR8B | 2 | C[3] | - | PR8B | 2 | C[3] | - |
| F21 | PR4A | 2 | T[3] | - | PR8A | 2 | T[3] | - | PR8A | 2 | T[3] | - |
| E22 | PR3B | 2 | C | RUM0_PLLC_FB_A | PR7B | 2 | C | RUM0_PLLC_FB_A | PR7B | 2 | C | RUM0_PLLC_FB_A |
| E21 | PR3A | 2 | T | RUM0_PLLT_FB_A | PR7A | 2 | T | RUM0_PLLT_FB_A | PR7A | 2 | T | RUM0_PLLT_FB_A |
| D22 | PR2B | 2 | C[3] | - | PR6B | 2 | C[3] | - | PR6B | 2 | C[3] | - |
| D21 | PR2A | 2 | T[3] | - | PR6A | 2 | T[3] | - | PR6A | 2 | T[3] | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| F19 | TDO | - | - | - | TDO | - | - | - | TDO | - | - | - |
| E20 | VCCJ | - | - | - | VCCJ | - | - | - | VCCJ | - | - | - |
| D20 | TDI | - | - | - | TDI | - | - | - | TDI | - | - | - |
| D19 | TMS | - | - | - | TMS | - | - | - | TMS | - | - | - |
| D18 | TCK | - | - | - | TCK | - | - | - | TCK | - | - | - |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| E19 | - | - | - | - | PT48A | 1 | - | - | PT52A | 1 | - | - |
| D17 | - | - | - | - | PT47B | 1 | C | - | PT51B | 1 | C | - |
| D16 | - | - | - | - | PT47A | 1 | T | DQS | PT51A | 1 | T | DQS |
| C16 | - | - | - | - | PT46B | 1 | - | - | PT50B | 1 | - | - |
| C15 | - | - | - | - | PT45A | 1 | - | - | PT49A | 1 | - | - |
| C17 | - | - | - | - | PT44B | 1 | C | - | PT48B | 1 | C | - |
| C18 | PT39A | 1 | - | - | PT44A | 1 | T | - | PT48A | 1 | T | - |
| C19 | PT38B | 1 | C | - | PT43B | 1 | C | - | PT47B | 1 | C | - |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |

## LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| J15 | GND | - | - | - | GND | - | - | - |
| J8 | GND | - | - | - | GND | - | - | - |
| J9 | GND | - | - | - | GND | - | - | - |
| K10 | GND | - | - | - | GND | - | - | - |
| K11 | GND | - | - | - | GND | - | - | - |
| K12 | GND | - | - | - | GND | - | - | - |
| K13 | GND | - | - | - | GND | - | - | - |
| K14 | GND | - | - | - | GND | - | - | - |
| K9 | GND | - | - | - | GND | - | - | - |
| L10 | GND | - | - | - | GND | - | - | - |
| L11 | GND | - | - | - | GND | - | - | - |
| L12 | GND | - | - | - | GND | - | - | - |
| L13 | GND | - | - | - | GND | - | - | - |
| L14 | GND | - | - | - | GND | - | - | - |
| L9 | GND | - | - | - | GND | - | - | - |
| M10 | GND | - | - | - | GND | - | - | - |
| M11 | GND | - | - | - | GND | - | - | - |
| M12 | GND | - | - | - | GND | - | - | - |
| M13 | GND | - | - | - | GND | - | - | - |
| M14 | GND | - | - | - | GND | - | - | - |
| M9 | GND | - | - | - | GND | - | - | - |
| N10 | GND | - | - | - | GND | - | - | - |
| N11 | GND | - | - | - | GND | - | - | - |
| N12 | GND | - | - | - | GND | - | - | - |
| N13 | GND | - | - | - | GND | - | - | - |
| N14 | GND | - | - | - | GND | - | - | - |
| N9 | GND | - | - | - | GND | - | - | - |
| P10 | GND | - | - | - | GND | - | - | - |
| P11 | GND | - | - | - | GND | - | - | - |
| P12 | GND | - | - | - | GND | - | - | - |
| P13 | GND | - | - | - | GND | - | - | - |
| P14 | GND | - | - | - | GND | - | - | - |
| P15 | GND | - | - | - | GND | - | - | - |
| P8 | GND | - | - | - | GND | - | - | - |
| P9 | GND | - | - | - | GND | - | - | - |
| R14 | GND | - | - | - | GND | - | - | - |
| R9 | GND | - | - | - | GND | - | - | - |
| F10 | VCC | - | - | - | VCC | - | - | - |
| F13 | VCC | - | - | - | VCC | - | - | - |
| G10 | VCC | - | - | - | VCC | - | - | - |
| G13 | VCC | - | - | - | VCC | - | - | - |
| G14 | VCC | - | - | - | VCC | - | - | - |

Lattice Semiconductor Corporation

# LatticeXP Family Data Sheet
# Ordering Information

**December 2005** **Data Sheet DS1001**

## Part Number Description

LFXP XX X – X XXXXXX X

**Device Family**
LatticeXP FPGA

**Logic Capacity**
3K LUTs = 3
6K LUTs = 6
10K LUTs = 10
15K LUTs = 15
20K LUTs = 20

**Supply Voltage**
C = 1.8V/2.5V/3.3V
E = 1.2V

Note: Parts dual marked per table below.

**Grade**
C = Commercial
I = Industrial

**Package**
T100 = 100-pin TQFP
T144 = 144-pin TQFP
Q208 = 208-pin PQFP
F256 = 256-ball fpBGA
F388 = 388-ball fpBGA
F484 = 484-ball fpBGA

TN100 = 100-pin Lead-free TQFP
TN144 = 144-pin Lead-free TQFP
QN208 = 208-pin Lead-free PQFP
FN256 = 256-ball Lead-free fpBGA
FN388 = 388-ball Lead-free fpBGA
FN484 = 484-ball Lead-free fpBGA

**Speed**
3 = Slowest
4
5 = Fastest

## Ordering Information (Contact Factory for Specific Device Availability)

Note:þLatticeXP devices are dual marked. For example, the commercial speed grade LFXP10E-4F256C is also marked with industrial grade -3I (LFXP10E-3F256I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:

### Commercial (Cont.)

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP6E-3F256C | 188 | 1.2V | -3 | fpBGA | 256 | COM | 5.8K |
| LFXP6E-4F256C | 188 | 1.2V | -4 | fpBGA | 256 | COM | 5.8K |
| LFXP6E-5F256C | 188 | 1.2V | -5 | fpBGA | 256 | COM | 5.8K |
| LFXP6E-3Q208C | 142 | 1.2V | -3 | PQFP | 208 | COM | 5.8K |
| LFXP6E-4Q208C | 142 | 1.2V | -4 | PQFP | 208 | COM | 5.8K |
| LFXP6E-5Q208C | 142 | 1.2V | -5 | PQFP | 208 | COM | 5.8K |
| LFXP6E-3T144C | 100 | 1.2V | -3 | TQFP | 144 | COM | 5.8K |
| LFXP6E-4T144C | 100 | 1.2V | -4 | TQFP | 144 | COM | 5.8K |
| LFXP6E-5T144C | 100 | 1.2V | -5 | TQFP | 144 | COM | 5.8K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP10E-3F388C | 244 | 1.2V | -3 | fpBGA | 388 | COM | 9.7K |
| LFXP10E-4F388C | 244 | 1.2V | -4 | fpBGA | 388 | COM | 9.7K |
| LFXP10E-5F388C | 244 | 1.2V | -5 | fpBGA | 388 | COM | 9.7K |
| LFXP10E-3F256C | 188 | 1.2V | -3 | fpBGA | 256 | COM | 9.7K |
| LFXP10E-4F256C | 188 | 1.2V | -4 | fpBGA | 256 | COM | 9.7K |
| LFXP10E-5F256C | 188 | 1.2V | -5 | fpBGA | 256 | COM | 9.7K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP15E-3F484C | 300 | 1.2V | -3 | fpBGA | 484 | COM | 15.5K |
| LFXP15E-4F484C | 300 | 1.2V | -4 | fpBGA | 484 | COM | 15.5K |
| LFXP15E-5F484C | 300 | 1.2V | -5 | fpBGA | 484 | COM | 15.5K |
| LFXP15E-3F388C | 268 | 1.2V | -3 | fpBGA | 388 | COM | 15.5K |
| LFXP15E-4F388C | 268 | 1.2V | -4 | fpBGA | 388 | COM | 15.5K |
| LFXP15E-5F388C | 268 | 1.2V | -5 | fpBGA | 388 | COM | 15.5K |
| LFXP15E-3F256C | 188 | 1.2V | -3 | fpBGA | 256 | COM | 15.5K |
| LFXP15E-4F256C | 188 | 1.2V | -4 | fpBGA | 256 | COM | 15.5K |
| LFXP15E-5F256C | 188 | 1.2V | -5 | fpBGA | 256 | COM | 15.5K |