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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10000
Total RAM Bits	221184
Number of I/O	244
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	388-BBGA
Supplier Device Package	388-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp10c-4f388i

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Figure 2-1. LatticeXP Top Level Block Diagram

PFU and PFF Blocks

The core of the LatticeXP devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of the data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-2. All the interconnections to and from PFU blocks are from routing. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-2. PFU Diagram



Table 2-4. PFU Modes of Operation

Logic Ripple		RAM ¹	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	2-bit Add x 4 SPR16x2 x 4 DPR16x2 x 2	
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR16x4 x 2 DPR16x4 x 1	ROM16x2 x 4
LUT 6x 2 or MUX 8x1 x 2	2-bit Counter x 4	SPR16x8 x 1	ROM16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM16x8 x 1

1. These modes are not available in PFF blocks

Routing

There are many resources provided in the LatticeXP devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal, vertical and diagonal directions. The x2 and x6 resources are buffered allowing both short and long connections routing between PFUs.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock Distribution Network

The clock inputs are selected from external I/O, the sysCLOCK[™] PLLs or routing. These clock inputs are fed through the chip via a clock distribution system.

Primary Clock Sources

LatticeXP devices derive clocks from three primary sources: PLL outputs, dedicated clock inputs and routing. LatticeXP devices have two to four sysCLOCK PLLs, located on the left and right sides of the device. There are four dedicated clock inputs, one on each side of the device. Figure 2-5 shows the 20 primary clock sources.

Figure 2-5. Primary Clock Sources



Note: Smaller devices have two PLLs.

Secondary Clock Sources

LatticeXP devices have four secondary clock resources per quadrant. The secondary clock branches are tapped at every PFU. These secondary clock networks can also be used for controls and high fanout data. These secondary clocks are derived from four clock input pads and 16 routing signals as shown in Figure 2-6.

Lattice Semiconductor

Figure 2-8. Per Quadrant Secondary Clock Selection



Figure 2-9. Slice Clock Selection



sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signals to the feedback divider: from CLKOP (PLL internal), from clock net (CLKOP or CLKOS) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the t_{LOCK} parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

Table 2-6. sysMEM Block Configurations

Memory Mode	Configurations			
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36			
Single Port True Dual Port Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18			
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36			

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

Figure 2-14 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

Hot Socketing Specifications^{1, 2, 3, 4, 5, 6}

Symbol	Parameter	ter Condition		Тур.	Max.	Units
I _{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX.)	-		+/-1000	μΑ

1. Insensitive to sequence of V_{CC} , V_{CCAUX} and V_{CCIO} . However, assumes monotonic rise/fall rates for V_{CC} , V_{CCAUX} and V_{CCIO} . 2. $0 \le V_{CC} \le V_{CC}$ (MAX) or $0 \le V_{CCAUX} \le V_{CCAUX}$ (MAX). 3. $0 \le V_{CCIO} \le V_{CCIO}$ (MAX) for top and bottom I/O banks. 4. $0.2 \le V_{CCIO} \le V_{CCIO}$ (MAX) for left and right I/O banks. 5. I_{DK} is additive to I_{PU} , I_{PW} or I_{BH} . 6. LVCMOS and LVTTL only.

LVPECL

The LatticeXP devices support differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL



	Table 3-3.	LVPECL	DC Condi	tions¹
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Symbol	Description	Typical	Units
Z _{OUT}	Output impedance	100	ohms
R _P	Driver parallel resistor	187	ohms
R _S	Driver series resistor	100	ohms
R _T	Receiver termination	100	ohms
V _{OH}	Output high voltage	2.03	V
V _{OL}	Output low voltage	1.27	V
V _{OD}	Output differential voltage	0.76	V
V _{CM}	Output common mode voltage	1.65	V
Z _{BACK}	Back impedance	85.7	ohms
I _{DC}	DC output current	12.7	mA

Over Recommended Operating Conditions

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

RSDS

The LatticeXP devices support differential RSDS standard. This standard is emulated using complementary LVC-MOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-5. DDR Timings

LatticeXP Internal Timing Parameters¹

		-5		-4		-3		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
PFU/PFF Logic	Mode Timing							
t _{LUT4_PFU}	LUT4 Delay (A to D Inputs to F Output)	—	0.28		0.34		0.40	ns
t _{LUT6_PFU}	LUT6 Delay (A to D Inputs to OFX Output)		0.44		0.53		0.63	ns
t _{LSR_PFU}	Set/Reset to Output of PFU		0.90		1.08		1.29	ns
t _{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.13		0.15		0.19	_	ns
t _{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.04		-0.03	—	-0.03	_	ns
t _{SUD_PFU}	Clock to D Input Setup Time	0.13		0.16		0.19	_	ns
t _{HD_PFU}	Clock to D Input Hold Time	-0.03		-0.02	—	-0.02		ns
t _{CK2Q_PFU}	Clock to Q Delay, D-type Register Configuration		0.40		0.48		0.58	ns
t _{LE2Q_PFU}	Clock to Q Delay Latch Configuration		0.53		0.64		0.76	ns
t _{LD2Q_PFU}	D to Q Throughput Delay when Latch is Enabled	—	0.55		0.66		0.79	ns
PFU Dual Port M	Nemory Mode Timing							
t _{CORAM_PFU}	Clock to Output		0.40		0.48		0.58	ns
t _{SUDATA_PFU}	Data Setup Time	-0.18		-0.14	—	-0.11	_	ns
t _{HDATA_PFU}	Data Hold Time	0.28		0.34	—	0.40	_	ns
t _{SUADDR_PFU}	Address Setup Time	-0.46		-0.37	—	-0.30	_	ns
t _{HADDR_PFU}	Address Hold Time	0.71		0.85	—	1.02	_	ns
t _{SUWREN_PFU}	Write/Read Enable Setup Time	-0.22		-0.17	—	-0.14	_	ns
t _{HWREN_PFU}	Write/Read Enable Hold Time	0.33		0.40	—	0.48	_	ns
PIC Timing								
PIO Input/Outpu	It Buffer Timing							
t _{IN_PIO}	Input Buffer Delay		0.62		0.72		0.85	ns
t _{OUT_PIO}	Output Buffer Delay	—	2.12		2.54		3.05	ns
IOLOGIC Input/	Output Timing							
t _{SUI_PIO}	Input Register Setup Time (Data Before Clock)	1.35		1.83		2.37	_	ns
t _{HI_PIO}	Input Register Hold Time (Data After Clock)	0.05		0.05	—	0.05		ns
t _{COO_PIO}	Output Register Clock to Output Delay		0.36		0.44		0.52	ns
t _{SUCE_PIO}	Input Register Clock Enable Setup Time	-0.09	—	-0.07	—	-0.06	_	ns
t _{HCE_PIO}	Input Register Clock Enable Hold Time	0.13		0.16	—	0.19	_	ns
t _{SULSR_PIO}	Set/Reset Setup Time	0.19		0.23	—	0.28	_	ns
t _{HLSR_PIO}	Set/Reset Hold Time	-0.14	—	-0.11	—	-0.09	_	ns
EBR Timing								
t _{CO_EBR}	Clock to Output from Address or Data		4.01		4.81		5.78	ns
t _{COO_EBR}	Clock to Output from EBR Output Register		0.81		0.97		1.17	ns
t _{SUDATA_EBR}	Setup Data to EBR Memory	-0.26		-0.21	—	-0.17	_	ns
t _{HDATA_EBR}	Hold Data to EBR Memory			0.49	—	0.59	_	ns
t _{SUADDR_EBR}	Setup Address to EBR Memory	-0.26		-0.21	—	-0.17	_	ns
t _{HADDR_EBR}	Hold Address to EBR Memory	0.41	—	0.49	—	0.59	—	ns
t _{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory	-0.17	—	-0.13	—	-0.11	—	ns
t _{HWREN_EBR}	Hold Write/Read Enable to EBR Memory	0.26	—	0.31	—	0.37	—	ns
t _{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.19	—	0.23	—	0.28	—	ns
t _{HCE EBR}	Clock Enable Hold Time to EBR Output Register	-0.13	—	-0.10	—	-0.08	—	ns

Over Recommended Operating Conditions

sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min.	Тур.	Max.	Units
f _{IN}	Input Clock Frequency (CLKI, CLKFB)		25	—	375	MHz
f _{OUT}	Output Clock Frequency (CLKOP, CLKOS)		25	—	375	MHz
f _{OUT2}	K-Divider Output Frequency (CLKOK)		0.195	—	187.5	MHz
f _{VCO}	PLL VCO Frequency		375	—	750	MHz
f _{PFD}	Phase Detector Input Frequency		25	—	—	MHz
AC Characte	eristics					
t _{DT}	Output Clock Duty Cycle	Default duty cycle elected ³	45	50	55	%
t _{PH} ⁴	Output Phase Accuracy		_	—	0.05	UI
. 1	Output Clock Pariod littar	f _{OUT} Š 100MHz	_	—	+/- 125	ps
OPJIT		f _{OUT} < 100MHz	—	—	0.02	UIPP
t _{SK}	Input Clock to Output Clock Skew	Divider ratio = integer	_	—	+/- 200	ps
t _W	Output Clock Pulse Width	At 90% or 10% ³	1	—	_	ns
t _{LOCK} ²	PLL Lock-in Time		—	—	150	us
t _{PA}	Programmable Delay Unit		100	250	400	ps
t _{IPJIT}	Input Clock Period Jitter		_	—	+/- 200	ps
t _{FBKDLY}	External Feedback Delay		—	—	10	ns
t _{HI}	Input Clock High Time	90% to 90%	0.5	—		ns
t _{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t _{RST}	RST Pulse Width		10	_	_	ns

Over Recommended Operating Conditions

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. As compared to CLKOP output.

Timing v.F0.11

LatticeXP "C" Sleep Mode Timing

Parameter	Descriptions		Min.	Тур.	Max.	Units
t _{PWRDN}	SLEEPN Low to I/O Tristate		—	20	32	ns
		LFXP3	—	1.4	2.1	ms
		LFXP6	—	1.7	2.4	ms
t _{PWRUP}	SLEEPN High to Power Up	LFXP10	—	1.1	1.8	ms
		LFXP15	—	1.4	2.1	ms
		LFXP20	—	1.7	2.4	ms
t _{WSLEEPN}	SLEEPN Pulse Width to Initiate Sleep Mode		400	-	—	ns
t _{WAWAKE}	SLEEPN Pulse Rejection		—	_	120	ns

PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO within PIC	Polarity	DDR Strobe (DQS) and Data (DQ) Pins		
P[Edge] [n_4]	A	True	DQ		
	В	Complement	DQ		
P[Edge] [p_3]	A	True	DQ		
	В	Complement	DQ		
P[Edge] [p_2]	A	True	DQ		
	В	Complement	DQ		
P[Edge] [p-1]	A	True	DQ		
P[Edge] [n]					
	В	Complement	DQ		
P[Edge] [n+1]	A	True	[Edge]DQSn		
	В	Complement	DQ		
P[Edge] [n 2]	A	True	DQ		
	В	Complement	DQ		
P[Edge] [n 3]	A	True	DQ		
	В	Complement	DQ		

Notes:

1. "n" is a row/column PIC number.

2. The DDR interface is designed for memories that support one DQS strobe per eight bits of data. In some packages, all the potential DDR data (DQ) pins may not be available.

3. The definition of the PIC numbering is provided in the Signal Names column of the Signal Descriptions table in this data sheet.

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

		LFXP6		LFXP10				
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L15	PR21B	3	C ³	-	PR28B	3	C ³	-
L14	PR21A	3	T ³	-	PR28A	3	T ³	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
L12	PR17B	3	С	-	PR26A	3	-	-
M16	PR20B	3	С	-	PR25B	3	С	RLM0_PLLC_IN_A
N16	PR20A	3	Т	-	PR25A	3	Т	RLM0_PLLT_IN_A
K14	PR19B	3	C ³	-	PR24B	3	C ³	-
K15	PR19A	3	T ³	-	PR24A	3	T ³	DQS
K12	PR17A	3	Т	-	PR23B	3	-	-
K13	PR22A	3	-	VREF2_3	PR22A	3	-	VREF2_3
-	GNDIO3	3	-	-	GNDIO3	3	-	-
L16	PR18B	3	C ³	-	PR21B	3	C ³	-
K16	PR18A	3	T ³	-	PR21A	3	T ³	-
J15	PR16B	3	C ³	-	PR19B	3	C ³	-
J14	PR16A	3	T ³	-	PR19A	3	T ³	-
J13	GNDP1	-	-	-	GNDP1	-	-	-
J12	VCCP1	-	-	-	VCCP1	-	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
J16	PR12B	2	С	PCLKC2_0	PR17B	2	С	PCLKC2_0
H16	PR12A	2	Т	PCLKT2_0	PR17A	2	Т	PCLKT2_0
H13	PR13B	2	C ³	-	PR16B	2	C ³	-
H12	PR13A	2	T ³	-	PR16A	2	T ³	DQS
H15	PR2B	2	C ³	-	PR15B	2	-	-
H14	PR6B	2	-	VREF1_2	PR14A	2	-	VREF1_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G15	PR11B	2	C ³	-	PR13B	2	C ³	-
G14	PR11A	2	T ³	-	PR13A	2	T ³	-
G16	PR8B	2	С	RUM0_PLLC_IN_A	PR12B	2	С	RUM0_PLLC_IN_A
F16	PR8A	2	Т	RUM0_PLLT_IN_A	PR12A	2	Т	RUM0_PLLT_IN_A
G13	PR2A	2	T ³	-	PR11B	2	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G12	PR9B	2	C ³	-	PR8B	2	С	-
F13	PR9A	2	T ³	-	PR8A	2	Т	-
B16	PR7B	2	C ³	-	PR7B	2	C ³	-
C16	PR7A	2	T ³	DQS	PR7A	2	T ³	DQS
F15	PR14A	2	-	-	PR6B	2	-	-
E15	PR5A	2	-	VREF2_2	PR5A	2	-	VREF2_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
F14	PR4B	2	C ³	-	PR4B	2	C ³	-
E14	PR4A	2	T ³	-	PR4A	2	T ³	-
D15	PR3B	2	С	RUM0_PLLC_FB_A	PR3B	2	С	RUM0_PLLC_FB_A
C15	PR3A	2	Т	RUM0_PLLT_FB_A	PR3A	2	Т	RUM0_PLLT_FB_A

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

		LFXP15		LFXP20				
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L4	PL32A	6	-	-	PL36A	6	-	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
K4	PL33A	6	Т	-	PL37A	6	Т	-
K5	PL33B	6	С	-	PL37B	6	С	-
N1	PL35A	6	-	VREF2_6	PL39A	6	-	VREF2_6
N2	PL36B	6	-	-	PL40B	6	-	-
P1	PL37A	6	T ³	DQS	PL41A	6	T ³	DQS
P2	PL37B	6	C³	-	PL41B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
L5	PL38A	6	Т	LLM0_PLLT_FB_A	PL42A	6	Т	LLM0_PLLT_FB_A
M6	PL38B	6	С	LLM0_PLLC_FB_A	PL42B	6	С	LLM0_PLLC_FB_A
M3	PL39A	6	T ³	-	PL43A	6	T ³	-
N3	PL39B	6	C ³	-	PL43B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
P4	SLEEPN ¹ /TOE ²	-	-	-	SLEEPN ¹ /TOE ²	-	-	-
P3	INITN	5	-	-	INITN	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
R4	PB11A	5	Т	-	PB15A	5	Т	-
N5	PB11B	5	С	-	PB15B	5	С	-
P5	PB12A	5	Т	VREF1_5	PB16A	5	Т	VREF1_5
-	GNDIO5	5	-	-	GNDIO5	5	-	-
R1	PB12B	5	С	-	PB16B	5	С	-
N6	PB13A	5	-	-	PB17A	5	-	-
M7	PB14B	5	-	-	PB18B	5	-	-
R2	PB15A	5	Т	DQS	PB19A	5	Т	DQS
T2	PB15B	5	С	-	PB19B	5	С	-
R3	PB16A	5	Т	-	PB20A	5	Т	-
Т3	PB16B	5	С	-	PB20B	5	С	-
T4	PB17A	5	Т	-	PB21A	5	Т	-
R5	PB17B	5	С	VREF2_5	PB21B	5	С	VREF2_5
N7	PB18A	5	Т	-	PB22A	5	Т	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
M8	PB18B	5	С	-	PB22B	5	С	-
T5	PB19A	5	Т	-	PB23A	5	Т	-
P6	PB19B	5	С	-	PB23B	5	С	-
T6	PB20A	5	Т	-	PB24A	5	Т	-
R6	PB20B	5	С	-	PB24B	5	С	-
P7	PB21A	5	-	-	PB25A	5	-	-
N8	PB22B	5	-	-	PB26B	5	-	-
R7	PB23A	5	Т	DQS	PB27A	5	Т	DQS

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

	LFXP10				LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
AA20	PB36B	4	С	-	PB41B	4	С	-	PB45B	4	С	-
AB21	PB37A	4	Т	-	PB42A	4	Т	-	PB46A	4	Т	-
AA21	PB37B	4	С	-	PB42B	4	С	-	PB46B	4	С	-
AA22	PB38A	4	Т	-	PB43A	4	Т	-	PB47A	4	Т	-
Y21	PB38B	4	С	-	PB43B	4	С	-	PB47B	4	С	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
W16	PB39A	4	-	-	PB44A	4	Т	-	PB48A	4	Т	-
W17	-	-	-	-	PB44B	4	С	-	PB48B	4	С	-
Y15	-	-	-	-	PB45A	4	-	-	PB49A	4	-	-
Y16	-	-	-	-	PB46B	4	-	-	PB50B	4	-	-
W19	-	-	-	-	PB47A	4	Т	DQS	PB51A	4	Т	DQS
W18	-	-	-	-	PB47B	4	С	-	PB51B	4	С	-
W20	-	-	-	-	PB48A	4	-	-	PB52A	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
T20	PR35B	3	C ³	-	PR39B	3	C ³	-	PR43B	3	C ³	-
T19	PR35A	3	T ³	-	PR39A	3	T ³	-	PR43A	3	T ³	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
U19	PR34B	3	С	RLM0_PLLC_FB_A	PR38B	3	С	RLM0_PLLC_FB_A	PR42B	3	С	RLM0_PLLC_FB_A
U20	PR34A	3	Т	RLM0_PLLT_FB_A	PR38A	3	Т	RLM0_PLLT_FB_A	PR42A	3	Т	RLM0_PLLT_FB_A
V19	PR33B	3	C ³	-	PR37B	3	C ³	-	PR41B	3	C ³	-
V20	PR33A	3	T ³	DQS	PR37A	3	T ³	DQS	PR41A	3	T ³	DQS
R19	PR32B	3	-	-	PR36B	3	-	-	PR40B	3	-	-
R20	PR31A	3	-	VREF1_3	PR35A	3	-	VREF1_3	PR39A	3	-	VREF1_3
W21	PR30B	3	C ³	-	PR34B	3	C ³	-	PR38B	3	C ³	-
Y22	PR30A	3	T ³	-	PR34A	3	T ³	-	PR38A	3	Т³	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
P19	PR29B	3	С	-	PR33B	3	С	-	PR37B	3	С	-
P20	PR29A	3	Т	-	PR33A	3	Т	-	PR37A	3	Т	-
V21	PR28B	3	C ³	-	PR32B	3	C ³	-	PR36B	3	C ³	-
W22	PR28A	3	T ³	-	PR32A	3	T ³	-	PR36A	3	Т³	-
U21	PR26B	3	C ³	-	PR30B	3	C ³	-	PR34B	3	C ³	-
V22	PR26A	3	T ³	-	PR30A	3	T ³	-	PR34A	3	T ³	-
T21	PR25B	3	С	RLM0_PLLC_IN_A	PR29B	3	С	RLM0_PLLC_IN_A	PR33B	3	С	RLM0_PLLC_IN_A
U22	PR25A	3	т	RLM0_PLLT_IN_A	PR29A	3	Т	RLM0_PLLT_IN_A	PR33A	3	Т	RLM0_PLLT_IN_A
-	GNDIO3	3	-		GNDIO3	3	-		GNDIO3	3	-	
R21	PR24B	3	C ³	-	PR28B	3	C ³	-	PR32B	3	C ³	-
T22	PR24A	3	T ³	DQS	PR28A	3	T ³	DQS	PR32A	3	T ³	DQS
N19	PR23B	3	-	-	PR27B	3	-	-	PR31B	3	-	-
N20	PR22A	3	-	VREF2 3	PR26A	3	-	VREF2 3	PR30A	3	-	VREF2 3
R22	PR21B	3	C ³	-	PR25B	3	C ³	-	PR29B	3	C ³	-
P22	PR21A	3	T ³	-	PR25A	3	T ³	-	PR29A	3	T ³	-
P21	PR20B	3	С	_	PR24B	3	С	-	PR28B	3	С	-
N21	PR20A	3	T	-	PR24A	3	T	-	PR28A	3	T	-
	GNDIO3	3	<u>-</u>	_	GNDIO3	3	-	_	GNDIO3	3	-	-
M20	PR19B	3	C3	_	PB23B	3	C ³	-	PR27B	3	C ³	-
M19	PR19A	3	т ³	_	PR23A	3	T ³	_	PR27A	3	T ³	-
N22	GNDP1	-	<u>-</u>		GNDP1	-	-	_	GNDP1	-	-	-
1122	GINDET	<u> </u>	l -			1	-		GNDET	-	-	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

	LFXP10)	LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
C20	PT38A	1	Т	-	PT43A	1	Т	-	PT47A	1	Т	-
C21	PT37B	1	С	-	PT42B	1	С	-	PT46B	1	С	-
C22	PT37A	1	Т	-	PT42A	1	Т	-	PT46A	1	Т	-
B22	PT36B	1	С	-	PT41B	1	С	-	PT45B	1	С	-
A21	PT36A	1	Т	-	PT41A	1	Т	-	PT45A	1	Т	-
D15	PT35B	1	С	-	PT40B	1	С	-	PT44B	1	С	-
D14	PT35A	1	Т	-	PT40A	1	Т	-	PT44A	1	Т	-
B21	PT34B	1	С	VREF1_1	PT39B	1	С	VREF1_1	PT43B	1	С	VREF1_1
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
A20	PT34A	1	Т	DQS	PT39A	1	Т	DQS	PT43A	1	Т	DQS
B20	PT33B	1	-	-	PT38B	1	-	-	PT42B	1	-	-
A19	PT32A	1	-	-	PT37A	1	-	-	PT41A	1	-	-
B19	PT31B	1	С	-	PT36B	1	С	-	PT40B	1	С	-
A18	PT31A	1	Т	-	PT36A	1	Т	-	PT40A	1	Т	-
C14	PT30B	1	С	-	PT35B	1	С	-	PT39B	1	С	-
C13	PT30A	1	Т	D0	PT35A	1	Т	D0	PT39A	1	Т	D0
B18	PT29B	1	С	D1	PT34B	1	С	D1	PT38B	1	С	D1
A17	PT29A	1	Т	VREF2_1	PT34A	1	Т	VREF2_1	PT38A	1	Т	VREF2_1
B17	PT28B	1	С	-	PT33B	1	С	-	PT37B	1	С	-
A16	PT28A	1	Т	D2	PT33A	1	Т	D2	PT37A	1	Т	D2
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
B16	PT27B	1	С	D3	PT32B	1	С	D3	PT36B	1	С	D3
A15	PT27A	1	Т	-	PT32A	1	Т	-	PT36A	1	Т	-
B15	PT26B	1	С	-	PT31B	1	С	-	PT35B	1	С	-
A14	PT26A	1	Т	DQS	PT31A	1	Т	DQS	PT35A	1	Т	DQS
D13	PT25B	1	-	-	PT30B	1	-	-	PT34B	1	-	-
D12	PT24A	1	-	D4	PT29A	1	-	D4	PT33A	1	-	D4
B14	PT23B	1	С	-	PT28B	1	С	-	PT32B	1	С	-
A13	PT23A	1	Т	D5	PT28A	1	Т	D5	PT32A	1	Т	D5
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
B13	PT22B	1	С	D6	PT27B	1	С	D6	PT31B	1	С	D6
A12	PT22A	1	Т	-	PT27A	1	Т	-	PT31A	1	Т	-
B12	PT21B	1	С	D7	PT26B	1	С	D7	PT30B	1	С	D7
C12	PT21A	1	Т	-	PT26A	1	Т	-	PT30A	1	Т	-
C11	PT20B	0	С	BUSY	PT25B	0	С	BUSY	PT29B	0	С	BUSY
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
B11	PT20A	0	Т	CS1N	PT25A	0	Т	CS1N	PT29A	0	Т	CS1N
A11	PT19B	0	С	PCLKC0_0	PT24B	0	С	PCLKC0_0	PT28B	0	С	PCLKC0_0
A10	PT19A	0	Т	PCLKT0_0	PT24A	0	Т	PCLKT0_0	PT28A	0	Т	PCLKT0_0
B10	PT18B	0	С	-	PT23B	0	С	-	PT27B	0	С	-
B9	PT18A	0	Т	DQS	PT23A	0	Т	DQS	PT27A	0	Т	DQS
D11	PT17B	0	-	-	PT22B	0	-	-	PT26B	0	-	-
D10	PT16A	0	-	DOUT	PT21A	0	-	DOUT	PT25A	0	-	DOUT
A9	PT15B	0	С	-	PT20B	0	С	-	PT24B	0	С	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C8	PT15A	0	Т	WRITEN	PT20A	0	Т	WRITEN	PT24A	0	Т	WRITEN
B8	PT14B	0	С	-	PT19B	0	С	-	PT23B	0	С	-
A8	PT14A	0	Т	VREF1_0	PT19A	0	Т	VREF1_0	PT23A	0	Т	VREF1_0
C7	PT13B	0	С	-	PT18B	0	С	-	PT22B	0	С	-
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LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA

			LFXP15		LFXP20				
Ball	Ball			Dual	Ball			Dual	
Number	Function	Bank	Differential	Function	Function	Bank	Differential	Function	
F5	PROGRAMN	7	-	-	PROGRAMN	7	-	-	
E3	CCLK	7	-	-	CCLK	7	-	-	
C1	PL2B	7	-	-	PL2B	7	-	-	
-	GNDIO7	7	-	-	GNDIO7	7	-	-	
G5	PL3A	7	T³	-	PL3A	7	T ³	-	
G6	PL3B	7	C ³	-	PL3B	7	C ³	-	
F4	PL4A	7	Т	-	PL4A	7	Т	-	
F3	PL4B	7	С	-	PL4B	7	С	-	
G4	PL5A	7	T ³	-	PL5A	7	T ³	-	
G3	PL5B	7	C ³	-	PL5B	7	C ³	-	
D1	PL6A	7	T ³	-	PL6A	7	T ³	-	
D2	PL6B	7	C ³	-	PL6B	7	C ³	-	
-	GNDIO7	7	-	-	GNDIO7	7	-	-	
E1	PL7A	7	Т	LUM0_PLLT_FB_A	PL7A	7	Т	LUM0_PLLT_FB_A	
E2	PL7B	7	С	LUM0_PLLC_FB_A	PL7B	7	С	LUM0_PLLC_FB_A	
H5	PL8A	7	T ³	-	PL8A	7	T ³	-	
H6	PL8B	7	C ³	-	PL8B	7	C ³	-	
H4	PL9A	7	-	-	PL9A	7	-	-	
H3	PL10B	7	-	VREF1_7	PL10B	7	-	VREF1_7	
F1	PL11A	7	T ³	DQS	PL11A	7	T ³	DQS	
F2	PL11B	7	C ³	-	PL11B	7	C ³	-	
-	GNDIO7	7	-	-	GNDIO7	7	-	-	
J5	PL12A	7	Т	-	PL12A	7	Т	-	
J6	PL12B	7	С	-	PL12B	7	С	-	
G1	PL13A	7	T ³	-	PL13A	7	T ³	-	
G2	PL13B	7	C ³	-	PL13B	7	C ³	-	
J4	PL15A	7	T ³	-	PL15A	7	T ³	-	
J3	PL15B	7	C ³	-	PL15B	7	C ³	-	
-	GNDIO7	7	-	-	GNDIO7	7	-	-	
H1	PL16A	7	Т	LUMO PLLT IN A	PL16A	7	Т	LUMO PLLT IN A	
H2	PL16B	7	С	LUMO PLLC IN A	PL16B	7	С	LUMO PLLC IN A	
	PL17A	7	T ³	-	PL17A	7	T ³	•	
J2	PL17B	7	C ³	-	PL17B	7	C ³	-	
K3	PL18A	7	-	VREF2_7	PL18A	7	-	VREF2_7	
K2	PL19B	7	-	-	PL19B	7	-	-	
K4	PL20A	7	T ³	DOS	PI 20A	7	T ³	DOS	
-	GNDIO7	7	-		GNDIO7	7	-		
K5	PI 20B	7	C ³	-	PI 20B	7	C ³		
K1	PI 21A	7	т	-	PI 21A	7	т	-	
12	PI 21R	7	, C		PI 21R	7	C.	_	
	PI 224	7	т ³		PI 224	7	т ³		
12		7		-		7		-	
LO	FL22D	1	0	-	FL22D	1	0	-	

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

	LFXP15				LFXP20				
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function	
L1	-	-	-	-	PL23A	7	T³	-	
M1	-	-	-	-	PL23B	7	C ³	-	
M2	-	-	-	-	PL24A	7	-	-	
L5	VCCP0	-	-	-	VCCP0	-	-	-	
N2	GNDP0	-	-	-	GNDP0	-	-	-	
N1	-	-	-	-	PL25B	6	-	-	
P2	-	-	-	-	PL26A	6	T ³	-	
P1	-	-	-	-	PL26B	6	C ³	-	
M4	PL23A	6	T ³	-	PL27A	6	T ³	-	
М3	PL23B	6	C ³	-	PL27B	6	C ³	-	
R2	PL24A	6	Т	PCLKT6_0	PL28A	6	Т	PCLKT6_0	
-	GNDIO6	6	-	-	GNDIO6	6	-	-	
R1	PL24B	6	С	PCLKC6_0	PL28B	6	С	PCLKC6_0	
N3	PL25A	6	Τ³	-	PL29A	6	Τ³	-	
N4	PL25B	6	C ³	-	PL29B	6	C ³	-	
M5	PL26A	6	-	-	PL30A	6	-	-	
N5	PL27B	6	-	VREF1_6	PL31B	6	-	VREF1_6	
T2	PL28A	6	Τ³	DQS	PL32A	6	Τ³	DQS	
T1	PL28B	6	C ³	-	PL32B	6	C ³	-	
-	GNDIO6	6	-	-	GNDIO6	6	-	-	
U2	PL29A	6	Т	LLM0_PLLT_IN_A	PL33A	6	Т	LLM0_PLLT_IN_A	
U1	PL29B	6	С	LLM0_PLLC_IN_A	PL33B	6	С	LLM0_PLLC_IN_A	
P3	PL30A	6	Τ³	-	PL34A	6	Τ³	-	
P4	PL30B	6	C ³	-	PL34B	6	C ³	-	
P6	PL32A	6	Τ³	-	PL36A	6	T³	-	
P5	PL32B	6	C ³	-	PL36B	6	C ³	-	
-	GNDIO6	6	-	-	GNDIO6	6	-	-	
V2	PL33A	6	Т	-	PL37A	6	Т	-	
V1	PL33B	6	С	-	PL37B	6	С	-	
W2	PL34A	6	Τ³	-	PL38A	6	Τ³	-	
W1	PL34B	6	C ³	-	PL38B	6	C ³	-	
R3	PL35A	6	-	VREF2_6	PL39A	6	-	VREF2_6	
R4	PL36B	6	-	-	PL40B	6	-	-	
R6	PL37A	6	Τ³	DQS	PL41A	6	T³	DQS	
R5	PL37B	6	C ³	-	PL41B	6	C ³	-	
-	GNDIO6	6	-	-	GNDIO6	6	-	-	
Y2	PL38A	6	Т	LLM0_PLLT_FB_A	PL42A	6	Т	LLM0_PLLT_FB_A	
Y1	PL38B	6	С	LLM0_PLLC_FB_A	PL42B	6	С	LLM0_PLLC_FB_A	
Т3	PL39A	6	T³	-	PL43A	6	T³	-	
T4	PL39B	6	C ³	-	PL43B	6	C ³	-	
W3	PL40A	6	T ³	-	PL44A	6	T ³	-	
V3	PL40B	6	C ³	-	PL44B	6	C ³	-	

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

	LFXP15				LFXP20					
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function		
AB5	PB16A	5	Т	-	PB20A	5	Т	-		
AB6	PB16B	5	С	-	PB20B	5	C	-		
AA8	PB17A	5	Т	-	PB21A	5	Т	-		
AA9	PB17B	5	С	VREF2_5	PB21B	5	C	VREF2_5		
W10	PB18A	5	Т	-	PB22A	5	Т	-		
-	GNDIO5	5	-	-	GNDIO5	5	-	-		
V10	PB18B	5	С	-	PB22B	5	C	-		
AB7	PB19A	5	Т	-	PB23A	5	Т	-		
AB8	PB19B	5	С	-	PB23B	5	C	-		
AB9	PB20A	5	Т	-	PB24A	5	Т	-		
AB10	PB20B	5	С	-	PB24B	5	С	-		
Y10	PB21A	5	-	-	PB25A	5	-	-		
AA10	PB22B	5	-	-	PB26B	5	-	-		
W11	PB23A	5	Т	DQS	PB27A	5	Т	DQS		
V11	PB23B	5	С	-	PB27B	5	С	-		
-	GNDIO5	5	-	-	GNDIO5	5	-	-		
Y11	PB24A	5	Т	-	PB28A	5	Т	-		
AA11	PB24B	5	С	-	PB28B	5	С	-		
AB11	PB25A	5	Т	-	PB29A	5	Т	-		
AB12	PB25B	5	С	-	PB29B	5	С	-		
Y12	PB26A	4	Т	-	PB30A	4	Т	-		
AA12	PB26B	4	С	-	PB30B	4	С	-		
W12	PB27A	4	Т	PCLKT4_0	PB31A	4	Т	PCLKT4_0		
V12	PB27B	4	С	PCLKC4_0	PB31B	4	С	PCLKC4_0		
-	GNDIO4	4	-	-	GNDIO4	4	-	-		
AB13	PB28A	4	Т	-	PB32A	4	Т	-		
AB14	PB28B	4	С	-	PB32B	4	С	-		
AA13	PB29A	4	-	-	PB33A	4	-	-		
Y13	PB30B	4	-	-	PB34B	4	-	-		
AB15	PB31A	4	Т	DQS	PB35A	4	Т	DQS		
AB16	PB31B	4	С	VREF1_4	PB35B	4	С	VREF1_4		
V13	PB32A	4	Т	-	PB36A	4	Т	-		
W13	PB32B	4	С	-	PB36B	4	С	-		
AA14	PB33A	4	Т	-	PB37A	4	Т	-		
-	GNDIO4	4	-	-	GNDIO4	4	-	-		
AA15	PB33B	4	С	-	PB37B	4	С	-		
AB17	PB34A	4	Т	-	PB38A	4	Т	-		
AB18	PB34B	4	С	-	PB38B	4	С	-		
W14	PB35A	4	Т	-	PB39A	4	Т	-		
Y14	PB35B	4	С	-	PB39B	4	С	-		
U14	PB36A	4	Т	VREF2 4	PB40A	4	Т	VREF2 4		
V14	PB36B	4	С	-	PB40B	4	С	-		
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LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

	LFXP15				LFXP20					
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function		
R18	PR38B	3	С	RLM0_PLLC_FB_A	PR42B	3	С	RLM0_PLLC_FB_A		
R17	PR38A	3	Т	RLM0_PLLT_FB_A	PR42A	3	Т	RLM0_PLLT_FB_A		
Y22	PR37B	3	C ³	-	PR41B	3	C ³	-		
Y21	PR37A	3	T ³	DQS	PR41A	3	T ³	DQS		
W22	PR36B	3	-	-	PR40B	3	-	-		
W21	PR35A	3	-	VREF1_3	PR39A	3	-	VREF1_3		
P17	PR34B	3	C ³	-	PR38B	3	C ³	-		
P18	PR34A	3	T ³	-	PR38A	3	T ³	-		
-	GNDIO3	3	-	-	GNDIO3	3	-	-		
R19	PR33B	3	С	-	PR37B	3	С	-		
R20	PR33A	3	Т	-	PR37A	3	Т	-		
V22	PR32B	3	C ³	-	PR36B	3	C ³	-		
V21	PR32A	3	T ³	-	PR36A	3	T ³	-		
U22	PR30B	3	C ³	-	PR34B	3	C ³	-		
U21	PR30A	3	T ³	-	PR34A	3	T ³	-		
P19	PR29B	3	С	RLM0_PLLC_IN_A	PR33B	3	С	RLM0_PLLC_IN_A		
P20	PR29A	3	Т	RLM0_PLLT_IN_A	PR33A	3	Т	RLM0_PLLT_IN_A		
-	GNDIO3	3	-	-	GNDIO3	3	-	-		
T22	PR28B	3	C ³	-	PR32B	3	C ³	-		
T21	PR28A	3	T ³	DQS	PR32A	3	T ³	DQS		
R22	PR27B	3	-	-	PR31B	3	-	-		
R21	PR26A	3	-	VREF2_3	PR30A	3	-	VREF2_3		
N19	PR25B	3	C ³	-	PR29B	3	C ³	-		
N20	PR25A	3	T ³	-	PR29A	3	T ³	-		
N18	PR24B	3	С	-	PR28B	3	С	-		
M18	PR24A	3	Т	-	PR28A	3	Т	-		
-	GNDIO3	3	-	-	GNDIO3	3	-	-		
P22	PR23B	3	C ³	-	PR27B	3	C ³	-		
P21	PR23A	3	T ³	-	PR27A	3	T ³	-		
N22	-	-	-	-	PR26B	3	C ³	-		
N21	-	-	-	-	PR26A	3	T ³	-		
M19	-	-	-	-	PR25B	3	-	-		
M20	GNDP1	-	-	-	GNDP1	-	-	-		
L18	VCCP1	-	-	-	VCCP1	-	-	-		
M21	-	-	-	-	PR24A	2	-	-		
M22	PR22B	2	C ³	-	PR23B	2	C ³	-		
L22	PR22A	2	T ³	-	PR23A	2	T ³	-		
-	GNDIO2	2	-	-	GNDIO2	2	-	-		
L19	-	-	-	-	PR22B	2	C ³	-		
L20	-	-	-	-	PR22A	2	T ³	-		
L21	PR21B	2	С	PCLKC2_0	PR21B	2	С	PCLKC2_0		
K22	PR21A	2	Т	PCLKT2_0	PR21A	2	Т	PCLKT2_0		

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Part Number	l/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6E-3F256C	188	1.2V	-3	fpBGA	256	COM	5.8K
LFXP6E-4F256C	188	1.2V	-4	fpBGA	256	COM	5.8K
LFXP6E-5F256C	188	1.2V	-5	fpBGA	256	COM	5.8K
LFXP6E-3Q208C	142	1.2V	-3	PQFP	208	COM	5.8K
LFXP6E-4Q208C	142	1.2V	-4	PQFP	208	COM	5.8K
LFXP6E-5Q208C	142	1.2V	-5	PQFP	208	COM	5.8K
LFXP6E-3T144C	100	1.2V	-3	TQFP	144	COM	5.8K
LFXP6E-4T144C	100	1.2V	-4	TQFP	144	COM	5.8K
LFXP6E-5T144C	100	1.2V	-5	TQFP	144	COM	5.8K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10E-3F388C	244	1.2V	-3	fpBGA	388	COM	9.7K
LFXP10E-4F388C	244	1.2V	-4	fpBGA	388	COM	9.7K
LFXP10E-5F388C	244	1.2V	-5	fpBGA	388	COM	9.7K
LFXP10E-3F256C	188	1.2V	-3	fpBGA	256	COM	9.7K
LFXP10E-4F256C	188	1.2V	-4	fpBGA	256	COM	9.7K
LFXP10E-5F256C	188	1.2V	-5	fpBGA	256	COM	9.7K

Part Number	l/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15E-3F484C	300	1.2V	-3	fpBGA	484	COM	15.5K
LFXP15E-4F484C	300	1.2V	-4	fpBGA	484	COM	15.5K
LFXP15E-5F484C	300	1.2V	-5	fpBGA	484	COM	15.5K
LFXP15E-3F388C	268	1.2V	-3	fpBGA	388	COM	15.5K
LFXP15E-4F388C	268	1.2V	-4	fpBGA	388	COM	15.5K
LFXP15E-5F388C	268	1.2V	-5	fpBGA	388	COM	15.5K
LFXP15E-3F256C	188	1.2V	-3	fpBGA	256	COM	15.5K
LFXP15E-4F256C	188	1.2V	-4	fpBGA	256	COM	15.5K
LFXP15E-5F256C	188	1.2V	-5	fpBGA	256	COM	15.5K

Commercial (Cont.)