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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 10000 |
| Total RAM Bits | 221184 |
| Number of I/O | 188 |
| Number of Gates | - |
| Voltage - Supply | 1.71V ~ 3.465V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 256-BGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp10c-5f256c |

## Introduction

The LatticeXP family of FPGA devices combine logic gates, embedded memory and high performance I/Os in a single architecture that is both non-volatile and infinitely reconfigurable to support cost-effective system designs.

The re-programmable non-volatile technology used in the LatticeXP family is the next generation ispXP™ technology. With this technology, expensive external configuration memories are not required and designs are secured from unauthorized read-back. In addition, instant-on capability allows for easy interfacing in many applications.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeXP family of FPGA devices. Synthesis library support for LatticeXP is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeXP device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeXP family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

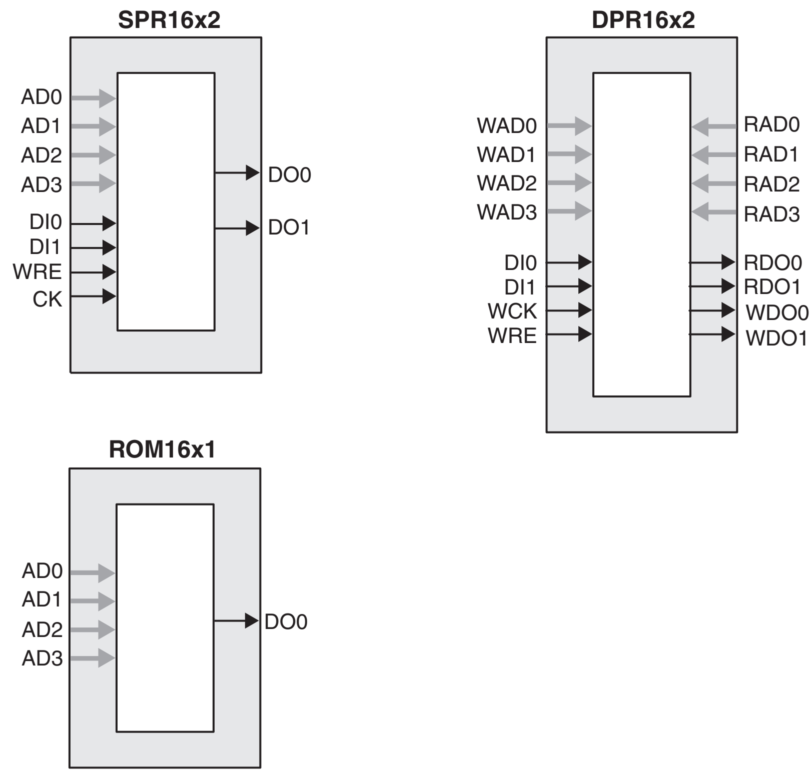
The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-4 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices, one Slice functions as the read-write port. The other companion Slice supports the read-only port. For more information on RAM mode in LatticeXP devices, please see details of additional technical documentation at the end of this data sheet.

***Table 2-3. Number of Slices Required for Implementing Distributed RAM***

| | SPR16x2 | DPR16x2 |
|---|---|---|
| Number of Slices | 1 | 2 |

Note: SPR = Single Port RAM, DPR = Dual Port RAM

***Figure 2-4. Distributed Memory Primitives***




**ROM Mode:** The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

### PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

*Table 2-6. sysMEM Block Configurations*

| Memory Mode | Configurations |
|---|---|
| Single Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18<br>256 x 36 |
| True Dual Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18 |
| Pseudo Dual Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18<br>256 x 36 |

## Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

## RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

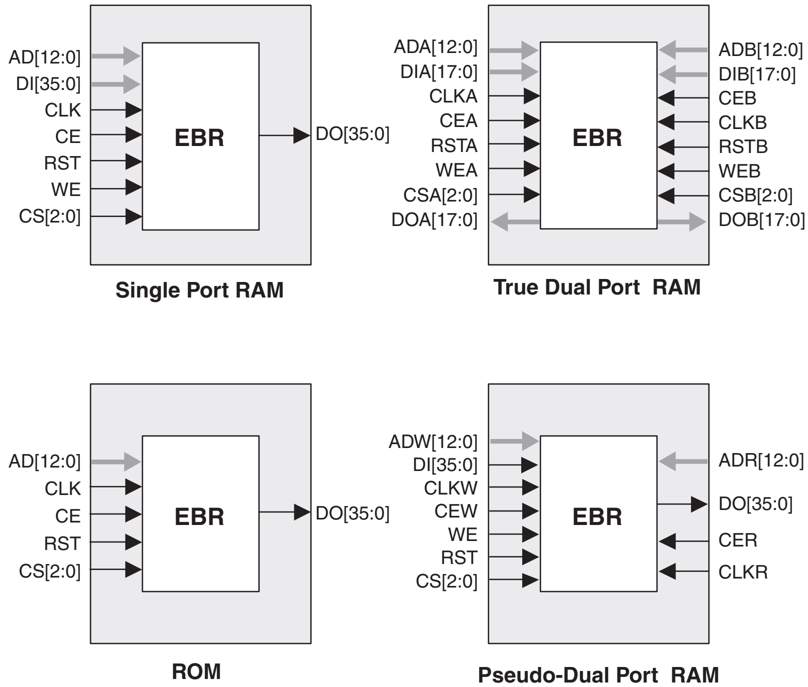
## Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

## Single, Dual and Pseudo-Dual Port Modes

Figure 2-14 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

*Figure 2-14. sysMEM Memory Primitives*



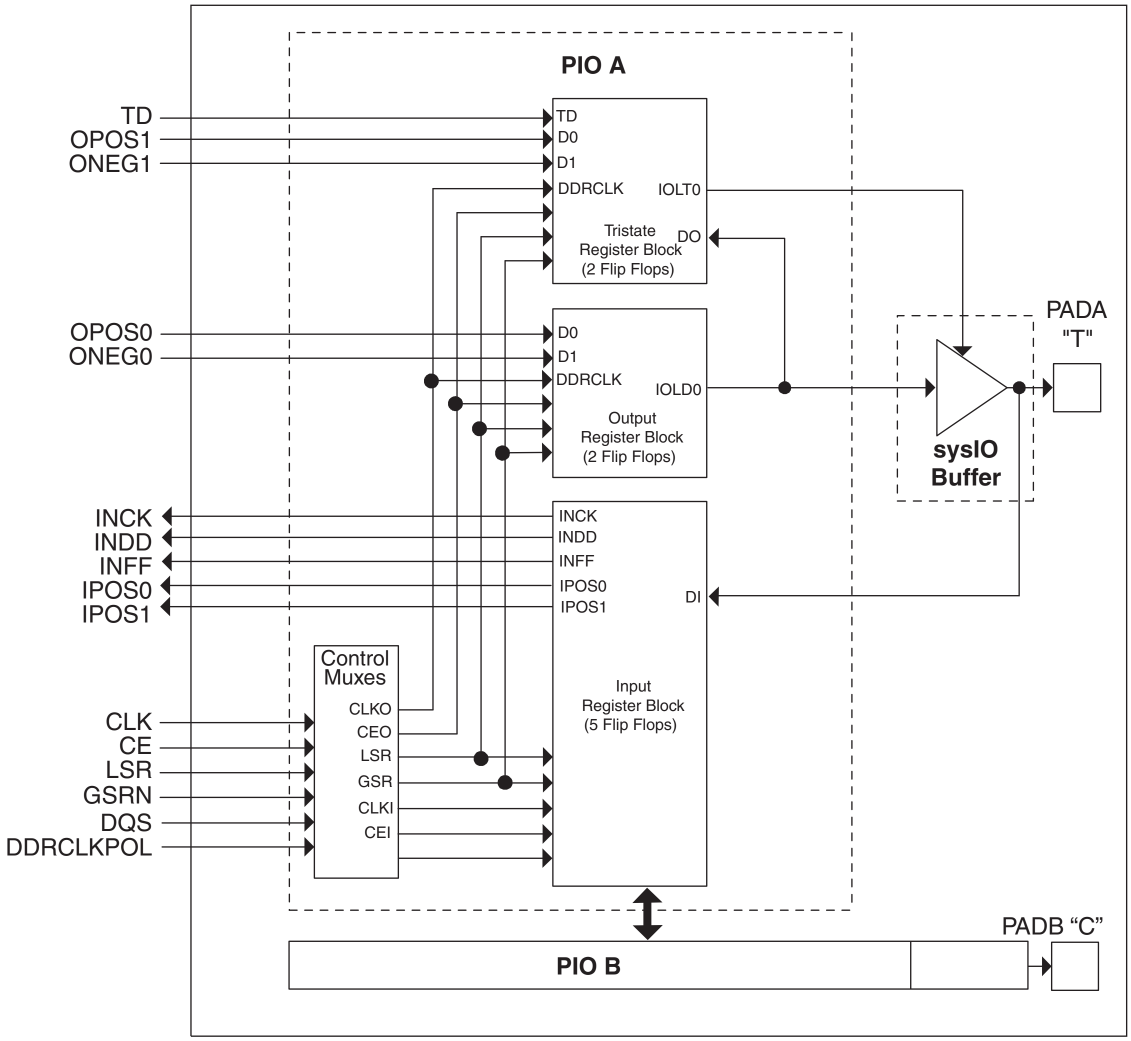

The EBR memory supports three forms of write behavior for single port or dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** -þa copy of the input data appears at the output of the same port during a write cycle.þThis mode is supported for all data widths.
3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

## Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-15.

*Figure 2-17. PIC Diagram*




In the LatticeXP family, seven PIOs or four (3.5) PICs are grouped together to provide two LVDS differential pairs, one PIC pair and one single I/O, as shown in Figure 2-18.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as "T" and "C"). The PAD Labels "T" and "C" distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 14 PIOs (a group of 8 PICs) contains a delay element to facilitate the generation of DQS signals as shown in Figure 2-19. The DQS signal feeds the DQS bus which spans the set of 13 PIOs (8 PICs). The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table in this data sheet.

### Polarity Control Logic

In a typical DDR Memory interface design, the phase relation between the incoming delayed DQS strobe and the internal system Clock (during the READ cycle) is unknown.

The LatticeXP family contains dedicated circuits to transfer data between these domains. To prevent setup and hold violations at the domain transfer between DQS (delayed) and the system Clock a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of the each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.

## sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in eight groups referred to as Banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

**sysIO Buffer Banks**

LatticeXP devices have eight sysIO buffer banks; each is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage ($V_{CCIO}$), and two voltage references $V_{REF1}$ and $V_{REF2}$ resources allowing each bank to be completely independent from each other. Figure 2-28 shows the eight banks and their associated supplies.

In the LatticeXP devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS, PCI and PCI-X) are powered using $V_{CCIO}$. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as a fixed threshold input independent of $V_{CCIO}$. In addition to the bank $V_{CCIO}$ supplies, the LatticeXP devices have a $V_{CC}$ core logic power supply, and a $V_{CCAUX}$ supply that power all differential and referenced buffers.

Each bank can support up to two separate VREF voltages, VREF1 and VREF2 that set the threshold for the referenced input buffers. In the LatticeXP devices, a dedicated pin in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

# DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}, I_{IH}$[1, 2, 4] | Input or I/O Leakage | $0 \le V_{IN} \le (V_{CCIO} - 0.2V)$ | — | — | 10 | µA |
| | | $(V_{CCIO} - 0.2V) < V_{IN} \le 3.6V$ | — | — | 40 | µA |
| $I_{PU}$ | I/O Active Pull-up Current | $0 \le V_{IN} \le 0.7\ V_{CCIO}$ | -30 | — | -150 | µA |
| $I_{PD}$ | I/O Active Pull-down Current | $V_{IL}$ (MAX) $\le V_{IN} \le V_{IH}$ (MAX) | 30 | — | 150 | µA |
| $I_{BHLS}$ | Bus Hold Low sustaining current | $V_{IN} = V_{IL}$ (MAX) | 30 | — | — | µA |
| $I_{BHHS}$ | Bus Hold High sustaining current | $V_{IN} = 0.7V_{CCIO}$ | -30 | — | — | µA |
| $I_{BHLO}$ | Bus Hold Low Overdrive current | $0 \le V_{IN} \le V_{IH}$ (MAX) | — | — | 150 | µA |
| $I_{BHHO}$ | Bus Hold High Overdrive current | $0 \le V_{IN} \le V_{IH}$ (MAX) | — | — | -150 | µA |
| $V_{BHT}$ | Bus Hold trip Points | $0 \le V_{IN} \le V_{IH}$ (MAX) | $V_{IL}$ (MAX) | — | $V_{IH}$ (MIN) | V |
| C1 | I/O Capacitance[3] | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, $V_{CC}$ = 1.2V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 8 | — | pf |
| C2 | Dedicated Input Capacitance[3] | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, $V_{CC}$ = 1.2V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 8 | — | pf |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. Not applicable to SLEEPN/TOE pin.
3. $T_A$ 25°C, f = 1.0MHz
4. When $V_{IH}$ is higher than $V_{CCIO}$, a transient current typically of 30ns in duration or less with a peak current of 6mA can be expected on the high-to-low transition.

# Supply Current (Sleep Mode)[1, 2, 3]

| Symbol | Parameter | Device | Typ.[4] | Max | Units |
|---|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LFXP3C | 12 | 65 | µA |
| | | LFXP6C | 14 | 75 | µA |
| | | LFXP10C | 16 | 85 | µA |
| | | LFXP15C | 18 | 95 | µA |
| | | LFXP20C | 20 | 105 | µA |
| $I_{CCP}$ | PLL Power Supply (per PLL) | All LFXP 'C' Devices | 1 | 5 | µA |
| $I_{CCAUX}$ | Auxiliary Power Supply | LFXP3C | 2 | 90 | µA |
| | | LFXP6C | 2 | 100 | µA |
| | | LFXP10C | 2 | 110 | µA |
| | | LFXP15C | 3 | 120 | µA |
| | | LFXP20C | 4 | 130 | µA |
| $I_{CCIO}$ | Bank Power Supply[5] | LFXP3C | 2 | 20 | µA |
| | | LFXP6C | 2 | 22 | µA |
| | | LFXP10C | 2 | 24 | µA |
| | | LFXP15C | 3 | 27 | µA |
| | | LFXP20C | 4 | 30 | µA |
| $I_{CCJ}$ | VCCJ Power Supply | All LFXP 'C' Devices | 1 | 5 | µA |

1. Assumes all inputs are configured as LVCMOS and held at the VCCIO or GND.
2. Frequency 0MHz.
3. User pattern: blank.
4. $T_A$=25°C, power supplies at nominal voltage.
5. Per bank.

## Supply Current (Standby)[1, 2, 3, 4]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typ.[5] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LFXP3E | 15 | mA |
| | | LFXP6E | 20 | mA |
| | | LFXP10E | 35 | mA |
| | | LFXP15E | 45 | mA |
| | | LFXP20E | 55 | mA |
| | | LFXP3C | 35 | mA |
| | | LFXP6C | 40 | mA |
| | | LFXP10C | 70 | mA |
| | | LFXP15C | 80 | mA |
| | | LFXP20C | 90 | mA |
| $I_{CCP}$ | PLL Power Supply (per PLL) | All | 8 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply $V_{CCAUX}$ = 3.3V | LFXP3E/C | 22 | mA |
| | | LFXP6E/C | 22 | mA |
| | | LFXP10E/C | 30 | mA |
| | | LFXP15E/C | 30 | mA |
| | | LFXP20E/C | 30 | mA |
| $I_{CCIO}$ | Bank Power Supply[6] | All | 2 | mA |
| $I_{CCJ}$ | $V_{CCJ}$ Power Supply | All | 1 | mA |

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the VCCIO or GND.
3. Frequency 0MHz.
4. User pattern: blank.
5. $T_A$=25°C, power supplies at nominal voltage.
6. Per bank.

*Figure 3-2. BLVDS Multi-point Output Example*

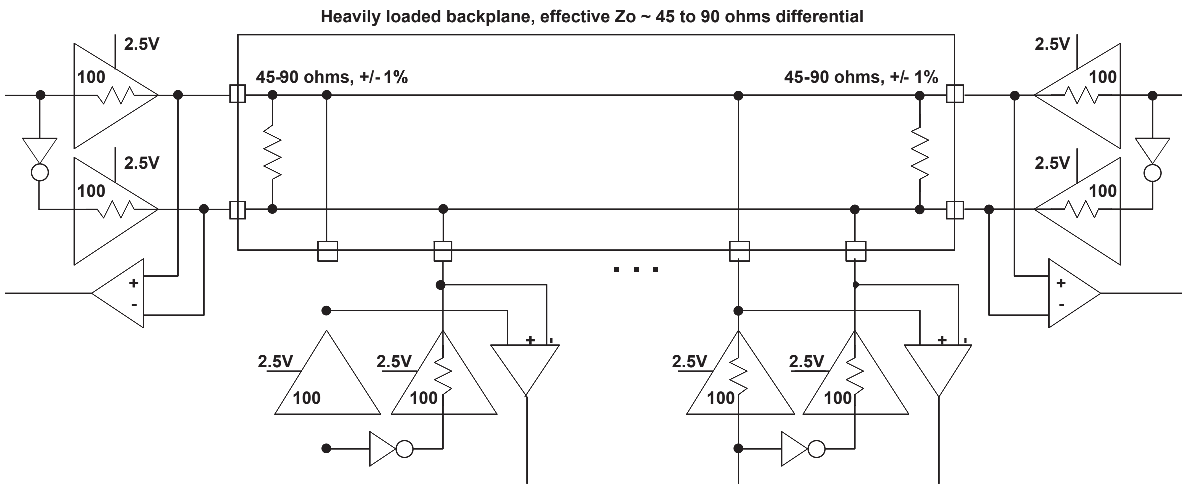



*Table 3-2. BLVDS DC Conditions[1]*

**Over Recommended Operating Conditions**

| Symbol | Description | Typical | | Units |
|---|---|---|---|---|
| | | Zo = 45 | Zo = 90 | |
| $Z_{OUT}$ | Output impedance | 100 | 100 | ohms |
| $R_{TLEFT}$ | Left end termination | 45 | 90 | ohms |
| $R_{TRIGHT}$ | Right end termination | 45 | 90 | ohms |
| $V_{OH}$ | Output high voltage | 1.375 | 1.48 | V |
| $V_{OL}$ | Output low voltage | 1.125 | 1.02 | V |
| $V_{OD}$ | Output differential voltage | 0.25 | 0.46 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | 1.25 | V |
| $I_{DC}$ | DC output current | 11.2 | 10.2 | mA |

1. For input buffer, see LVDS table.

## LatticeXP Family Timing Adders[1] (Continued)

**Over Recommended Operating Conditions**

| Buffer Type | Description | -5 | -4 | -3 | Units |
|---|---|---|---|---|---|
| HSTL15_I | HSTL_15 class I | 0.2 | 0.2 | 0.2 | ns |
| HSTL15_III | HSTL_15 class III | 0.2 | 0.2 | 0.2 | ns |
| HSTL15D_I | Differential HSTL 15 class I | 0.2 | 0.2 | 0.2 | ns |
| HSTL15D_III | Differential HSTL 15 class III | 0.2 | 0.2 | 0.2 | ns |
| SSTL33_I | SSTL_3 class I | 0.1 | 0.1 | 0.1 | ns |
| SSTL33_II | SSTL_3 class II | 0.3 | 0.3 | 0.3 | ns |
| SSTL33D_I | Differential SSTL_3 class I | 0.1 | 0.1 | 0.1 | ns |
| SSTL33D_II | Differential SSTL_3 class II | 0.3 | 0.3 | 0.3 | ns |
| SSTL25_I | SSTL_2 class I | -0.1 | -0.1 | -0.1 | ns |
| SSTL25_II | SSTL_2 class II | 0.3 | 0.3 | 0.3 | ns |
| SSTL25D_I | Differential SSTL_2 class I | -0.1 | -0.1 | -0.1 | ns |
| SSTL25D_II | Differential SSTL_2 class II | 0.3 | 0.3 | 0.3 | ns |
| SSTL18_I | SSTL_1.8 class I | 0.1 | 0.1 | 0.1 | ns |
| SSTL18D_I | Differential SSTL_1.8 class I | 0.1 | 0.1 | 0.1 | ns |
| LVTTL33_4mA | LVTTL 4mA drive | 0.8 | 0.8 | 0.8 | ns |
| LVTTL33_8mA | LVTTL 8mA drive | 0.5 | 0.5 | 0.5 | ns |
| LVTTL33_12mA | LVTTL 12mA drive | 0.3 | 0.3 | 0.3 | ns |
| LVTTL33_16mA | LVTTL 16mA drive | 0.4 | 0.4 | 0.4 | ns |
| LVTTL33_20mA | LVTTL 20mA drive | 0.3 | 0.3 | 0.3 | ns |
| LVCMOS33_2mA | LVCMOS 3.3 2mA drive | 0.8 | 0.8 | 0.8 | ns |
| LVCMOS33_4mA | LVCMOS 3.3 4mA drive | 0.8 | 0.8 | 0.8 | ns |
| LVCMOS33_8mA | LVCMOS 3.3 8mA drive | 0.5 | 0.5 | 0.5 | ns |
| LVCMOS33_12mA | LVCMOS 3.3 12mA drive | 0.3 | 0.3 | 0.3 | ns |
| LVCMOS33_16mA | LVCMOS 3.3 16mA drive | 0.4 | 0.4 | 0.4 | ns |
| LVCMOS33_20mA | LVCMOS 3.3 20mA drive | 0.3 | 0.3 | 0.3 | ns |
| LVCMOS25_2mA | LVCMOS 2.5 2mA drive | 0.7 | 0.7 | 0.7 | ns |
| LVCMOS25_4mA | LVCMOS 2.5 4mA drive | 0.7 | 0.7 | 0.7 | ns |
| LVCMOS25_8mA | LVCMOS 2.5 8mA drive | 0.4 | 0.4 | 0.4 | ns |
| LVCMOS25_12mA | LVCMOS 2.5 12mA drive | 0.0 | 0.0 | 0.0 | ns |
| LVCMOS25_16mA | LVCMOS 2.5 16mA drive | 0.2 | 0.2 | 0.2 | ns |
| LVCMOS25_20mA | LVCMOS 2.5 20mA drive | 0.4 | 0.4 | 0.4 | ns |
| LVCMOS18_2mA | LVCMOS 1.8 2mA drive | 0.6 | 0.6 | 0.6 | ns |
| LVCMOS18_4mA | LVCMOS 1.8 4mA drive | 0.6 | 0.6 | 0.6 | ns |
| LVCMOS18_8mA | LVCMOS 1.8 8mA drive | 0.4 | 0.4 | 0.4 | ns |
| LVCMOS18_12mA | LVCMOS 1.8 12mA drive | 0.2 | 0.2 | 0.2 | ns |
| LVCMOS18_16mA | LVCMOS 1.8 16mA drive | 0.2 | 0.2 | 0.2 | ns |
| LVCMOS15_2mA | LVCMOS 1.5 2mA drive | 0.6 | 0.6 | 0.6 | ns |
| LVCMOS15_4mA | LVCMOS 1.5 4mA drive | 0.6 | 0.6 | 0.6 | ns |
| LVCMOS15_8mA | LVCMOS 1.5 8mA drive | 0.2 | 0.2 | 0.2 | ns |
| LVCMOS12_2mA | LVCMOS 1.2 2mA drive | 0.4 | 0.4 | 0.4 | ns |
| LVCMOS12_6mA | LVCMOS 1.2 6mA drive | 0.4 | 0.4 | 0.4 | ns |
| PCI33 | PCI33 | 0.3 | 0.3 | 0.3 | ns |

1. General timing numbers based on LVCMOS 2.5, 12mA.

Timing v.F0.11

# LatticeXP sysCONFIG Port Timing Specifications

**Over Recommended Operating Conditions**

| Parameter | Description | Min. | Max. | Units |
|---|---|---|---|---|
| **sysCONFIG Byte Data Flow** | | | | |
| $t_{SUCBDI}$ | Byte D[0:7] Setup Time to CCLK | 7 | — | ns |
| $t_{HCBDI}$ | Byte D[0:7] Hold Time to CCLK | 3 | — | ns |
| $t_{CODO}$ | Clock to Dout in Flowthrough Mode | — | 12 | ns |
| $t_{SUCS}$ | CS[0:1] Setup Time to CCLK | 7 | — | ns |
| $t_{HCS}$ | CS[0:1] Hold Time to CCLK | 2 | — | ns |
| $t_{SUWD}$ | Write Signal Setup Time to CCLK | 7 | — | ns |
| $t_{HWD}$ | Write Signal Hold Time to CCLK | 2 | — | ns |
| $t_{DCB}$ | CCLK to BUSY Delay Time | — | 12 | ns |
| $t_{CORD}$ | Clock to Out for Read Data | — | 12 | ns |
| **sysCONFIG Byte Slave Clocking** | | | | |
| $t_{BSCH}$ | Byte Slave Clock Minimum High Pulse | 6 | — | ns |
| $t_{BSCL}$ | Byte Slave Clock Minimum Low Pulse | 8 | — | ns |
| $t_{BSCYC}$ | Byte Slave Clock Cycle Time | 15 | — | ns |
| **sysCONFIG Serial (Bit) Data Flow** | | | | |
| $t_{SUSCDI}$ | DI (Data In) Setup Time to CCLK | 7 | — | ns |
| $t_{HSCDI}$ | DI (Data In) Hold Time to CCLK | 2 | — | ns |
| $t_{CODO}$ | Clock to Dout in Flowthrough Mode | — | 12 | ns |
| **sysCONFIG Serial Slave Clocking** | | | | |
| $t_{SSCH}$ | Serial Slave Clock Minimum High Pulse | 6 | — | ns |
| $t_{SSCL}$ | Serial Slave Clock Minimum Low Pulse | 6 | — | ns |
| **sysCONFIG POR, Initialization and Wake Up** | | | | |
| $t_{ICFG}$ | Minimum Vcc to INIT High | — | 50 | ms |
| $t_{VMC}$ | Time from $t_{ICFG}$ to Valid Master Clock | — | 2 | us |
| $t_{PRGMRJ}$ | Program Pin Pulse Rejection | — | 7 | ns |
| $t_{PRGM}$[2] | PROGRAMN Low Time to Start Configuration | 25 | — | ns |
| $t_{DINIT}$ | INIT Low Time | — | 1 | ms |
| $t_{DPPINIT}$ | Delay Time from PROGRAMN Low to INIT Low | — | 37 | ns |
| $t_{DINITD}$ | Delay Time from PROGRAMN Low to DONE Low | — | 37 | ns |
| $t_{IODISS}$ | User I/O Disable from PROGRAMN Low | — | 25 | ns |
| $t_{IOENSS}$ | User I/O Enabled Time from CCLK Edge During Wake-up Sequence | — | 25 | ns |
| $t_{MWC}$ | Additional Wake Master Clock Signals after Done Pin High | 120 | — | cycles |
| **Configuration Master Clock (CCLK)** | | | | |
| Frequency[1] | | Selected Value - 30% | Selected Value + 30% | MHz |
| Duty Cycle | | 40 | 60 | % |

1. See Table 2-10 for available CCLK frequencies.
2. The threshold level for PROGRAMN, as well as for CFG[1] and CFG[0], is determined by $V_{CC}$, such that the threshold = $V_{CC}/2$.

Timing v.F0.11

# LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP (Cont.)

| Pin Number | LFXP3 | | | | LFXP6 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | Differential | Dual Function | Pin Function | Bank | Differential | Dual Function |
| 139 | PT6A | 0 | - | DI | PT9A | 0 | - | DI |
| 140 | PT5A | 0 | - | CSN | PT8A | 0 | - | CSN |
| 141 | PT3B | 0 | - | VREF2_0 | PT6B | 0 | - | VREF2_0 |
| 142 | CFG0 | 0 | - | - | CFG0 | 0 | - | - |
| 143 | CFG1 | 0 | - | - | CFG1 | 0 | - | - |
| 144 | DONE | 0 | - | - | DONE | 0 | - | - |

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

## LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFXP6 | | | | LFXP10 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| E8 | PT13B | 0 | - | - | PT17B | 0 | - | - |
| D8 | PT12A | 0 | - | DOUT | PT16A | 0 | - | DOUT |
| A6 | PT11B | 0 | C | - | PT15B | 0 | C | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C6 | PT11A | 0 | T | WRITEN | PT15A | 0 | T | WRITEN |
| E7 | PT10B | 0 | C | - | PT14B | 0 | C | - |
| D7 | PT10A | 0 | T | VREF1_0 | PT14A | 0 | T | VREF1_0 |
| A5 | PT9B | 0 | C | - | PT13B | 0 | C | - |
| B5 | PT9A | 0 | T | DI | PT13A | 0 | T | DI |
| A4 | PT8B | 0 | C | - | PT12B | 0 | C | - |
| B6 | PT8A | 0 | T | CSN | PT12A | 0 | T | CSN |
| E6 | PT7B | 0 | C | - | PT11B | 0 | C | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| D6 | PT7A | 0 | T | - | PT11A | 0 | T | - |
| D5 | PT6B | 0 | C | VREF2_0 | PT10B | 0 | C | VREF2_0 |
| A3 | PT6A | 0 | T | DQS | PT10A | 0 | T | DQS |
| B3 | PT5B | 0 | - | - | PT9B | 0 | - | - |
| B2 | PT4A | 0 | - | - | PT8A | 0 | - | - |
| A2 | PT3B | 0 | C | - | PT7B | 0 | C | - |
| B1 | PT3A | 0 | T | - | PT7A | 0 | T | - |
| F5 | PT2B | 0 | C | - | PT6B | 0 | C | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C5 | PT2A | 0 | T | - | PT6A | 0 | T | - |
| C4 | CFG0 | 0 | - | - | CFG0 | 0 | - | - |
| B4 | CFG1 | 0 | - | - | CFG1 | 0 | - | - |
| C3 | DONE | 0 | - | - | DONE | 0 | - | - |
| A1 | GND | - | - | - | GND | - | - | - |
| A16 | GND | - | - | - | GND | - | - | - |
| F11 | GND | - | - | - | GND | - | - | - |
| F6 | GND | - | - | - | GND | - | - | - |
| G10 | GND | - | - | - | GND | - | - | - |
| G7 | GND | - | - | - | GND | - | - | - |
| G8 | GND | - | - | - | GND | - | - | - |
| G9 | GND | - | - | - | GND | - | - | - |
| H10 | GND | - | - | - | GND | - | - | - |
| H7 | GND | - | - | - | GND | - | - | - |
| H8 | GND | - | - | - | GND | - | - | - |
| H9 | GND | - | - | - | GND | - | - | - |
| J10 | GND | - | - | - | GND | - | - | - |
| J7 | GND | - | - | - | GND | - | - | - |
| J8 | GND | - | - | - | GND | - | - | - |
| J9 | GND | - | - | - | GND | - | - | - |

## LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

| | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| L7 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| L8 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| J6 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| K6 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| G6 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| H6 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

# LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

| | LFXP10 | | | | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function |
| AA20 | PB36B | 4 | C | - | PB41B | 4 | C | - | PB45B | 4 | C | - |
| AB21 | PB37A | 4 | T | - | PB42A | 4 | T | - | PB46A | 4 | T | - |
| AA21 | PB37B | 4 | C | - | PB42B | 4 | C | - | PB46B | 4 | C | - |
| AA22 | PB38A | 4 | T | - | PB43A | 4 | T | - | PB47A | 4 | T | - |
| Y21 | PB38B | 4 | C | - | PB43B | 4 | C | - | PB47B | 4 | C | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| W16 | PB39A | 4 | - | - | PB44A | 4 | T | - | PB48A | 4 | T | - |
| W17 | - | - | - | - | PB44B | 4 | C | - | PB48B | 4 | C | - |
| Y15 | - | - | - | - | PB45A | 4 | - | - | PB49A | 4 | - | - |
| Y16 | - | - | - | - | PB46B | 4 | - | - | PB50B | 4 | - | - |
| W19 | - | - | - | - | PB47A | 4 | T | DQS | PB51A | 4 | T | DQS |
| W18 | - | - | - | - | PB47B | 4 | C | - | PB51B | 4 | C | - |
| W20 | - | - | - | - | PB48A | 4 | - | - | PB52A | 4 | - | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| T20 | PR35B | 3 | C[3] | - | PR39B | 3 | C[3] | - | PR43B | 3 | C[3] | - |
| T19 | PR35A | 3 | T[3] | - | PR39A | 3 | T[3] | - | PR43A | 3 | T[3] | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| U19 | PR34B | 3 | C | RLM0_PLLC_FB_A | PR38B | 3 | C | RLM0_PLLC_FB_A | PR42B | 3 | C | RLM0_PLLC_FB_A |
| U20 | PR34A | 3 | T | RLM0_PLLT_FB_A | PR38A | 3 | T | RLM0_PLLT_FB_A | PR42A | 3 | T | RLM0_PLLT_FB_A |
| V19 | PR33B | 3 | C[3] | - | PR37B | 3 | C[3] | - | PR41B | 3 | C[3] | - |
| V20 | PR33A | 3 | T[3] | DQS | PR37A | 3 | T[3] | DQS | PR41A | 3 | T[3] | DQS |
| R19 | PR32B | 3 | - | - | PR36B | 3 | - | - | PR40B | 3 | - | - |
| R20 | PR31A | 3 | - | VREF1_3 | PR35A | 3 | - | VREF1_3 | PR39A | 3 | - | VREF1_3 |
| W21 | PR30B | 3 | C[3] | - | PR34B | 3 | C[3] | - | PR38B | 3 | C[3] | - |
| Y22 | PR30A | 3 | T[3] | - | PR34A | 3 | T[3] | - | PR38A | 3 | T[3] | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| P19 | PR29B | 3 | C | - | PR33B | 3 | C | - | PR37B | 3 | C | - |
| P20 | PR29A | 3 | T | - | PR33A | 3 | T | - | PR37A | 3 | T | - |
| V21 | PR28B | 3 | C[3] | - | PR32B | 3 | C[3] | - | PR36B | 3 | C[3] | - |
| W22 | PR28A | 3 | T[3] | - | PR32A | 3 | T[3] | - | PR36A | 3 | T[3] | - |
| U21 | PR26B | 3 | C[3] | - | PR30B | 3 | C[3] | - | PR34B | 3 | C[3] | - |
| V22 | PR26A | 3 | T[3] | - | PR30A | 3 | T[3] | - | PR34A | 3 | T[3] | - |
| T21 | PR25B | 3 | C | RLM0_PLLC_IN_A | PR29B | 3 | C | RLM0_PLLC_IN_A | PR33B | 3 | C | RLM0_PLLC_IN_A |
| U22 | PR25A | 3 | T | RLM0_PLLT_IN_A | PR29A | 3 | T | RLM0_PLLT_IN_A | PR33A | 3 | T | RLM0_PLLT_IN_A |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| R21 | PR24B | 3 | C[3] | - | PR28B | 3 | C[3] | - | PR32B | 3 | C[3] | - |
| T22 | PR24A | 3 | T[3] | DQS | PR28A | 3 | T[3] | DQS | PR32A | 3 | T[3] | DQS |
| N19 | PR23B | 3 | - | - | PR27B | 3 | - | - | PR31B | 3 | - | - |
| N20 | PR22A | 3 | - | VREF2_3 | PR26A | 3 | - | VREF2_3 | PR30A | 3 | - | VREF2_3 |
| R22 | PR21B | 3 | C[3] | - | PR25B | 3 | C[3] | - | PR29B | 3 | C[3] | - |
| P22 | PR21A | 3 | T[3] | - | PR25A | 3 | T[3] | - | PR29A | 3 | T[3] | - |
| P21 | PR20B | 3 | C | - | PR24B | 3 | C | - | PR28B | 3 | C | - |
| N21 | PR20A | 3 | T | - | PR24A | 3 | T | - | PR28A | 3 | T | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| M20 | PR19B | 3 | C[3] | - | PR23B | 3 | C[3] | - | PR27B | 3 | C[3] | - |
| M19 | PR19A | 3 | T[3] | - | PR23A | 3 | T[3] | - | PR27A | 3 | T[3] | - |
| N22 | GNDP1 | - | - | - | GNDP1 | - | - | - | GNDP1 | - | - | - |

## LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| AB5 | PB16A | 5 | T | - | PB20A | 5 | T | - |
| AB6 | PB16B | 5 | C | - | PB20B | 5 | C | - |
| AA8 | PB17A | 5 | T | - | PB21A | 5 | T | - |
| AA9 | PB17B | 5 | C | VREF2_5 | PB21B | 5 | C | VREF2_5 |
| W10 | PB18A | 5 | T | - | PB22A | 5 | T | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| V10 | PB18B | 5 | C | - | PB22B | 5 | C | - |
| AB7 | PB19A | 5 | T | - | PB23A | 5 | T | - |
| AB8 | PB19B | 5 | C | - | PB23B | 5 | C | - |
| AB9 | PB20A | 5 | T | - | PB24A | 5 | T | - |
| AB10 | PB20B | 5 | C | - | PB24B | 5 | C | - |
| Y10 | PB21A | 5 | - | - | PB25A | 5 | - | - |
| AA10 | PB22B | 5 | - | - | PB26B | 5 | - | - |
| W11 | PB23A | 5 | T | DQS | PB27A | 5 | T | DQS |
| V11 | PB23B | 5 | C | - | PB27B | 5 | C | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| Y11 | PB24A | 5 | T | - | PB28A | 5 | T | - |
| AA11 | PB24B | 5 | C | - | PB28B | 5 | C | - |
| AB11 | PB25A | 5 | T | - | PB29A | 5 | T | - |
| AB12 | PB25B | 5 | C | - | PB29B | 5 | C | - |
| Y12 | PB26A | 4 | T | - | PB30A | 4 | T | - |
| AA12 | PB26B | 4 | C | - | PB30B | 4 | C | - |
| W12 | PB27A | 4 | T | PCLKT4_0 | PB31A | 4 | T | PCLKT4_0 |
| V12 | PB27B | 4 | C | PCLKC4_0 | PB31B | 4 | C | PCLKC4_0 |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| AB13 | PB28A | 4 | T | - | PB32A | 4 | T | - |
| AB14 | PB28B | 4 | C | - | PB32B | 4 | C | - |
| AA13 | PB29A | 4 | - | - | PB33A | 4 | - | - |
| Y13 | PB30B | 4 | - | - | PB34B | 4 | - | - |
| AB15 | PB31A | 4 | T | DQS | PB35A | 4 | T | DQS |
| AB16 | PB31B | 4 | C | VREF1_4 | PB35B | 4 | C | VREF1_4 |
| V13 | PB32A | 4 | T | - | PB36A | 4 | T | - |
| W13 | PB32B | 4 | C | - | PB36B | 4 | C | - |
| AA14 | PB33A | 4 | T | - | PB37A | 4 | T | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| AA15 | PB33B | 4 | C | - | PB37B | 4 | C | - |
| AB17 | PB34A | 4 | T | - | PB38A | 4 | T | - |
| AB18 | PB34B | 4 | C | - | PB38B | 4 | C | - |
| W14 | PB35A | 4 | T | - | PB39A | 4 | T | - |
| Y14 | PB35B | 4 | C | - | PB39B | 4 | C | - |
| U14 | PB36A | 4 | T | VREF2_4 | PB40A | 4 | T | VREF2_4 |
| V14 | PB36B | 4 | C | - | PB40B | 4 | C | - |

## LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| R18 | PR38B | 3 | C | RLM0_PLLC_FB_A | PR42B | 3 | C | RLM0_PLLC_FB_A |
| R17 | PR38A | 3 | T | RLM0_PLLT_FB_A | PR42A | 3 | T | RLM0_PLLT_FB_A |
| Y22 | PR37B | 3 | C[3] | - | PR41B | 3 | C[3] | - |
| Y21 | PR37A | 3 | T[3] | DQS | PR41A | 3 | T[3] | DQS |
| W22 | PR36B | 3 | - | - | PR40B | 3 | - | - |
| W21 | PR35A | 3 | - | VREF1_3 | PR39A | 3 | - | VREF1_3 |
| P17 | PR34B | 3 | C[3] | - | PR38B | 3 | C[3] | - |
| P18 | PR34A | 3 | T[3] | - | PR38A | 3 | T[3] | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| R19 | PR33B | 3 | C | - | PR37B | 3 | C | - |
| R20 | PR33A | 3 | T | - | PR37A | 3 | T | - |
| V22 | PR32B | 3 | C[3] | - | PR36B | 3 | C[3] | - |
| V21 | PR32A | 3 | T[3] | - | PR36A | 3 | T[3] | - |
| U22 | PR30B | 3 | C[3] | - | PR34B | 3 | C[3] | - |
| U21 | PR30A | 3 | T[3] | - | PR34A | 3 | T[3] | - |
| P19 | PR29B | 3 | C | RLM0_PLLC_IN_A | PR33B | 3 | C | RLM0_PLLC_IN_A |
| P20 | PR29A | 3 | T | RLM0_PLLT_IN_A | PR33A | 3 | T | RLM0_PLLT_IN_A |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| T22 | PR28B | 3 | C[3] | - | PR32B | 3 | C[3] | - |
| T21 | PR28A | 3 | T[3] | DQS | PR32A | 3 | T[3] | DQS |
| R22 | PR27B | 3 | - | - | PR31B | 3 | - | - |
| R21 | PR26A | 3 | - | VREF2_3 | PR30A | 3 | - | VREF2_3 |
| N19 | PR25B | 3 | C[3] | - | PR29B | 3 | C[3] | - |
| N20 | PR25A | 3 | T[3] | - | PR29A | 3 | T[3] | - |
| N18 | PR24B | 3 | C | - | PR28B | 3 | C | - |
| M18 | PR24A | 3 | T | - | PR28A | 3 | T | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| P22 | PR23B | 3 | C[3] | - | PR27B | 3 | C[3] | - |
| P21 | PR23A | 3 | T[3] | - | PR27A | 3 | T[3] | - |
| N22 | - | - | - | - | PR26B | 3 | C[3] | - |
| N21 | - | - | - | - | PR26A | 3 | T[3] | - |
| M19 | - | - | - | - | PR25B | 3 | - | - |
| M20 | GNDP1 | - | - | - | GNDP1 | - | - | - |
| L18 | VCCP1 | - | - | - | VCCP1 | - | - | - |
| M21 | - | - | - | - | PR24A | 2 | - | - |
| M22 | PR22B | 2 | C[3] | - | PR23B | 2 | C[3] | - |
| L22 | PR22A | 2 | T[3] | - | PR23A | 2 | T[3] | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| L19 | - | - | - | - | PR22B | 2 | C[3] | - |
| L20 | - | - | - | - | PR22A | 2 | T[3] | - |
| L21 | PR21B | 2 | C | PCLKC2_0 | PR21B | 2 | C | PCLKC2_0 |
| K22 | PR21A | 2 | T | PCLKT2_0 | PR21A | 2 | T | PCLKT2_0 |

## LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| J15 | GND | - | - | - | GND | - | - | - |
| J8 | GND | - | - | - | GND | - | - | - |
| J9 | GND | - | - | - | GND | - | - | - |
| K10 | GND | - | - | - | GND | - | - | - |
| K11 | GND | - | - | - | GND | - | - | - |
| K12 | GND | - | - | - | GND | - | - | - |
| K13 | GND | - | - | - | GND | - | - | - |
| K14 | GND | - | - | - | GND | - | - | - |
| K9 | GND | - | - | - | GND | - | - | - |
| L10 | GND | - | - | - | GND | - | - | - |
| L11 | GND | - | - | - | GND | - | - | - |
| L12 | GND | - | - | - | GND | - | - | - |
| L13 | GND | - | - | - | GND | - | - | - |
| L14 | GND | - | - | - | GND | - | - | - |
| L9 | GND | - | - | - | GND | - | - | - |
| M10 | GND | - | - | - | GND | - | - | - |
| M11 | GND | - | - | - | GND | - | - | - |
| M12 | GND | - | - | - | GND | - | - | - |
| M13 | GND | - | - | - | GND | - | - | - |
| M14 | GND | - | - | - | GND | - | - | - |
| M9 | GND | - | - | - | GND | - | - | - |
| N10 | GND | - | - | - | GND | - | - | - |
| N11 | GND | - | - | - | GND | - | - | - |
| N12 | GND | - | - | - | GND | - | - | - |
| N13 | GND | - | - | - | GND | - | - | - |
| N14 | GND | - | - | - | GND | - | - | - |
| N9 | GND | - | - | - | GND | - | - | - |
| P10 | GND | - | - | - | GND | - | - | - |
| P11 | GND | - | - | - | GND | - | - | - |
| P12 | GND | - | - | - | GND | - | - | - |
| P13 | GND | - | - | - | GND | - | - | - |
| P14 | GND | - | - | - | GND | - | - | - |
| P15 | GND | - | - | - | GND | - | - | - |
| P8 | GND | - | - | - | GND | - | - | - |
| P9 | GND | - | - | - | GND | - | - | - |
| R14 | GND | - | - | - | GND | - | - | - |
| R9 | GND | - | - | - | GND | - | - | - |
| F10 | VCC | - | - | - | VCC | - | - | - |
| F13 | VCC | - | - | - | VCC | - | - | - |
| G10 | VCC | - | - | - | VCC | - | - | - |
| G13 | VCC | - | - | - | VCC | - | - | - |
| G14 | VCC | - | - | - | VCC | - | - | - |

**Industrial (Cont.)**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP15E-3F484I | 300 | 1.2V | -3 | fpBGA | 484 | IND | 15.5K |
| LFXP15E-4F484I | 300 | 1.2V | -4 | fpBGA | 484 | IND | 15.5K |
| LFXP15E-3F388I | 268 | 1.2V | -3 | fpBGA | 388 | IND | 15.5K |
| LFXP15E-4F388I | 268 | 1.2V | -4 | fpBGA | 388 | IND | 15.5K |
| LFXP15E-3F256I | 188 | 1.2V | -3 | fpBGA | 256 | IND | 15.5K |
| LFXP15E-4F256I | 188 | 1.2V | -4 | fpBGA | 256 | IND | 15.5K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP20E-3F484I | 340 | 1.2V | -3 | fpBGA | 484 | IND | 19.7K |
| LFXP20E-4F484I | 340 | 1.2V | -4 | fpBGA | 484 | IND | 19.7K |
| LFXP20E-3F388I | 268 | 1.2V | -3 | fpBGA | 388 | IND | 19.7K |
| LFXP20E-4F388I | 268 | 1.2V | -4 | fpBGA | 388 | IND | 19.7K |
| LFXP20E-3F256I | 188 | 1.2V | -3 | fpBGA | 256 | IND | 19.7K |
| LFXP20E-4F256I | 188 | 1.2V | -4 | fpBGA | 256 | IND | 19.7K |

## Lead-free Packaging

**Commercial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP3C-3QN208C | 136 | 1.8/2.5/3.3V | -3 | PQFP | 208 | COM | 3.1K |
| LFXP3C-4QN208C | 136 | 1.8/2.5/3.3V | -4 | PQFP | 208 | COM | 3.1K |
| LFXP3C-5QN208C | 136 | 1.8/2.5/3.3V | -5 | PQFP | 208 | COM | 3.1K |
| LFXP3C-3TN144C | 100 | 1.8/2.5/3.3V | -3 | TQFP | 144 | COM | 3.1K |
| LFXP3C-4TN144C | 100 | 1.8/2.5/3.3V | -4 | TQFP | 144 | COM | 3.1K |
| LFXP3C-5TN144C | 100 | 1.8/2.5/3.3V | -5 | TQFP | 144 | COM | 3.1K |
| LFXP3C-3TN100C | 62 | 1.8/2.5/3.3V | -3 | TQFP | 100 | COM | 3.1K |
| LFXP3C-4TN100C | 62 | 1.8/2.5/3.3V | -4 | TQFP | 100 | COM | 3.1K |
| LFXP3C-5TN100C | 62 | 1.8/2.5/3.3V | -5 | TQFP | 100 | COM | 3.1K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP6C-3FN256C | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | COM | 5.8K |
| LFXP6C-4FN256C | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | COM | 5.8K |
| LFXP6C-5FN256C | 188 | 1.8/2.5/3.3V | -5 | fpBGA | 256 | COM | 5.8K |
| LFXP6C-3QN208C | 142 | 1.8/2.5/3.3V | -3 | PQFP | 208 | COM | 5.8K |
| LFXP6C-4QN208C | 142 | 1.8/2.5/3.3V | -4 | PQFP | 208 | COM | 5.8K |
| LFXP6C-5QN208C | 142 | 1.8/2.5/3.3V | -5 | PQFP | 208 | COM | 5.8K |
| LFXP6C-3TN144C | 100 | 1.8/2.5/3.3V | -3 | TQFP | 144 | COM | 5.8K |
| LFXP6C-4TN144C | 100 | 1.8/2.5/3.3V | -4 | TQFP | 144 | COM | 5.8K |
| LFXP6C-5TN144C | 100 | 1.8/2.5/3.3V | -5 | TQFP | 144 | COM | 5.8K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP10C-3FN388C | 244 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | COM | 9.7K |
| LFXP10C-4FN388C | 244 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | COM | 9.7K |
| LFXP10C-5FN388C | 244 | 1.8/2.5/3.3V | -5 | fpBGA | 388 | COM | 9.7K |
| LFXP10C-3FN256C | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | COM | 9.7K |
| LFXP10C-4FN256C | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | COM | 9.7K |
| LFXP10C-5FN256C | 188 | 1.8/2.5/3.3V | -5 | fpBGA | 256 | COM | 9.7K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP15C-3FN484C | 300 | 1.8/2.5/3.3V | -3 | fpBGA | 484 | COM | 15.5K |
| LFXP15C-4FN484C | 300 | 1.8/2.5/3.3V | -4 | fpBGA | 484 | COM | 15.5K |
| LFXP15C-5FN484C | 300 | 1.8/2.5/3.3V | -5 | fpBGA | 484 | COM | 15.5K |
| LFXP15C-3FN388C | 268 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | COM | 15.5K |
| LFXP15C-4FN388C | 268 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | COM | 15.5K |
| LFXP15C-5FN388C | 268 | 1.8/2.5/3.3V | -5 | fpBGA | 388 | COM | 15.5K |
| LFXP15C-3FN256C | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | COM | 15.5K |
| LFXP15C-4FN256C | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | COM | 15.5K |
| LFXP15C-5FN256C | 188 | 1.8/2.5/3.3V | -5 | fpBGA | 256 | COM | 15.5K |