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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10000
Total RAM Bits	221184
Number of I/O	188
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp10e-4fn256c

Lattice Semiconductor Corporation

LatticeXP Family Data Sheet
Architecture

July 2007 Data Sheet DS1001

Architecture Overview

The LatticeXP architecture contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM Embedded Block RAM (EBR) as shown in Figure 2-1.

On the left and right sides of the PFU array, there are Non-volatile Memory Blocks. In configuration mode this non-volatile memory is programmed via the IEEE 1149.1 TAP port or the sysCONFIG™ peripheral port. On power up, the configuration data is transferred from the Non-volatile Memory Blocks to the configuration SRAM. With this technology, expensive external configuration memories are not required and designs are secured from unauthorized read-back. This transfer of data from non-volatile memory to configuration SRAM via wide busses happens in microseconds, providing an “instant-on” capability that allows easy interfacing in many applications.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional unit without RAM/ROM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM, ROM and register functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row. The PFU blocks are used on the outside rows. The rest of the core consists of rows of PFF blocks interspersed with rows of PFU blocks. For every three rows of PFF blocks there is a row of PFU blocks.

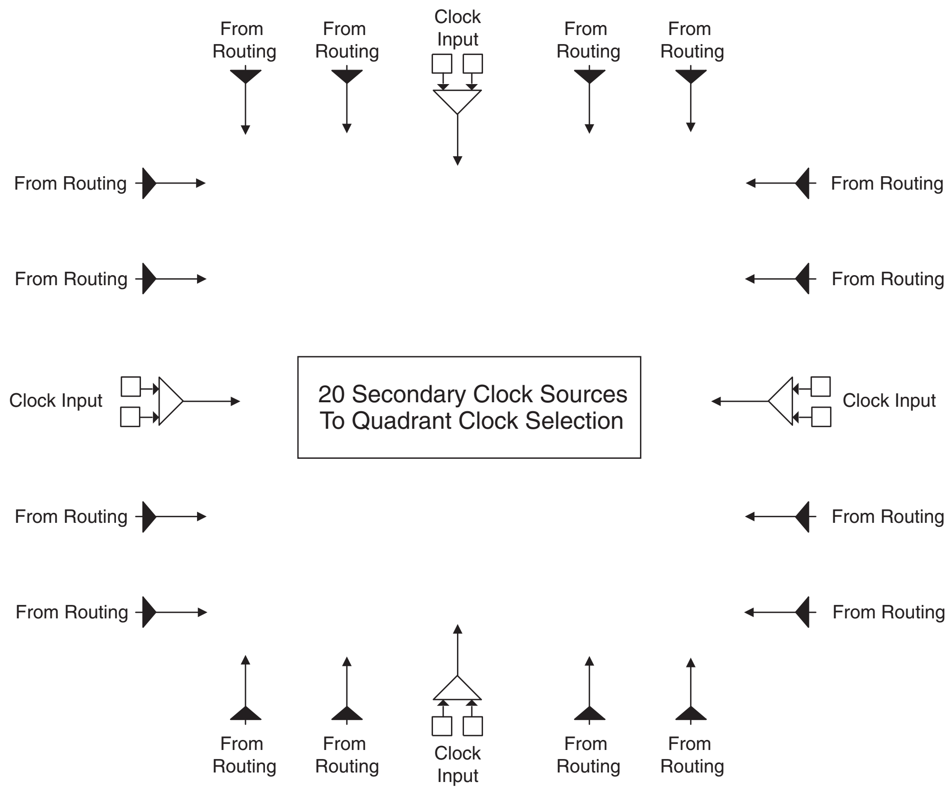
Each PIC block encompasses two PIOs (PIO pairs) with their respective sysIO interfaces. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. sysMEM EBRs are large dedicated fast memory blocks. They can be configured as RAM or ROM.

The PFU, PFF, PIC and EBR Blocks are arranged in a two-dimensional grid with rows and columns as shown in Figure 2-1. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

At the end of the rows containing the sysMEM Blocks are the sysCLOCK Phase Locked Loop (PLL) Blocks. These PLLs have multiply, divide and phase shifting capability; they are used to manage the phase relationship of the clocks. The LatticeXP architecture provides up to four PLLs per device.

Every device in the family has a JTAG Port with internal Logic Analyzer (ispTRACY) capability. The sysCONFIG port which allows for serial or parallel device configuration. The LatticeXP devices are available for operation from 3.3V, 2.5V, 1.8V and 1.2V power supplies, providing easy integration into the overall system.

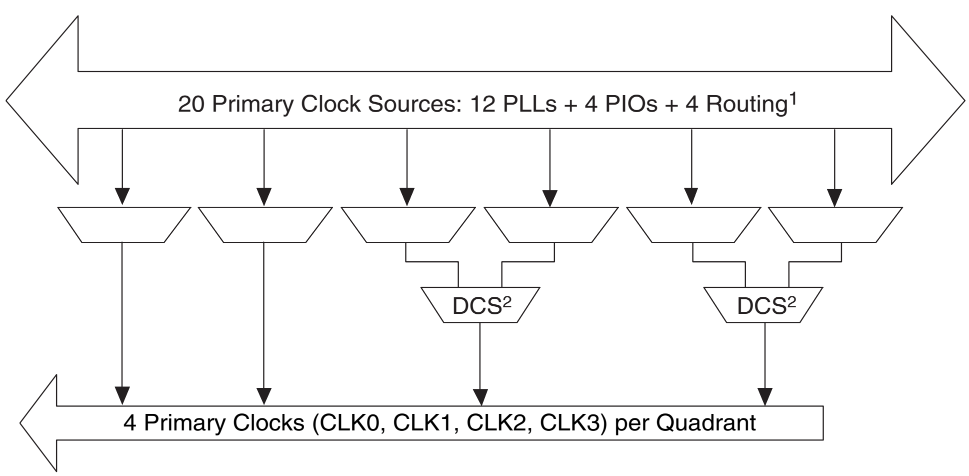
Figure 2-6. Secondary Clock Sources



Clock Routing

The clock routing structure in LatticeXP devices consists of four Primary Clock lines and a Secondary Clock network per quadrant. The primary clocks are generated from MUXs located in each quadrant. Figure 2-7 shows this clock routing. The four secondary clocks are generated from MUXs located in each quadrant as shown in Figure 2-8. Each slice derives its clock from the primary clock lines, secondary clock lines and routing as shown in Figure 2-9.

Figure 2-7. Per Quadrant Primary Clock Selection



1. Smaller devices have fewer PLL related lines.
2. Dynamic clock select.

For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved irrespective of where the select signal is toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-12 illustrates the DCS Block Macro.

Figure 2-12. DCS Block Primitive

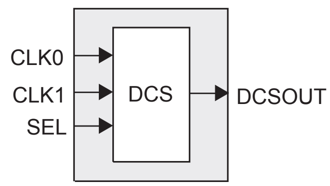
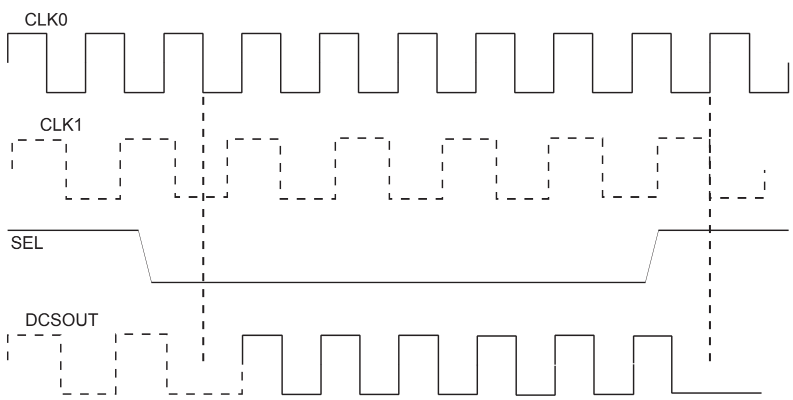


Figure 2-13 shows timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information on the DCS, please see details of additional technical documentation at the end of this data sheet.

Figure 2-13. DCS Waveforms



sysMEM Memory

The LatticeXP family of devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-6.

Hot Socketing Specifications[1, 2, 3, 4, 5, 6]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq V_{IH}$ (MAX.)	—	—	+/-1000	µA

1. Insensitive to sequence of V_{CC}, V_{CCAUX} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC}, V_{CCAUX} and V_{CCIO}.
2. $0 \leq V_{CC} \leq V_{CC}$ (MAX) or $0 \leq V_{CCAUX} \leq V_{CCAUX}$ (MAX).
3. $0 \leq V_{CCIO} \leq V_{CCIO}$ (MAX) for top and bottom I/O banks.
4. $0.2 \leq V_{CCIO} \leq V_{CCIO}$ (MAX) for left and right I/O banks.
5. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.
6. LVCMOS and LVTTL only.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

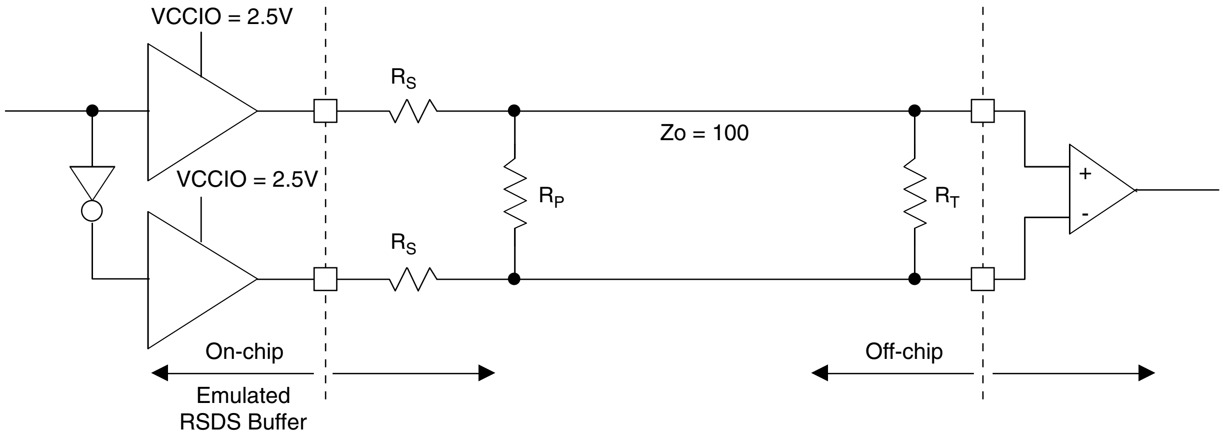
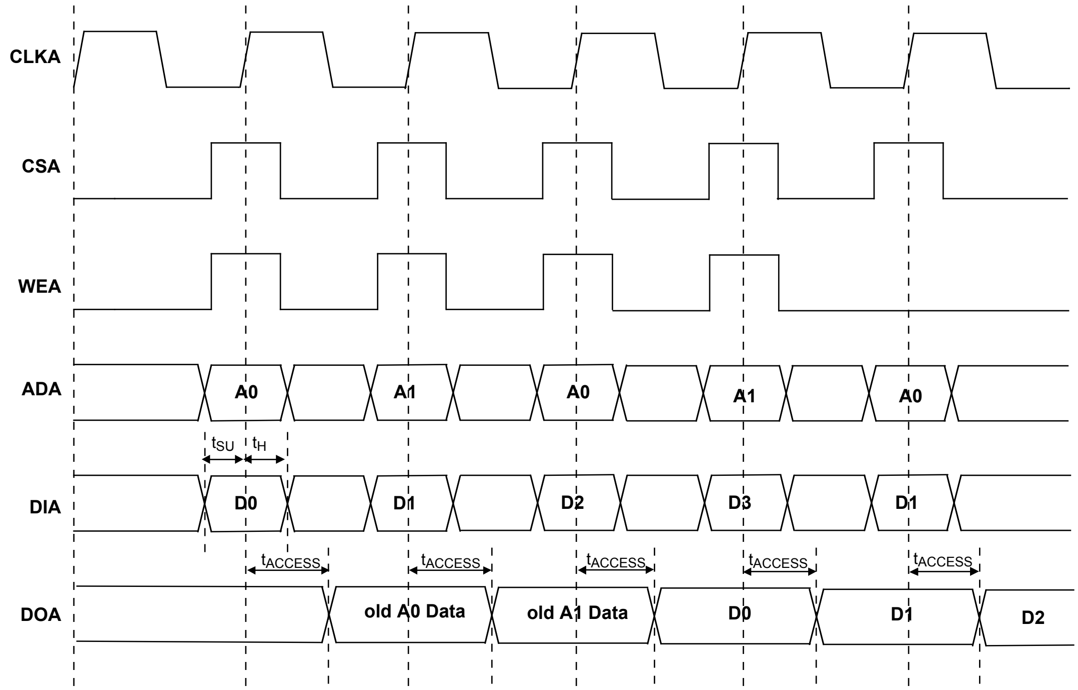


Table 3-4. RSDS DC Conditions

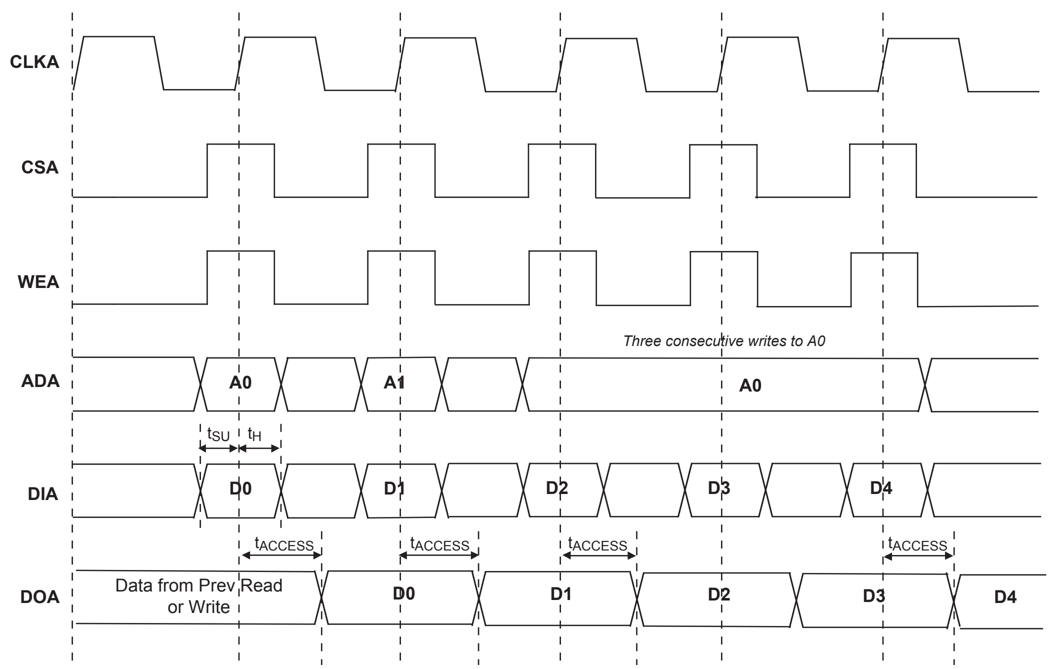
Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	ohms
R_S	Driver series resistor	300	ohms
R_P	Driver parallel resistor	121	ohms
R_T	Receiver termination	100	ohms
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	ohms
I_{DC}	DC output current	3.66	mA

Figure 3-10. Read Before Write (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

Figure 3-11. Write Through (SP Read/Write On Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

LatticeXP sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
sysCONFIG Byte Data Flow				
t_{SUCBDI}	Byte D[0:7] Setup Time to CCLK	7	—	ns
t_{HCBDI}	Byte D[0:7] Hold Time to CCLK	3	—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	—	12	ns
t_{SUCS}	CS[0:1] Setup Time to CCLK	7	—	ns
t_{HCS}	CS[0:1] Hold Time to CCLK	2	—	ns
t_{SUWD}	Write Signal Setup Time to CCLK	7	—	ns
t_{HWD}	Write Signal Hold Time to CCLK	2	—	ns
t_{DCB}	CCLK to BUSY Delay Time	—	12	ns
t_{CORD}	Clock to Out for Read Data	—	12	ns
sysCONFIG Byte Slave Clocking				
t_{BSCH}	Byte Slave Clock Minimum High Pulse	6	—	ns
t_{BSCL}	Byte Slave Clock Minimum Low Pulse	8	—	ns
t_{BSCYC}	Byte Slave Clock Cycle Time	15	—	ns
sysCONFIG Serial (Bit) Data Flow				
t_{SUSCDI}	DI (Data In) Setup Time to CCLK	7	—	ns
t_{HSCDI}	DI (Data In) Hold Time to CCLK	2	—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	—	12	ns
sysCONFIG Serial Slave Clocking				
t_{SSCH}	Serial Slave Clock Minimum High Pulse	6	—	ns
t_{SSCL}	Serial Slave Clock Minimum Low Pulse	6	—	ns
sysCONFIG POR, Initialization and Wake Up				
t_{ICFG}	Minimum Vcc to INIT High	—	50	ms
t_{VMC}	Time from t_{ICFG} to Valid Master Clock	—	2	us
t_{PRGMRJ}	Program Pin Pulse Rejection	—	7	ns
t_{PRGM}[2]	PROGRAMN Low Time to Start Configuration	25	—	ns
t_{DINIT}	INIT Low Time	—	1	ms
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INIT Low	—	37	ns
t_{DINITD}	Delay Time from PROGRAMN Low to DONE Low	—	37	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low	—	25	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence	—	25	ns
t_{MWC}	Additional Wake Master Clock Signals after Done Pin High	120	—	cycles
Configuration Master Clock (CCLK)				
Frequency[1]		Selected Value - 30%	Selected Value + 30%	MHz
Duty Cycle		40	60	%

1. See Table 2-10 for available CCLK frequencies.
2. The threshold level for PROGRAMN, as well as for CFG[1] and CFG[0], is determined by V_{CC}, such that the threshold = $V_{CC}/2$.

Timing v.F0.11

Switching Test Conditions

Figure 3-13 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Figure 3-5.

Figure 3-13. Output Test Load, LVTTL and LVCMOS Standards

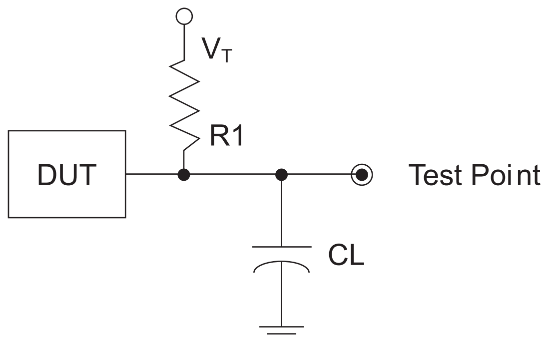


Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	0pF	LVCMOS 3.3 = 1.5V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	188	0pF	$V_{CCIO}/2$	V_{OL}
LVCMOS 2.5 I/O (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVCMOS 2.5 I/O (H -> Z)			V_{OH} - 0.15	V_{OL}
LVCMOS 2.5 I/O (L -> Z)			V_{OL} + 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Pin Information Summary[1]

Pin Type		XP3 100 TQFP	XP3 144 TQFP	XP3 208 PQFP	XP6 144 TQFP	XP6 208 PQFP	XP6 256 fpBGA
Single Ended User I/O		62	100	136	100	142	188
Differential Pair User I/O[2]		19	35	56	35	58	80
Configuration	Dedicated	11	11	11	11	11	11
	Muxed	14	14	14	14	14	14
TAP		5	5	5	5	5	5
Dedicated (total without supplies)		6	6	6	6	6	6
V_{CC}		2	4	8	4	8	8
V_{CCAUX}		2	2	2	2	2	4
V_{CCPLL}		2	2	2	2	2	2
V_{CCIO}	Bank0	1	1	2	1	2	2
	Bank1	1	1	2	1	2	2
	Bank2	1	1	2	1	2	2
	Bank3	1	1	2	1	2	2
	Bank4	1	2	2	2	2	2
	Bank5	1	1	2	1	2	2
	Bank6	1	1	2	1	2	2
	Bank7	1	1	2	1	2	2
GND		10	13	24	13	24	24
GND_{PLL}		2	2	2	2	2	2
NC		0	0	6	0	0	0
Single Ended/Differential I/O per Bank[2]	Bank0	8/2	12/3	20/8	12/3	20/8	26/11
	Bank1	9/0	12/2	18/6	12/2	18/6	26/11
	Bank2	8/3	12/5	14/6	12/5	17/7	21/9
	Bank3	6/2	13/5	14/6	13/5	14/6	21/9
	Bank4	5/2	14/6	21/9	14/6	21/9	26/11
	Bank5	12/4	12/4	21/9	12/4	21/9	26/11
	Bank6	4/2	13/5	14/6	13/5	17/7	21/9
	Bank7	10/4	12/5	14/6	12/5	14/6	21/9
V_{CCJ}		1	1	1	1	1	1

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
2. The differential I/O per bank includes both dedicated LVDS and emulated LVDS pin pairs. Please see the Logic Signal Connections table for more information.

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA

	LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
C2	PROGRAMN	7	-	-	PROGRAMN	7	-	-
C1	CCLK	7	-	-	CCLK	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
D2	PL7A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A
D3	PL7B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A
D1	PL9A	7	-	-	PL9A	7	-	-
E2	PL10B	7	-	VREF1_7	PL10B	7	-	VREF1_7
E1	PL11A	7	T[3]	DQS	PL11A	7	T[3]	DQS
F1	PL11B	7	C[3]	-	PL11B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
E3	PL12A	7	T	-	PL12A	7	T	-
F4	PL12B	7	C	-	PL12B	7	C	-
F3	PL13A	7	T[3]	-	PL13A	7	T[3]	-
F2	PL13B	7	C[3]	-	PL13B	7	C[3]	-
G1	PL15B	7	-	-	PL15B	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
G3	PL16A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A
G2	PL16B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A
H1	PL17A	7	T[3]	-	PL17A	7	T[3]	-
H2	PL17B	7	C[3]	-	PL17B	7	C[3]	-
G4	PL18A	7	-	VREF2_7	PL18A	7	-	VREF2_7
G5	PL19B	7	-	-	PL19B	7	-	-
J1	PL20A	7	T[3]	DQS	PL20A	7	T[3]	DQS
-	GNDIO7	7	-	-	GNDIO7	7	-	-
J2	PL20B	7	C[3]	-	PL20B	7	C[3]	-
H3	PL22A	7	T[3]	-	PL22A	7	T[3]	-
J3	PL22B	7	C[3]	-	PL22B	7	C[3]	-
H4	VCCP0	-	-	-	VCCP0	-	-	-
H5	GNDP0	-	-	-	GNDP0	-	-	-
K1	PL24A	6	T	PCLKT6_0	PL28A	6	T	PCLKT6_0
-	GNDIO6	6	-	-	GNDIO6	6	-	-
K2	PL24B	6	C	PCLKC6_0	PL28B	6	C	PCLKC6_0
J4	PL26A	6	-	-	PL30A	6	-	-
J5	PL27B	6	-	VREF1_6	PL31B	6	-	VREF1_6
L1	PL28A	6	T[3]	DQS	PL32A	6	T[3]	DQS
L2	PL28B	6	C[3]	-	PL32B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
M1	PL29A	6	T	LLM0_PLLT_IN_A	PL33A	6	T	LLM0_PLLT_IN_A
M2	PL29B	6	C	LLM0_PLLC_IN_A	PL33B	6	C	LLM0_PLLC_IN_A
K3	PL30A	6	T[3]	-	PL34A	6	T[3]	-
L3	PL30B	6	C[3]	-	PL34B	6	C[3]	-

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

	LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
T7	PB23B	5	C	-	PB27B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
P8	PB24A	5	T	-	PB28A	5	T	-
T8	PB24B	5	C	-	PB28B	5	C	-
R8	PB25A	5	T	-	PB29A	5	T	-
T9	PB25B	5	C	-	PB29B	5	C	-
R9	PB26A	4	T	-	PB30A	4	T	-
P9	PB26B	4	C	-	PB30B	4	C	-
T10	PB27A	4	T	PCLKT4_0	PB31A	4	T	PCLKT4_0
T11	PB27B	4	C	PCLKC4_0	PB31B	4	C	PCLKC4_0
-	GNDIO4	4	-	-	GNDIO4	4	-	-
R10	PB28A	4	T	-	PB32A	4	T	-
P10	PB28B	4	C	-	PB32B	4	C	-
N9	PB29A	4	-	-	PB33A	4	-	-
M9	PB30B	4	-	-	PB34B	4	-	-
R12	PB31A	4	T	DQS	PB35A	4	T	DQS
T12	PB31B	4	C	VREF1_4	PB35B	4	C	VREF1_4
P13	PB32A	4	T	-	PB36A	4	T	-
R13	PB32B	4	C	-	PB36B	4	C	-
M11	PB33A	4	T	-	PB37A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
N11	PB33B	4	C	-	PB37B	4	C	-
N10	PB34A	4	T	-	PB38A	4	T	-
M10	PB34B	4	C	-	PB38B	4	C	-
T13	PB35A	4	T	-	PB39A	4	T	-
P14	PB35B	4	C	-	PB39B	4	C	-
R11	PB36A	4	T	VREF2_4	PB40A	4	T	VREF2_4
P12	PB36B	4	C	-	PB40B	4	C	-
T14	PB37A	4	-	-	PB41A	4	-	-
R14	PB38B	4	-	-	PB42B	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
P11	PB39A	4	T	DQS	PB43A	4	T	DQS
N12	PB39B	4	C	-	PB43B	4	C	-
T15	PB40A	4	T	-	PB44A	4	T	-
R15	PB40B	4	C	-	PB44B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
P15	PR38B	3	C	RLM0_PLLC_FB_A	PR42B	3	C	RLM0_PLLC_FB_A
N15	PR38A	3	T	RLM0_PLLT_FB_A	PR42A	3	T	RLM0_PLLT_FB_A

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15 Ball Function	LFXP15 Bank	LFXP15 Differential	LFXP15 Dual Function	LFXP20 Ball Function	LFXP20 Bank	LFXP20 Differential	LFXP20 Dual Function
P16	PR37B	3	C[3]	-	PR41B	3	C[3]	-
R16	PR37A	3	T[3]	DQS	PR41A	3	T[3]	DQS
M15	PR36B	3	-	-	PR40B	3	-	-
N14	PR35A	3	-	VREF1_3	PR39A	3	-	VREF1_3
-	GNDIO3	3	-	-	GNDIO3	3	-	-
M14	PR33B	3	C	-	PR37B	3	C	-
L13	PR33A	3	T	-	PR37A	3	T	-
L15	PR32B	3	C[3]	-	PR36B	3	C[3]	-
L14	PR32A	3	T[3]	-	PR36A	3	T[3]	-
L12	PR30A	3	-	-	PR34A	3	-	-
M16	PR29B	3	C	RLM0_PLLC_IN_A	PR33B	3	C	RLM0_PLLC_IN_A
N16	PR29A	3	T	RLM0_PLLT_IN_A	PR33A	3	T	RLM0_PLLT_IN_A
-	GNDIO3	3	-	-	GNDIO3	3	-	-
K14	PR28B	3	C[3]	-	PR32B	3	C[3]	-
K15	PR28A	3	T[3]	DQS	PR32A	3	T[3]	DQS
K12	PR27B	3	-	-	PR31B	3	-	-
K13	PR26A	3	-	VREF2_3	PR30A	3	-	VREF2_3
L16	PR25B	3	C[3]	-	PR29B	3	C[3]	-
K16	PR25A	3	T[3]	-	PR29A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
J15	PR23B	3	C[3]	-	PR27B	3	C[3]	-
J14	PR23A	3	T[3]	-	PR27A	3	T[3]	-
J13	GNDP1	-	-	-	GNDP1	-	-	-
J12	VCCP1	-	-	-	VCCP1	-	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
J16	PR21B	2	C	PCLKC2_0	PR21B	2	C	PCLKC2_0
H16	PR21A	2	T	PCLKT2_0	PR21A	2	T	PCLKT2_0
H13	PR20B	2	C[3]	-	PR20B	2	C[3]	-
H12	PR20A	2	T[3]	DQS	PR20A	2	T[3]	DQS
H15	PR19B	2	-	-	PR19B	2	-	-
H14	PR18A	2	-	VREF1_2	PR18A	2	-	VREF1_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G15	PR17B	2	C[3]	-	PR17B	2	C[3]	-
G14	PR17A	2	T[3]	-	PR17A	2	T[3]	-
G16	PR16B	2	C	RUM0_PLLC_IN_A	PR16B	2	C	RUM0_PLLC_IN_A
F16	PR16A	2	T	RUM0_PLLT_IN_A	PR16A	2	T	RUM0_PLLT_IN_A
G13	PR15B	2	-	-	PR15B	2	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G12	PR12B	2	C	-	PR12B	2	C	-
F13	PR12A	2	T	-	PR12A	2	T	-
B16	PR11B	2	C[3]	-	PR11B	2	C[3]	-
C16	PR11A	2	T[3]	DQS	PR11A	2	T[3]	DQS

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15 Ball Function	LFXP15 Bank	LFXP15 Differential	LFXP15 Dual Function	LFXP20 Ball Function	LFXP20 Bank	LFXP20 Differential	LFXP20 Dual Function
-	GNDIO2	2	-	-	GNDIO2	2	-	-
F15	PR10B	2	-	-	PR10B	2	-	-
E15	PR9A	2	-	VREF2_2	PR9A	2	-	VREF2_2
F14	PR8B	2	C[3]	-	PR8B	2	C[3]	-
E14	PR8A	2	T[3]	-	PR8A	2	T[3]	-
D15	PR7B	2	C	RUM0_PLLC_FB_A	PR7B	2	C	RUM0_PLLC_FB_A
C15	PR7A	2	T	RUM0_PLLT_FB_A	PR7A	2	T	RUM0_PLLT_FB_A
-	GNDIO2	2	-	-	GNDIO2	2	-	-
E16	TDO	-	-	-	TDO	-	-	-
D16	VCCJ	-	-	-	VCCJ	-	-	-
D14	TDI	-	-	-	TDI	-	-	-
C14	TMS	-	-	-	TMS	-	-	-
B14	TCK	-	-	-	TCK	-	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
A15	PT40B	1	C	-	PT44B	1	C	-
B15	PT40A	1	T	-	PT44A	1	T	-
D12	PT39B	1	C	VREF1_1	PT43B	1	C	VREF1_1
-	GNDIO1	1	-	-	GNDIO1	1	-	-
C11	PT39A	1	T	DQS	PT43A	1	T	DQS
A14	PT38B	1	-	-	PT42B	1	-	-
B13	PT37A	1	-	-	PT41A	1	-	-
F12	PT36B	1	C	-	PT40B	1	C	-
E11	PT36A	1	T	-	PT40A	1	T	-
A13	PT35B	1	C	-	PT39B	1	C	-
C13	PT35A	1	T	D0	PT39A	1	T	D0
C10	PT34B	1	C	D1	PT38B	1	C	D1
E10	PT34A	1	T	VREF2_1	PT38A	1	T	VREF2_1
A12	PT33B	1	C	-	PT37B	1	C	-
B12	PT33A	1	T	D2	PT37A	1	T	D2
-	GNDIO1	1	-	-	GNDIO1	1	-	-
C12	PT32B	1	C	D3	PT36B	1	C	D3
A11	PT32A	1	T	-	PT36A	1	T	-
B11	PT31B	1	C	-	PT35B	1	C	-
D11	PT31A	1	T	DQS	PT35A	1	T	DQS
B9	PT30B	1	-	-	PT34B	1	-	-
D9	PT29A	1	-	D4	PT33A	1	-	D4
A10	PT28B	1	C	-	PT32B	1	C	-
B10	PT28A	1	T	D5	PT32A	1	T	D5
-	GNDIO1	1	-	-	GNDIO1	1	-	-
D10	PT27B	1	C	D6	PT31B	1	C	D6

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

	LFXP10				LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
AA20	PB36B	4	C	-	PB41B	4	C	-	PB45B	4	C	-
AB21	PB37A	4	T	-	PB42A	4	T	-	PB46A	4	T	-
AA21	PB37B	4	C	-	PB42B	4	C	-	PB46B	4	C	-
AA22	PB38A	4	T	-	PB43A	4	T	-	PB47A	4	T	-
Y21	PB38B	4	C	-	PB43B	4	C	-	PB47B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
W16	PB39A	4	-	-	PB44A	4	T	-	PB48A	4	T	-
W17	-	-	-	-	PB44B	4	C	-	PB48B	4	C	-
Y15	-	-	-	-	PB45A	4	-	-	PB49A	4	-	-
Y16	-	-	-	-	PB46B	4	-	-	PB50B	4	-	-
W19	-	-	-	-	PB47A	4	T	DQS	PB51A	4	T	DQS
W18	-	-	-	-	PB47B	4	C	-	PB51B	4	C	-
W20	-	-	-	-	PB48A	4	-	-	PB52A	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
T20	PR35B	3	C[3]	-	PR39B	3	C[3]	-	PR43B	3	C[3]	-
T19	PR35A	3	T[3]	-	PR39A	3	T[3]	-	PR43A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
U19	PR34B	3	C	RLM0_PLLC_FB_A	PR38B	3	C	RLM0_PLLC_FB_A	PR42B	3	C	RLM0_PLLC_FB_A
U20	PR34A	3	T	RLM0_PLLT_FB_A	PR38A	3	T	RLM0_PLLT_FB_A	PR42A	3	T	RLM0_PLLT_FB_A
V19	PR33B	3	C[3]	-	PR37B	3	C[3]	-	PR41B	3	C[3]	-
V20	PR33A	3	T[3]	DQS	PR37A	3	T[3]	DQS	PR41A	3	T[3]	DQS
R19	PR32B	3	-	-	PR36B	3	-	-	PR40B	3	-	-
R20	PR31A	3	-	VREF1_3	PR35A	3	-	VREF1_3	PR39A	3	-	VREF1_3
W21	PR30B	3	C[3]	-	PR34B	3	C[3]	-	PR38B	3	C[3]	-
Y22	PR30A	3	T[3]	-	PR34A	3	T[3]	-	PR38A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
P19	PR29B	3	C	-	PR33B	3	C	-	PR37B	3	C	-
P20	PR29A	3	T	-	PR33A	3	T	-	PR37A	3	T	-
V21	PR28B	3	C[3]	-	PR32B	3	C[3]	-	PR36B	3	C[3]	-
W22	PR28A	3	T[3]	-	PR32A	3	T[3]	-	PR36A	3	T[3]	-
U21	PR26B	3	C[3]	-	PR30B	3	C[3]	-	PR34B	3	C[3]	-
V22	PR26A	3	T[3]	-	PR30A	3	T[3]	-	PR34A	3	T[3]	-
T21	PR25B	3	C	RLM0_PLLC_IN_A	PR29B	3	C	RLM0_PLLC_IN_A	PR33B	3	C	RLM0_PLLC_IN_A
U22	PR25A	3	T	RLM0_PLLT_IN_A	PR29A	3	T	RLM0_PLLT_IN_A	PR33A	3	T	RLM0_PLLT_IN_A
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
R21	PR24B	3	C[3]	-	PR28B	3	C[3]	-	PR32B	3	C[3]	-
T22	PR24A	3	T[3]	DQS	PR28A	3	T[3]	DQS	PR32A	3	T[3]	DQS
N19	PR23B	3	-	-	PR27B	3	-	-	PR31B	3	-	-
N20	PR22A	3	-	VREF2_3	PR26A	3	-	VREF2_3	PR30A	3	-	VREF2_3
R22	PR21B	3	C[3]	-	PR25B	3	C[3]	-	PR29B	3	C[3]	-
P22	PR21A	3	T[3]	-	PR25A	3	T[3]	-	PR29A	3	T[3]	-
P21	PR20B	3	C	-	PR24B	3	C	-	PR28B	3	C	-
N21	PR20A	3	T	-	PR24A	3	T	-	PR28A	3	T	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
M20	PR19B	3	C[3]	-	PR23B	3	C[3]	-	PR27B	3	C[3]	-
M19	PR19A	3	T[3]	-	PR23A	3	T[3]	-	PR27A	3	T[3]	-
N22	GNDP1	-	-	-	GNDP1	-	-	-	GNDP1	-	-	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

	LFXP10				LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
C20	PT38A	1	T	-	PT43A	1	T	-	PT47A	1	T	-
C21	PT37B	1	C	-	PT42B	1	C	-	PT46B	1	C	-
C22	PT37A	1	T	-	PT42A	1	T	-	PT46A	1	T	-
B22	PT36B	1	C	-	PT41B	1	C	-	PT45B	1	C	-
A21	PT36A	1	T	-	PT41A	1	T	-	PT45A	1	T	-
D15	PT35B	1	C	-	PT40B	1	C	-	PT44B	1	C	-
D14	PT35A	1	T	-	PT40A	1	T	-	PT44A	1	T	-
B21	PT34B	1	C	VREF1_1	PT39B	1	C	VREF1_1	PT43B	1	C	VREF1_1
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
A20	PT34A	1	T	DQS	PT39A	1	T	DQS	PT43A	1	T	DQS
B20	PT33B	1	-	-	PT38B	1	-	-	PT42B	1	-	-
A19	PT32A	1	-	-	PT37A	1	-	-	PT41A	1	-	-
B19	PT31B	1	C	-	PT36B	1	C	-	PT40B	1	C	-
A18	PT31A	1	T	-	PT36A	1	T	-	PT40A	1	T	-
C14	PT30B	1	C	-	PT35B	1	C	-	PT39B	1	C	-
C13	PT30A	1	T	D0	PT35A	1	T	D0	PT39A	1	T	D0
B18	PT29B	1	C	D1	PT34B	1	C	D1	PT38B	1	C	D1
A17	PT29A	1	T	VREF2_1	PT34A	1	T	VREF2_1	PT38A	1	T	VREF2_1
B17	PT28B	1	C	-	PT33B	1	C	-	PT37B	1	C	-
A16	PT28A	1	T	D2	PT33A	1	T	D2	PT37A	1	T	D2
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
B16	PT27B	1	C	D3	PT32B	1	C	D3	PT36B	1	C	D3
A15	PT27A	1	T	-	PT32A	1	T	-	PT36A	1	T	-
B15	PT26B	1	C	-	PT31B	1	C	-	PT35B	1	C	-
A14	PT26A	1	T	DQS	PT31A	1	T	DQS	PT35A	1	T	DQS
D13	PT25B	1	-	-	PT30B	1	-	-	PT34B	1	-	-
D12	PT24A	1	-	D4	PT29A	1	-	D4	PT33A	1	-	D4
B14	PT23B	1	C	-	PT28B	1	C	-	PT32B	1	C	-
A13	PT23A	1	T	D5	PT28A	1	T	D5	PT32A	1	T	D5
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
B13	PT22B	1	C	D6	PT27B	1	C	D6	PT31B	1	C	D6
A12	PT22A	1	T	-	PT27A	1	T	-	PT31A	1	T	-
B12	PT21B	1	C	D7	PT26B	1	C	D7	PT30B	1	C	D7
C12	PT21A	1	T	-	PT26A	1	T	-	PT30A	1	T	-
C11	PT20B	0	C	BUSY	PT25B	0	C	BUSY	PT29B	0	C	BUSY
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
B11	PT20A	0	T	CS1N	PT25A	0	T	CS1N	PT29A	0	T	CS1N
A11	PT19B	0	C	PCLKC0_0	PT24B	0	C	PCLKC0_0	PT28B	0	C	PCLKC0_0
A10	PT19A	0	T	PCLKT0_0	PT24A	0	T	PCLKT0_0	PT28A	0	T	PCLKT0_0
B10	PT18B	0	C	-	PT23B	0	C	-	PT27B	0	C	-
B9	PT18A	0	T	DQS	PT23A	0	T	DQS	PT27A	0	T	DQS
D11	PT17B	0	-	-	PT22B	0	-	-	PT26B	0	-	-
D10	PT16A	0	-	DOUT	PT21A	0	-	DOUT	PT25A	0	-	DOUT
A9	PT15B	0	C	-	PT20B	0	C	-	PT24B	0	C	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C8	PT15A	0	T	WRITEN	PT20A	0	T	WRITEN	PT24A	0	T	WRITEN
B8	PT14B	0	C	-	PT19B	0	C	-	PT23B	0	C	-
A8	PT14A	0	T	VREF1_0	PT19A	0	T	VREF1_0	PT23A	0	T	VREF1_0
C7	PT13B	0	C	-	PT18B	0	C	-	PT22B	0	C	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

	LFXP10				LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
A7	PT13A	0	T	DI	PT18A	0	T	DI	PT22A	0	T	DI
B7	PT12B	0	C	-	PT17B	0	C	-	PT21B	0	C	-
C6	PT12A	0	T	CSN	PT17A	0	T	CSN	PT21A	0	T	CSN
C10	PT11B	0	C	-	PT16B	0	C	-	PT20B	0	C	-
C9	PT11A	0	T	-	PT16A	0	T	-	PT20A	0	T	-
A6	PT10B	0	C	VREF2_0	PT15B	0	C	VREF2_0	PT19B	0	C	VREF2_0
B6	PT10A	0	T	DQS	PT15A	0	T	DQS	PT19A	0	T	DQS
A5	PT9B	0	-	-	PT14B	0	-	-	PT18B	0	-	-
B5	PT8A	0	-	-	PT13A	0	-	-	PT17A	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C5	PT7B	0	C	-	PT12B	0	C	-	PT16B	0	C	-
A4	PT7A	0	T	-	PT12A	0	T	-	PT16A	0	T	-
D9	PT6B	0	C	-	PT11B	0	C	-	PT15B	0	C	-
D8	PT6A	0	T	-	PT11A	0	T	-	PT15A	0	T	-
B4	PT5B	0	C	-	PT10B	0	C	-	PT14B	0	C	-
A2	PT5A	0	T	-	PT10A	0	T	-	PT14A	0	T	-
A3	PT4B	0	C	-	PT9B	0	C	-	PT13B	0	C	-
B3	PT4A	0	T	-	PT9A	0	T	-	PT13A	0	T	-
C4	PT3B	0	C	-	PT8B	0	C	-	PT12B	0	C	-
C3	PT3A	0	T	-	PT8A	0	T	-	PT12A	0	T	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C2	-	-	-	-	PT7B	0	C	-	PT11B	0	C	-
D3	PT2A	0	-	-	PT7A	0	T	DQS	PT11A	0	T	DQS
D7	-	-	-	-	PT6B	0	-	-	PT10B	0	-	-
D6	-	-	-	-	PT5A	0	-	-	PT9A	0	-	-
E4	-	-	-	-	PT4B	0	C	-	PT8B	0	C	-
D4	-	-	-	-	PT4A	0	T	-	PT8A	0	T	-
D5	-	-	-	-	PT3B	0	-	-	PT7B	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C1	CFG0	0	-	-	CFG0	0	-	-	CFG0	0	-	-
B2	CFG1	0	-	-	CFG1	0	-	-	CFG1	0	-	-
B1	DONE	0	-	-	DONE	0	-	-	DONE	0	-	-
A1	GND	-	-	-	GND	-	-	-	GND	-	-	-
A22	GND	-	-	-	GND	-	-	-	GND	-	-	-
AB1	GND	-	-	-	GND	-	-	-	GND	-	-	-
AB22	GND	-	-	-	GND	-	-	-	GND	-	-	-
H10	GND	-	-	-	GND	-	-	-	GND	-	-	-
H11	GND	-	-	-	GND	-	-	-	GND	-	-	-
H12	GND	-	-	-	GND	-	-	-	GND	-	-	-
H13	GND	-	-	-	GND	-	-	-	GND	-	-	-
H14	GND	-	-	-	GND	-	-	-	GND	-	-	-
J10	GND	-	-	-	GND	-	-	-	GND	-	-	-
J11	GND	-	-	-	GND	-	-	-	GND	-	-	-
J12	GND	-	-	-	GND	-	-	-	GND	-	-	-
J13	GND	-	-	-	GND	-	-	-	GND	-	-	-
J14	GND	-	-	-	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-	GND	-	-	-
K10	GND	-	-	-	GND	-	-	-	GND	-	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

	LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
H13	VCCIO1	1	-	-	VCCIO1	1	-	-
K15	VCCIO2	2	-	-	VCCIO2	2	-	-
L15	VCCIO2	2	-	-	VCCIO2	2	-	-
L16	VCCIO2	2	-	-	VCCIO2	2	-	-
L17	VCCIO2	2	-	-	VCCIO2	2	-	-
M15	VCCIO3	3	-	-	VCCIO3	3	-	-
M16	VCCIO3	3	-	-	VCCIO3	3	-	-
M17	VCCIO3	3	-	-	VCCIO3	3	-	-
N15	VCCIO3	3	-	-	VCCIO3	3	-	-
R12	VCCIO4	4	-	-	VCCIO4	4	-	-
R13	VCCIO4	4	-	-	VCCIO4	4	-	-
T12	VCCIO4	4	-	-	VCCIO4	4	-	-
U12	VCCIO4	4	-	-	VCCIO4	4	-	-
R10	VCCIO5	5	-	-	VCCIO5	5	-	-
R11	VCCIO5	5	-	-	VCCIO5	5	-	-
T11	VCCIO5	5	-	-	VCCIO5	5	-	-
U11	VCCIO5	5	-	-	VCCIO5	5	-	-
M6	VCCIO6	6	-	-	VCCIO6	6	-	-
M7	VCCIO6	6	-	-	VCCIO6	6	-	-
M8	VCCIO6	6	-	-	VCCIO6	6	-	-
N8	VCCIO6	6	-	-	VCCIO6	6	-	-
K8	VCCIO7	7	-	-	VCCIO7	7	-	-
L6	VCCIO7	7	-	-	VCCIO7	7	-	-
L7	VCCIO7	7	-	-	VCCIO7	7	-	-
L8	VCCIO7	7	-	-	VCCIO7	7	-	-

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

LatticeXP Family Data Sheet
Ordering Information

December 2005 Data Sheet DS1001

Part Number Description

LFXP XX X – X XXXXXX X

Device Family
LatticeXP FPGA

Logic Capacity
3K LUTs = 3
6K LUTs = 6
10K LUTs = 10
15K LUTs = 15
20K LUTs = 20

Supply Voltage
C = 1.8V/2.5V/3.3V
E = 1.2V

Note: Parts dual marked per table below.

Speed
3 = Slowest
4
5 = Fastest

Package
T100 = 100-pin TQFP
T144 = 144-pin TQFP
Q208 = 208-pin PQFP
F256 = 256-ball fpBGA
F388 = 388-ball fpBGA
F484 = 484-ball fpBGA

TN100 = 100-pin Lead-free TQFP
TN144 = 144-pin Lead-free TQFP
QN208 = 208-pin Lead-free PQFP
FN256 = 256-ball Lead-free fpBGA
FN388 = 388-ball Lead-free fpBGA
FN484 = 484-ball Lead-free fpBGA

Grade
C = Commercial
I = Industrial

Ordering Information (Contact Factory for Specific Device Availability)

Note:þLatticeXP devices are dual marked. For example, the commercial speed grade LFXP10E-4F256C is also marked with industrial grade -3I (LFXP10E-3F256I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:

Commercial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15C-3F484C	300	1.8/2.5/3.3V	-3	fpBGA	484	COM	15.5K
LFXP15C-4F484C	300	1.8/2.5/3.3V	-4	fpBGA	484	COM	15.5K
LFXP15C-5F484C	300	1.8/2.5/3.3V	-5	fpBGA	484	COM	15.5K
LFXP15C-3F388C	268	1.8/2.5/3.3V	-3	fpBGA	388	COM	15.5K
LFXP15C-4F388C	268	1.8/2.5/3.3V	-4	fpBGA	388	COM	15.5K
LFXP15C-5F388C	268	1.8/2.5/3.3V	-5	fpBGA	388	COM	15.5K
LFXP15C-3F256C	188	1.8/2.5/3.3V	-3	fpBGA	256	COM	15.5K
LFXP15C-4F256C	188	1.8/2.5/3.3V	-4	fpBGA	256	COM	15.5K
LFXP15C-5F256C	188	1.8/2.5/3.3V	-5	fpBGA	256	COM	15.5K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20C-3F484C	340	1.8/2.5/3.3V	-3	fpBGA	484	COM	19.7K
LFXP20C-4F484C	340	1.8/2.5/3.3V	-4	fpBGA	484	COM	19.7K
LFXP20C-5F484C	340	1.8/2.5/3.3V	-5	fpBGA	484	COM	19.7K
LFXP20C-3F388C	268	1.8/2.5/3.3V	-3	fpBGA	388	COM	19.7K
LFXP20C-4F388C	268	1.8/2.5/3.3V	-4	fpBGA	388	COM	19.7K
LFXP20C-5F388C	268	1.8/2.5/3.3V	-5	fpBGA	388	COM	19.7K
LFXP20C-3F256C	188	1.8/2.5/3.3V	-3	fpBGA	256	COM	19.7K
LFXP20C-4F256C	188	1.8/2.5/3.3V	-4	fpBGA	256	COM	19.7K
LFXP20C-5F256C	188	1.8/2.5/3.3V	-5	fpBGA	256	COM	19.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3E-3Q208C	136	1.2V	-3	PQFP	208	COM	3.1K
LFXP3E-4Q208C	136	1.2V	-4	PQFP	208	COM	3.1K
LFXP3E-5Q208C	136	1.2V	-5	PQFP	208	COM	3.1K
LFXP3E-3T144C	100	1.2V	-3	TQFP	144	COM	3.1K
LFXP3E-4T144C	100	1.2V	-4	TQFP	144	COM	3.1K
LFXP3E-5T144C	100	1.2V	-5	TQFP	144	COM	3.1K
LFXP3E-3T100C	62	1.2V	-3	TQFP	100	COM	3.1K
LFXP3E-4T100C	62	1.2V	-4	TQFP	100	COM	3.1K
LFXP3E-5T100C	62	1.2V	-5	TQFP	100	COM	3.1K

Industrial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10E-3FN388I	244	1.2V	-3	fpBGA	388	IND	9.7K
LFXP10E-4FN388I	244	1.2V	-4	fpBGA	388	IND	9.7K
LFXP10E-3FN256I	188	1.2V	-3	fpBGA	256	IND	9.7K
LFXP10E-4FN256I	188	1.2V	-4	fpBGA	256	IND	9.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15E-3FN484I	300	1.2V	-3	fpBGA	484	IND	15.5K
LFXP15E-4FN484I	300	1.2V	-4	fpBGA	484	IND	15.5K
LFXP15E-3FN388I	268	1.2V	-3	fpBGA	388	IND	15.5K
LFXP15E-4FN388I	268	1.2V	-4	fpBGA	388	IND	15.5K
LFXP15E-3FN256I	188	1.2V	-3	fpBGA	256	IND	15.5K
LFXP15E-4FN256I	188	1.2V	-4	fpBGA	256	IND	15.5K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20E-3FN484I	340	1.2V	-3	fpBGA	484	IND	19.7K
LFXP20E-4FN484I	340	1.2V	-4	fpBGA	484	IND	19.7K
LFXP20E-3FN388I	268	1.2V	-3	fpBGA	388	IND	19.7K
LFXP20E-4FN388I	268	1.2V	-4	fpBGA	388	IND	19.7K
LFXP20E-3FN256I	188	1.2V	-3	fpBGA	256	IND	19.7K
LFXP20E-4FN256I	188	1.2V	-4	fpBGA	256	IND	19.7K