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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| Product Status | Obsolete |
|--------------------------------|---|
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 15000 |
| Total RAM Bits | 331776 |
| Number of I/O | 268 |
| Number of Gates | - |
| Voltage - Supply | 1.71V ~ 3.465V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 388-BBGA |
| Supplier Device Package | 388-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp15c-3f388c |
| | |

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Table 2-4. PFU Modes of Operation

| Logic | Ripple | RAM ¹ | ROM |
|----------------------------|-------------------|----------------------------|-------------|
| LUT 4x8 or MUX 2x1 x 8 | 2-bit Add x 4 | SPR16x2 x 4 DPR16x2 x 2 | ROM16x1 x 8 |
| LUT 5x4 or MUX 4x1 x 4 | 2-bit Sub x 4 | SPR16x4 x 2 DPR16x4 x 1 | ROM16x2 x 4 |
| LUT 6x 2 or MUX 8x1 x 2 | 2-bit Counter x 4 | SPR16x8 x 1 | ROM16x4 x 2 |
| LUT 7x1 or MUX 16x1 x 1 | 2-bit Comp x 4 | | ROM16x8 x 1 |

1. These modes are not available in PFF blocks

Routing

There are many resources provided in the LatticeXP devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal, vertical and diagonal directions. The x2 and x6 resources are buffered allowing both short and long connections routing between PFUs.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock Distribution Network

The clock inputs are selected from external I/O, the sysCLOCK[™] PLLs or routing. These clock inputs are fed through the chip via a clock distribution system.

Primary Clock Sources

LatticeXP devices derive clocks from three primary sources: PLL outputs, dedicated clock inputs and routing. LatticeXP devices have two to four sysCLOCK PLLs, located on the left and right sides of the device. There are four dedicated clock inputs, one on each side of the device. Figure 2-5 shows the 20 primary clock sources.

Figure 2-15. Memory Core Reset



For further information on sysMEM EBR block, see the details of additional technical documentation at the end of this data sheet.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-16. The GSR input to the EBR is always asynchronous.

Figure 2-16. EBR Asynchronous Reset (Including GSR) Timing Diagram

| Reset | |
|-----------------|--|
| Clock | |
| Clock Enable | |

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

Programmable I/O Cells (PICs)

Each PIC contains two PIOs connected to their respective sysIO Buffers which are then connected to the PADs as shown in Figure 2-17. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to sysIO buffer, and receives input from the buffer.

Figure 2-18. Group of Seven PIOs



One PIO Pair

Figure 2-19. DQS Routing

| | PIO A PIO B | ← PADA "T" LVDS Pair PADB "C" |
|-------------|----------------|---|
| | PIO A | PADA "T" |
| ├ ── | PIO B | ← PADB "C" |
| ┣ | PIO A | PADA "T" |
| | PIO B | ← PADB "C" |
| ┣─── | PIO A | ← PADA "T" |
| | | |
| | | |
| † | PIO B | ← PADB "C" |
| | PIO A | SysIO Buffer Delay PADA "T" LVDS Pair |
| | PIO B | ► PADB "C" |
| ┣ | PIO A | ← PADA "T" |
| ┣ | PIO B | PADB "C" |
| - | | |
| | PIO A | PADA "T" |

ΡΙΟ

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for both single data rate (SDR) and double data rate (DDR) operation along with the necessary clock and selection logic. Programmable delay lines used to shift incoming clock and data signals are also included in these blocks.

Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-20 shows the diagram of the input register block.

Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and

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in selected blocks the input to the DQS delay block. If one of the bypass options is not chosen, the signal first passes through an optional delay block. This delay, if selected, ensures no positive input-register hold-time requirement when using a global clock.

The input block allows two modes of operation. In the single data rate (SDR) the data is registered, by one of the registers in the single data rate sync register block, with the system clock. In the DDR Mode two registers are used to sample the data on the positive and negative edges of the DQS signal creating two data streams, D0 and D2. These two data streams are synchronized with the system clock before entering the core. Further discussion on this topic is in the DDR Memory section of this data sheet.

Figure 2-21 shows the input register waveforms for DDR operation and Figure 2-22 shows the design tool primitives. The SDR/SYNC registers have reset and clock enable available.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to the system clock domain. For further discussion of this topic, see the DDR memory section of this data sheet.



Figure 2-20. Input Register Diagram

Figure 2-23. Output Register Block



*Latch is transparent when input is low.

Figure 2-24. ODDRXB Primitive



Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-25 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a Dtype or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-26. DQS Local Bus



Figure 2-27. DLL Calibration Bus and DQS/DQS Transition Distribution



master serial clock is 2.5MHz. Table 2-10 lists all the available Master Serial Clock frequencies. When a different Master Serial Clock is selected during the design process, the following sequence takes place:

- 1. User selects a different Master Serial Clock frequency for configuration.
- 2. During configuration the device starts with the default (2.5MHz) Master Serial Clock frequency.
- 3. The clock configuration settings are contained in the early configuration bit stream.
- 4. The Master Serial Clock frequency changes to the selected frequency once the clock configuration bits are received.

For further information on the use of this oscillator for configuration, please see details of additional technical documentation at the end of this data sheet.

Table 2-10. Selectable Master Serial Clock (CCLK) Frequencies During Configuration

| CCLK (MHz) | CCLK (MHz) | CCLK (MHz) |
|------------------|------------|------------|
| 2.5 ¹ | 13 | 45 |
| 4.3 | 15 | 51 |
| 5.4 | 20 | 55 |
| 6.9 | 26 | 60 |
| 8.1 | 30 | 130 |
| 9.2 | 34 | — |
| 10.0 | 41 | — |
| 1. Default | • | • |

Density Shifting

The LatticeXP family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

LatticeXP Internal Timing Parameters¹

| | | -5 | | -4 | | -3 | | |
|-------------------------|---|-------|------|-------|------|-------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| PFU/PFF Logic | Mode Timing | | | | | | | |
| t _{LUT4_PFU} | LUT4 Delay (A to D Inputs to F Output) | — | 0.28 | | 0.34 | | 0.40 | ns |
| t _{LUT6_PFU} | LUT6 Delay (A to D Inputs to OFX Output) | | 0.44 | | 0.53 | | 0.63 | ns |
| t _{LSR_PFU} | Set/Reset to Output of PFU | | 0.90 | | 1.08 | | 1.29 | ns |
| t _{SUM_PFU} | Clock to Mux (M0,M1) Input Setup Time | 0.13 | | 0.15 | | 0.19 | _ | ns |
| t _{HM_PFU} | Clock to Mux (M0,M1) Input Hold Time | -0.04 | | -0.03 | — | -0.03 | _ | ns |
| t _{SUD_PFU} | Clock to D Input Setup Time | 0.13 | | 0.16 | | 0.19 | _ | ns |
| t _{HD_PFU} | Clock to D Input Hold Time | -0.03 | | -0.02 | — | -0.02 | | ns |
| t _{CK2Q_PFU} | Clock to Q Delay, D-type Register Configuration | | 0.40 | | 0.48 | | 0.58 | ns |
| t _{LE2Q_PFU} | Clock to Q Delay Latch Configuration | | 0.53 | | 0.64 | | 0.76 | ns |
| t _{LD2Q_PFU} | D to Q Throughput Delay when Latch is Enabled | — | 0.55 | — | 0.66 | | 0.79 | ns |
| PFU Dual Port M | Nemory Mode Timing | | | | | | | |
| t _{CORAM_PFU} | Clock to Output | | 0.40 | | 0.48 | | 0.58 | ns |
| t _{SUDATA_PFU} | Data Setup Time | -0.18 | | -0.14 | — | -0.11 | _ | ns |
| t _{HDATA_PFU} | Data Hold Time | 0.28 | | 0.34 | — | 0.40 | _ | ns |
| t _{SUADDR_PFU} | Address Setup Time | -0.46 | | -0.37 | — | -0.30 | _ | ns |
| t _{HADDR_PFU} | Address Hold Time | 0.71 | | 0.85 | — | 1.02 | _ | ns |
| t _{SUWREN_PFU} | Write/Read Enable Setup Time | -0.22 | | -0.17 | — | -0.14 | _ | ns |
| t _{HWREN_PFU} | Write/Read Enable Hold Time | 0.33 | | 0.40 | — | 0.48 | _ | ns |
| PIC Timing | | | | | | | | |
| PIO Input/Outpu | It Buffer Timing | | | | | | | |
| t _{IN_PIO} | Input Buffer Delay | | 0.62 | | 0.72 | | 0.85 | ns |
| t _{OUT_PIO} | Output Buffer Delay | — | 2.12 | | 2.54 | | 3.05 | ns |
| IOLOGIC Input/ | Output Timing | | | | | | | |
| t _{SUI_PIO} | Input Register Setup Time (Data Before Clock) | 1.35 | | 1.83 | | 2.37 | _ | ns |
| t _{HI_PIO} | Input Register Hold Time (Data After Clock) | 0.05 | | 0.05 | | 0.05 | | ns |
| t _{COO_PIO} | Output Register Clock to Output Delay | | 0.36 | | 0.44 | | 0.52 | ns |
| t _{SUCE_PIO} | Input Register Clock Enable Setup Time | -0.09 | — | -0.07 | — | -0.06 | _ | ns |
| t _{HCE_PIO} | Input Register Clock Enable Hold Time | 0.13 | | 0.16 | — | 0.19 | _ | ns |
| t _{SULSR_PIO} | Set/Reset Setup Time | 0.19 | | 0.23 | — | 0.28 | _ | ns |
| t _{HLSR_PIO} | Set/Reset Hold Time | -0.14 | — | -0.11 | — | -0.09 | _ | ns |
| EBR Timing | | | | | | | | |
| t _{CO_EBR} | Clock to Output from Address or Data | | 4.01 | | 4.81 | | 5.78 | ns |
| t _{COO_EBR} | Clock to Output from EBR Output Register | | 0.81 | | 0.97 | | 1.17 | ns |
| t _{SUDATA_EBR} | Setup Data to EBR Memory | -0.26 | | -0.21 | — | -0.17 | _ | ns |
| t _{HDATA_EBR} | Hold Data to EBR Memory | 0.41 | | 0.49 | — | 0.59 | _ | ns |
| t _{SUADDR_EBR} | Setup Address to EBR Memory | -0.26 | | -0.21 | — | -0.17 | _ | ns |
| t _{HADDR_EBR} | Hold Address to EBR Memory | 0.41 | — | 0.49 | — | 0.59 | — | ns |
| t _{SUWREN_EBR} | Setup Write/Read Enable to EBR Memory | -0.17 | — | -0.13 | — | -0.11 | — | ns |
| t _{HWREN_EBR} | Hold Write/Read Enable to EBR Memory | 0.26 | — | 0.31 | — | 0.37 | — | ns |
| t _{SUCE_EBR} | Clock Enable Setup Time to EBR Output Register | 0.19 | — | 0.23 | — | 0.28 | — | ns |
| t _{HCE EBR} | Clock Enable Hold Time to EBR Output Register | -0.13 | — | -0.10 | — | -0.08 | — | ns |

Over Recommended Operating Conditions

EBR Memory Timing Diagrams

Figure 3-8. Read Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

Figure 3-9. Read Mode with Input and Output Registers



LatticeXP sysCONFIG Port Timing Specifications

| Over | Recommended | Operating | Conditions |
|------|-------------|-------------|------------|
| •••• | | • por a mig | ••••••• |

| Parameter | Description | Min. | Max. | Units |
|--------------------------------|--|----------------------------|----------------------------|--------|
| sysCONFIG By | te Data Flow | I | 1 | |
| t _{SUCBDI} | Byte D[0:7] Setup Time to CCLK | 7 | _ | ns |
| t _{HCBDI} | Byte D[0:7] Hold Time to CCLK | 3 | — | ns |
| t _{CODO} | Clock to Dout in Flowthrough Mode | — | 12 | ns |
| t _{SUCS} | CS[0:1] Setup Time to CCLK | 7 | — | ns |
| t _{HCS} | CS[0:1] Hold Time to CCLK | 2 | — | ns |
| t _{SUWD} | Write Signal Setup Time to CCLK | 7 | — | ns |
| t _{HWD} | Write Signal Hold Time to CCLK | 2 | — | ns |
| t _{DCB} | CCLK to BUSY Delay Time | — | 12 | ns |
| t _{CORD} | Clock to Out for Read Data | _ | 12 | ns |
| sysCONFIG By | te Slave Clocking | • | | • |
| t _{BSCH} | Byte Slave Clock Minimum High Pulse | 6 | — | ns |
| t _{BSCL} | Byte Slave Clock Minimum Low Pulse | 8 | — | ns |
| t _{BSCYC} | Byte Slave Clock Cycle Time | 15 | — | ns |
| sysCONFIG Se | rial (Bit) Data Flow | | | |
| t _{SUSCDI} | DI (Data In) Setup Time to CCLK | 7 | — | ns |
| t _{HSCDI} | DI (Data In) Hold Time to CCLK | 2 | — | ns |
| t _{CODO} | Clock to Dout in Flowthrough Mode | _ | 12 | ns |
| sysCONFIG Se | rial Slave Clocking | | | |
| t _{SSCH} | Serial Slave Clock Minimum High Pulse | 6 | — | ns |
| t _{SSCL} | Serial Slave Clock Minimum Low Pulse | 6 | — | ns |
| sysCONFIG PC | DR, Initialization and Wake Up | | | |
| t _{ICFG} | Minimum Vcc to INIT High | — | 50 | ms |
| t _{VMC} | Time from t _{ICFG} to Valid Master Clock | — | 2 | us |
| t _{PRGMRJ} | Program Pin Pulse Rejection | — | 7 | ns |
| t _{PRGM} ² | PROGRAMN Low Time to Start Configuration | 25 | — | ns |
| t _{DINIT} | INIT Low Time | — | 1 | ms |
| t _{DPPINIT} | Delay Time from PROGRAMN Low to INIT Low | — | 37 | ns |
| t _{DINITD} | Delay Time from PROGRAMN Low to DONE Low | _ | 37 | ns |
| t _{IODISS} | User I/O Disable from PROGRAMN Low | _ | 25 | ns |
| t _{IOENSS} | User I/O Enabled Time from CCLK Edge During Wake-up Sequence | — | 25 | ns |
| t _{MWC} | Additional Wake Master Clock Signals after Done Pin High | 120 | — | cycles |
| Configuration I | Master Clock (CCLK) | | | |
| Frequency ¹ | | Selected Value - 30% | Selected Value + 30% | MHz |
| Duty Cycle | | 40 | 60 | % |

1. See Table 2-10 for available CCLK frequencies.

2. The threshold level for PROGRAMN, as well as for CFG[1] and CFG[0], is determined by V_{CC} , such that the threshold = $V_{CC}/2$. Timing v.F0.11

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

| Din | | LFXP3 | | LFXP6 | | | | |
|--------|---------------------------------------|-------|----------------|---------------|---------------------------------------|------|----------------|---------------|
| Number | Pin Function | Bank | Differential | Dual Function | Pin Function | Bank | Differential | Dual Function |
| 47 | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| 48 | PL18B | 6 | C ³ | - | PL26B | 6 | C ³ | - |
| 49 | GND | - | - | - | GND | - | - | - |
| 50 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| 51 | SLEEPN ¹ /TOE ² | - | - | - | SLEEPN ¹ /TOE ² | - | - | - |
| 52 | INITN | 5 | - | - | INITN | 5 | - | - |
| 53 | VCC | - | - | - | VCC | - | - | - |
| 54 | PB2B | 5 | - | VREF1_5 | PB5B | 5 | - | VREF1_5 |
| 55 | PB3A | 5 | Т | - | PB6A | 5 | Т | DQS |
| 56 | PB3B | 5 | С | - | PB6B | 5 | С | - |
| 57 | PB4A | 5 | Т | - | PB7A | 5 | Т | - |
| 58 | PB4B | 5 | С | - | PB7B | 5 | С | - |
| 59 | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| 60 | PB5A | 5 | Т | - | PB8A | 5 | Т | - |
| 61 | PB5B | 5 | С | VREF2_5 | PB8B | 5 | C | VREF2_5 |
| 62 | PB6A | 5 | Т | - | PB9A | 5 | Т | - |
| 63 | PB6B | 5 | С | - | PB9B | 5 | C | - |
| 64 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| 65 | PB7A | 5 | Т | - | PB10A | 5 | Т | - |
| 66 | PB7B | 5 | С | - | PB10B | 5 | C | - |
| 67 | PB8A | 5 | Т | - | PB11A | 5 | Т | - |
| 68 | PB8B | 5 | С | - | PB11B | 5 | C | - |
| 69 | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| 70 | PB9A | 5 | - | - | PB12A | 5 | - | - |
| 71 | PB10B | 5 | - | - | PB13B | 5 | - | - |
| 72 | PB11A | 5 | Т | DQS | PB14A | 5 | Т | DQS |
| 73 | PB11B | 5 | С | - | PB14B | 5 | С | - |
| 74 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| 75 | PB12A | 5 | T | - | PB15A | 5 | T | - |
| 76 | PB12B | 5 | C | - | PB15B | 5 | C | - |
| 77 | PB13A | 5 | T | - | PB16A | 5 | T | - |
| 78 | PB13B | 5 | С | - | PB16B | 5 | С | - |
| 79 | GND | - | - | - | GND | - | - | - |
| 80 | VCC | - | - | - | VCC | - | - | - |
| 81 | PB14A | 4 | I | - | PB17A | 4 | | - |
| 82 | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| 83 | PB14B | 4 | C T | - | PB17B | 4 | C | - |
| 84 | PB15A | 4 | | PCLK14_0 | PB18A | 4 | 1 | PCLK14_0 |
| 85 | PB15B | 4 | C T | PCLKC4_0 | PB18B | 4 | C | PCLKC4_0 |
| 86 | PB16A | 4 | Т | - | PB19A | 4 | Т | - |
| 87 | | 4 | - | - | VCCIO4 | 4 | - | - |
| 88 | PB16B | 4 | C | - | PB19B | 4 | C | - |
| 89 | PB17A | 4 | - | - | PB20A | 4 | - | - |
| 90 | PB18B | 4 | - | - | PB21B | 4 | - | - |
| 91 | PB19A | 4 | Г | DQS | PB22A | 4 | ſ | DQS |
| 92 | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

| | | | LFXP6 | | | | LFXP10 | |
|----------------|---------------------------------------|------|----------------|------------------|---------------------------------------|------|----------------|------------------|
| Ball Number | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| K4 | PL20A | 6 | Т | - | PL29A | 6 | Т | - |
| K5 | PL20B | 6 | С | - | PL29B | 6 | С | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| N1 | PL23B | 6 | - | VREF2_6 | PL31A | 6 | - | VREF2_6 |
| N2 | PL21B | 6 | C ³ | - | PL32B | 6 | - | - |
| P1 | PL24A | 6 | T ³ | DQS | PL33A | 6 | T ³ | DQS |
| P2 | PL24B | 6 | C ³ | - | PL33B | 6 | C ³ | - |
| L5 | PL25A | 6 | Т | - | PL34A | 6 | Т | LLM0_PLLT_FB_A |
| M6 | PL25B | 6 | С | - | PL34B | 6 | С | LLM0_PLLC_FB_A |
| M3 | PL26A | 6 | T ³ | - | PL35A | 6 | T ³ | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| N3 | PL26B | 6 | C ³ | - | PL35B | 6 | C ³ | - |
| P4 | SLEEPN ¹ /TOE ² | - | - | - | SLEEPN ¹ /TOE ² | - | - | - |
| P3 | INITN | 5 | - | - | INITN | 5 | - | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| R4 | PB2A | 5 | Т | - | PB6A | 5 | Т | - |
| N5 | PB2B | 5 | С | - | PB6B | 5 | С | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| P5 | PB5B | 5 | - | VREF1_5 | PB7A | 5 | Т | VREF1_5 |
| R1 | PB3B | 5 | С | - | PB7B | 5 | С | - |
| N6 | PB4A | 5 | - | - | PB8A | 5 | - | - |
| M7 | PB3A | 5 | Т | - | PB9B | 5 | - | - |
| R2 | PB6A | 5 | Т | DQS | PB10A | 5 | Т | DQS |
| T2 | PB6B | 5 | С | - | PB10B | 5 | С | - |
| R3 | PB7A | 5 | Т | - | PB11A | 5 | Т | - |
| Т3 | PB7B | 5 | С | - | PB11B | 5 | С | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| T4 | PB8A | 5 | Т | - | PB12A | 5 | Т | - |
| R5 | PB8B | 5 | С | VREF2_5 | PB12B | 5 | С | VREF2_5 |
| N7 | PB9A | 5 | Т | - | PB13A | 5 | Т | - |
| M8 | PB9B | 5 | С | - | PB13B | 5 | С | - |
| T5 | PB10A | 5 | Т | - | PB14A | 5 | Т | - |
| P6 | PB10B | 5 | С | - | PB14B | 5 | С | - |
| Т6 | PB11A | 5 | Т | - | PB15A | 5 | Т | - |
| R6 | PB11B | 5 | С | - | PB15B | 5 | С | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| P7 | PB12A | 5 | - | - | PB16A | 5 | - | - |
| N8 | PB13B | 5 | - | - | PB17B | 5 | - | - |
| R7 | PB14A | 5 | Т | DQS | PB18A | 5 | Т | DQS |
| T7 | PB14B | 5 | С | - | PB18B | 5 | С | - |
| P8 | PB15A | 5 | Т | - | PB19A | 5 | Т | - |
| Т8 | PB15B | 5 | C | - | PB19B | 5 | C | - |

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

| | | | LFXP6 | | | | LFXP10 | |
|----------------|------------------|------|----------------|------------------|------------------|------|----------------|------------------|
| Ball Number | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| R8 | PB16A | 5 | Т | - | PB20A | 5 | Т | - |
| Т9 | PB16B | 5 | С | - | PB20B | 5 | С | - |
| R9 | PB17A | 4 | Т | - | PB21A | 4 | Т | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| P9 | PB17B | 4 | С | - | PB21B | 4 | С | - |
| T10 | PB18A | 4 | Т | PCLKT4_0 | PB22A | 4 | Т | PCLKT4_0 |
| T11 | PB18B | 4 | С | PCLKC4_0 | PB22B | 4 | С | PCLKC4_0 |
| R10 | PB19A | 4 | Т | - | PB23A | 4 | Т | - |
| P10 | PB19B | 4 | С | - | PB23B | 4 | С | - |
| N9 | PB20A | 4 | - | - | PB24A | 4 | - | - |
| M9 | PB21B | 4 | - | - | PB25B | 4 | - | - |
| R12 | PB22A | 4 | Т | DQS | PB26A | 4 | Т | DQS |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| T12 | PB22B | 4 | С | VREF1_4 | PB26B | 4 | С | VREF1_4 |
| P13 | PB23A | 4 | Т | - | PB27A | 4 | Т | - |
| R13 | PB23B | 4 | С | - | PB27B | 4 | С | - |
| M11 | PB24A | 4 | Т | - | PB28A | 4 | Т | - |
| N11 | PB24B | 4 | С | - | PB28B | 4 | С | - |
| N10 | PB25A | 4 | Т | - | PB29A | 4 | Т | - |
| M10 | PB25B | 4 | С | - | PB29B | 4 | С | - |
| T13 | PB26A | 4 | Т | - | PB30A | 4 | Т | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| P14 | PB26B | 4 | С | - | PB30B | 4 | С | - |
| R11 | PB27A | 4 | Т | VREF2_4 | PB31A | 4 | Т | VREF2_4 |
| P12 | PB27B | 4 | С | - | PB31B | 4 | С | - |
| T14 | PB28A | 4 | - | - | PB32A | 4 | - | - |
| R14 | PB29B | 4 | - | - | PB33B | 4 | - | - |
| P11 | PB30A | 4 | Т | DQS | PB34A | 4 | Т | DQS |
| N12 | PB30B | 4 | С | - | PB34B | 4 | С | - |
| T15 | PB31A | 4 | Т | - | PB35A | 4 | Т | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| R15 | PB31B | 4 | С | - | PB35B | 4 | С | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| P15 | PR26B | 3 | C ³ | - | PR34B | 3 | С | RLM0_PLLC_FB_A |
| N15 | PR26A | 3 | T ³ | - | PR34A | 3 | Т | RLM0_PLLT_FB_A |
| P16 | PR24B | 3 | C³ | - | PR33B | 3 | C ³ | - |
| R16 | PR24A | 3 | T ³ | DQS | PR33A | 3 | T ³ | DQS |
| M15 | PR15B | 3 | - | - | PR32B | 3 | - | - |
| N14 | PR23B | 3 | - | VREF1_3 | PR31A | 3 | - | VREF1_3 |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| M14 | PR25B | 3 | С | - | PR29B | 3 | С | - |
| L13 | PR25A | 3 | Т | - | PR29A | 3 | Т | - |

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

| | | | LFXP20 | | | | | |
|----------------|------------------|------|----------------|------------------|------------------|------|----------------|------------------|
| Ball Number | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| F15 | PR10B | 2 | - | - | PR10B | 2 | - | - |
| E15 | PR9A | 2 | - | VREF2_2 | PR9A | 2 | - | VREF2_2 |
| F14 | PR8B | 2 | C ³ | - | PR8B | 2 | C ³ | - |
| E14 | PR8A | 2 | T ³ | - | PR8A | 2 | T ³ | - |
| D15 | PR7B | 2 | С | RUM0_PLLC_FB_A | PR7B | 2 | С | RUM0_PLLC_FB_A |
| C15 | PR7A | 2 | Т | RUM0_PLLT_FB_A | PR7A | 2 | Т | RUM0_PLLT_FB_A |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| E16 | TDO | - | - | - | TDO | - | - | - |
| D16 | VCCJ | - | - | - | VCCJ | - | - | - |
| D14 | TDI | - | - | - | TDI | - | - | - |
| C14 | TMS | - | - | - | TMS | - | - | - |
| B14 | ТСК | - | - | - | ТСК | - | - | - |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| A15 | PT40B | 1 | С | - | PT44B | 1 | С | - |
| B15 | PT40A | 1 | Т | - | PT44A | 1 | Т | - |
| D12 | PT39B | 1 | С | VREF1_1 | PT43B | 1 | С | VREF1_1 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| C11 | PT39A | 1 | Т | DQS | PT43A | 1 | Т | DQS |
| A14 | PT38B | 1 | - | - | PT42B | 1 | - | - |
| B13 | PT37A | 1 | - | - | PT41A | 1 | - | - |
| F12 | PT36B | 1 | С | - | PT40B | 1 | С | - |
| E11 | PT36A | 1 | Т | - | PT40A | 1 | Т | - |
| A13 | PT35B | 1 | С | - | PT39B | 1 | С | - |
| C13 | PT35A | 1 | Т | D0 | PT39A | 1 | Т | D0 |
| C10 | PT34B | 1 | С | D1 | PT38B | 1 | С | D1 |
| E10 | PT34A | 1 | Т | VREF2_1 | PT38A | 1 | Т | VREF2_1 |
| A12 | PT33B | 1 | С | - | PT37B | 1 | С | - |
| B12 | PT33A | 1 | Т | D2 | PT37A | 1 | Т | D2 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| C12 | PT32B | 1 | С | D3 | PT36B | 1 | С | D3 |
| A11 | PT32A | 1 | Т | - | PT36A | 1 | Т | - |
| B11 | PT31B | 1 | С | - | PT35B | 1 | С | - |
| D11 | PT31A | 1 | Т | DQS | PT35A | 1 | Т | DQS |
| B9 | PT30B | 1 | - | - | PT34B | 1 | - | - |
| D9 | PT29A | 1 | - | D4 | PT33A | 1 | - | D4 |
| A10 | PT28B | 1 | С | - | PT32B | 1 | С | - |
| B10 | PT28A | 1 | Т | D5 | PT32A | 1 | Т | D5 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| D10 | PT27B | 1 | С | D6 | PT31B | 1 | С | D6 |

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

| | | | LFXP15 | | LFXP20 | | | | |
|----------------|------------------|------|--------------|------------------|------------------|------|--------------|------------------|--|
| Ball Number | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function | |
| A9 | PT27A | 1 | Т | - | PT31A | 1 | Т | - | |
| C9 | PT26B | 1 | С | D7 | PT30B | 1 | С | D7 | |
| C8 | PT26A | 1 | Т | - | PT30A | 1 | Т | - | |
| E9 | PT25B | 0 | С | BUSY | PT29B | 0 | С | BUSY | |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - | |
| B8 | PT25A | 0 | Т | CS1N | PT29A | 0 | Т | CS1N | |
| A8 | PT24B | 0 | С | PCLKC0_0 | PT28B | 0 | С | PCLKC0_0 | |
| A7 | PT24A | 0 | Т | PCLKT0_0 | PT28A | 0 | Т | PCLKT0_0 | |
| B7 | PT23B | 0 | С | - | PT27B | 0 | С | - | |
| C7 | PT23A | 0 | Т | DQS | PT27A | 0 | Т | DQS | |
| E8 | PT22B | 0 | - | - | PT26B | 0 | - | - | |
| D8 | PT21A | 0 | - | DOUT | PT25A | 0 | - | DOUT | |
| A6 | PT20B | 0 | С | - | PT24B | 0 | С | - | |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - | |
| C6 | PT20A | 0 | Т | WRITEN | PT24A | 0 | Т | WRITEN | |
| E7 | PT19B | 0 | C | - | PT23B | 0 | С | - | |
| D7 | PT19A | 0 | Т | VREF1_0 | PT23A | 0 | Т | VREF1_0 | |
| A5 | PT18B | 0 | С | - | PT22B | 0 | С | - | |
| B5 | PT18A | 0 | Т | DI | PT22A | 0 | Т | DI | |
| A4 | PT17B | 0 | С | - | PT21B | 0 | С | - | |
| B6 | PT17A | 0 | Т | CSN | PT21A | 0 | Т | CSN | |
| E6 | PT16B | 0 | С | - | PT20B | 0 | С | - | |
| D6 | PT16A | 0 | Т | - | PT20A | 0 | Т | - | |
| D5 | PT15B | 0 | C | VREF2_0 | PT19B | 0 | С | VREF2_0 | |
| A3 | PT15A | 0 | Т | DQS | PT19A | 0 | Т | DQS | |
| B3 | PT14B | 0 | - | - | PT18B | 0 | - | - | |
| B2 | PT13A | 0 | - | - | PT17A | 0 | - | - | |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - | |
| A2 | PT12B | 0 | С | - | PT16B | 0 | С | - | |
| B1 | PT12A | 0 | Т | - | PT16A | 0 | Т | - | |
| F5 | PT11B | 0 | С | - | PT15B | 0 | С | - | |
| C5 | PT11A | 0 | Т | - | PT15A | 0 | Т | - | |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - | |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - | |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - | |
| C4 | CFG0 | 0 | - | - | CFG0 | 0 | - | - | |
| B4 | CFG1 | 0 | - | - | CFG1 | 0 | - | - | |
| C3 | DONE | 0 | - | - | DONE | 0 | - | - | |
| A1 | GND | - | - | - | GND | - | - | - | |
| A16 | GND | - | - | - | GND | - | - | - | |
| F11 | GND | - | - | - | GND | - | - | - | |
| F6 | GND | - | - | - | GND | - | - | - | |

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

| | LFXP10 | | | | L | FXP15 | LFXP20 | | | | | |
|----------------|------------------|------|-------|---------------|------------------|-------|--------|---------------|------------------|------|-------|---------------|
| Ball Number | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function |
| C20 | PT38A | 1 | Т | - | PT43A | 1 | Т | - | PT47A | 1 | Т | - |
| C21 | PT37B | 1 | С | - | PT42B | 1 | С | - | PT46B | 1 | С | - |
| C22 | PT37A | 1 | Т | - | PT42A | 1 | Т | - | PT46A | 1 | Т | - |
| B22 | PT36B | 1 | С | - | PT41B | 1 | С | - | PT45B | 1 | С | - |
| A21 | PT36A | 1 | Т | - | PT41A | 1 | Т | - | PT45A | 1 | Т | - |
| D15 | PT35B | 1 | С | - | PT40B | 1 | С | - | PT44B | 1 | С | - |
| D14 | PT35A | 1 | Т | - | PT40A | 1 | Т | - | PT44A | 1 | Т | - |
| B21 | PT34B | 1 | С | VREF1_1 | PT39B | 1 | С | VREF1_1 | PT43B | 1 | С | VREF1_1 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| A20 | PT34A | 1 | Т | DQS | PT39A | 1 | Т | DQS | PT43A | 1 | Т | DQS |
| B20 | PT33B | 1 | - | - | PT38B | 1 | - | - | PT42B | 1 | - | - |
| A19 | PT32A | 1 | - | - | PT37A | 1 | - | - | PT41A | 1 | - | - |
| B19 | PT31B | 1 | С | - | PT36B | 1 | С | - | PT40B | 1 | С | - |
| A18 | PT31A | 1 | Т | - | PT36A | 1 | Т | - | PT40A | 1 | Т | - |
| C14 | PT30B | 1 | С | - | PT35B | 1 | С | - | PT39B | 1 | С | - |
| C13 | PT30A | 1 | Т | D0 | PT35A | 1 | Т | D0 | PT39A | 1 | Т | D0 |
| B18 | PT29B | 1 | С | D1 | PT34B | 1 | С | D1 | PT38B | 1 | С | D1 |
| A17 | PT29A | 1 | Т | VREF2_1 | PT34A | 1 | Т | VREF2_1 | PT38A | 1 | Т | VREF2_1 |
| B17 | PT28B | 1 | С | - | PT33B | 1 | С | - | PT37B | 1 | С | - |
| A16 | PT28A | 1 | Т | D2 | PT33A | 1 | Т | D2 | PT37A | 1 | Т | D2 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| B16 | PT27B | 1 | С | D3 | PT32B | 1 | С | D3 | PT36B | 1 | С | D3 |
| A15 | PT27A | 1 | Т | - | PT32A | 1 | Т | - | PT36A | 1 | Т | - |
| B15 | PT26B | 1 | С | - | PT31B | 1 | С | - | PT35B | 1 | С | - |
| A14 | PT26A | 1 | Т | DQS | PT31A | 1 | Т | DQS | PT35A | 1 | Т | DQS |
| D13 | PT25B | 1 | - | - | PT30B | 1 | - | - | PT34B | 1 | - | - |
| D12 | PT24A | 1 | - | D4 | PT29A | 1 | - | D4 | PT33A | 1 | - | D4 |
| B14 | PT23B | 1 | С | - | PT28B | 1 | С | - | PT32B | 1 | С | - |
| A13 | PT23A | 1 | Т | D5 | PT28A | 1 | Т | D5 | PT32A | 1 | Т | D5 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| B13 | PT22B | 1 | С | D6 | PT27B | 1 | С | D6 | PT31B | 1 | С | D6 |
| A12 | PT22A | 1 | Т | - | PT27A | 1 | Т | - | PT31A | 1 | Т | - |
| B12 | PT21B | 1 | С | D7 | PT26B | 1 | С | D7 | PT30B | 1 | С | D7 |
| C12 | PT21A | 1 | Т | - | PT26A | 1 | Т | - | PT30A | 1 | Т | - |
| C11 | PT20B | 0 | С | BUSY | PT25B | 0 | С | BUSY | PT29B | 0 | С | BUSY |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| B11 | PT20A | 0 | Т | CS1N | PT25A | 0 | Т | CS1N | PT29A | 0 | Т | CS1N |
| A11 | PT19B | 0 | С | PCLKC0_0 | PT24B | 0 | С | PCLKC0_0 | PT28B | 0 | С | PCLKC0_0 |
| A10 | PT19A | 0 | Т | PCLKT0_0 | PT24A | 0 | Т | PCLKT0_0 | PT28A | 0 | Т | PCLKT0_0 |
| B10 | PT18B | 0 | С | - | PT23B | 0 | С | - | PT27B | 0 | С | - |
| B9 | PT18A | 0 | Т | DQS | PT23A | 0 | Т | DQS | PT27A | 0 | Т | DQS |
| D11 | PT17B | 0 | - | - | PT22B | 0 | - | - | PT26B | 0 | - | - |
| D10 | PT16A | 0 | - | DOUT | PT21A | 0 | - | DOUT | PT25A | 0 | - | DOUT |
| A9 | PT15B | 0 | С | - | PT20B | 0 | С | - | PT24B | 0 | С | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C8 | PT15A | 0 | Т | WRITEN | PT20A | 0 | Т | WRITEN | PT24A | 0 | Т | WRITEN |
| B8 | PT14B | 0 | С | - | PT19B | 0 | С | - | PT23B | 0 | С | - |
| A8 | PT14A | 0 | Т | VREF1_0 | PT19A | 0 | Т | VREF1_0 | PT23A | 0 | Т | VREF1_0 |
| C7 | PT13B | 0 | С | - | PT18B | 0 | С | - | PT22B | 0 | С | - |
| L] | | 1 | | | | | | l . | | | | 1 |

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

| | LFXP10 | | | | LFXP15 | | | | LFXP20 | | | |
|----------------|------------------|------|-------|---------------|------------------|------|-------|---------------|------------------|------|-------|---------------|
| Ball Number | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function |
| A7 | PT13A | 0 | Т | DI | PT18A | 0 | Т | DI | PT22A | 0 | Т | DI |
| B7 | PT12B | 0 | С | - | PT17B | 0 | С | - | PT21B | 0 | С | - |
| C6 | PT12A | 0 | Т | CSN | PT17A | 0 | Т | CSN | PT21A | 0 | Т | CSN |
| C10 | PT11B | 0 | С | - | PT16B | 0 | С | - | PT20B | 0 | С | - |
| C9 | PT11A | 0 | Т | - | PT16A | 0 | Т | - | PT20A | 0 | Т | - |
| A6 | PT10B | 0 | С | VREF2_0 | PT15B | 0 | С | VREF2_0 | PT19B | 0 | С | VREF2_0 |
| B6 | PT10A | 0 | Т | DQS | PT15A | 0 | Т | DQS | PT19A | 0 | Т | DQS |
| A5 | PT9B | 0 | - | - | PT14B | 0 | - | - | PT18B | 0 | - | - |
| B5 | PT8A | 0 | - | - | PT13A | 0 | - | - | PT17A | 0 | - | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C5 | PT7B | 0 | С | - | PT12B | 0 | С | - | PT16B | 0 | С | - |
| A4 | PT7A | 0 | Т | - | PT12A | 0 | Т | - | PT16A | 0 | Т | - |
| D9 | PT6B | 0 | С | - | PT11B | 0 | С | - | PT15B | 0 | С | - |
| D8 | PT6A | 0 | Т | - | PT11A | 0 | Т | - | PT15A | 0 | Т | - |
| B4 | PT5B | 0 | С | - | PT10B | 0 | С | - | PT14B | 0 | С | - |
| A2 | PT5A | 0 | Т | - | PT10A | 0 | Т | - | PT14A | 0 | Т | - |
| A3 | PT4B | 0 | С | - | PT9B | 0 | С | - | PT13B | 0 | С | - |
| B3 | PT4A | 0 | Т | - | PT9A | 0 | Т | - | PT13A | 0 | Т | - |
| C4 | PT3B | 0 | С | - | PT8B | 0 | С | - | PT12B | 0 | С | - |
| C3 | PT3A | 0 | Т | - | PT8A | 0 | Т | - | PT12A | 0 | Т | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C2 | - | - | - | - | PT7B | 0 | С | - | PT11B | 0 | С | - |
| D3 | PT2A | 0 | - | - | PT7A | 0 | Т | DQS | PT11A | 0 | Т | DQS |
| D7 | - | - | - | - | PT6B | 0 | - | - | PT10B | 0 | - | - |
| D6 | - | - | - | - | PT5A | 0 | - | - | PT9A | 0 | - | - |
| E4 | - | - | - | - | PT4B | 0 | С | - | PT8B | 0 | С | - |
| D4 | - | - | - | - | PT4A | 0 | Т | - | PT8A | 0 | Т | - |
| D5 | - | - | - | - | PT3B | 0 | - | - | PT7B | 0 | - | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C1 | CFG0 | 0 | - | - | CFG0 | 0 | - | - | CFG0 | 0 | - | - |
| B2 | CFG1 | 0 | - | - | CFG1 | 0 | - | - | CFG1 | 0 | - | - |
| B1 | DONE | 0 | - | - | DONE | 0 | - | - | DONE | 0 | - | - |
| A1 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| A22 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| AB1 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| AB22 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| H10 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| H11 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| H12 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| H13 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| H14 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| J10 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| J11 | GND | - 1 | - | - | GND | - | - | - | GND | - | - | - |
| J12 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| J13 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| J14 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| J9 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| K10 | GND | - | - | - | GND | - | - | - | GND | - | - | - |
| L | | 1 | I | 1 | | | L | | | 1 | L | 1 |

| | | | `` | , | | | |
|-----------------|------|--------------|-------|---------|------|-------|------|
| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
| LFXP10C-3FN388I | 244 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | IND | 9.7K |
| LFXP10C-4FN388I | 244 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | IND | 9.7K |
| LFXP10C-3FN256I | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | IND | 9.7K |
| LFXP10C-4FN256I | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | IND | 9.7K |

Industrial (Cont.)

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|-----------------|------|--------------|-------|---------|------|-------|-------|
| LFXP15C-3FN484I | 300 | 1.8/2.5/3.3V | -3 | fpBGA | 484 | IND | 15.5K |
| LFXP15C-4FN484I | 300 | 1.8/2.5/3.3V | -4 | fpBGA | 484 | IND | 15.5K |
| LFXP15C-3FN388I | 268 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | IND | 15.5K |
| LFXP15C-4FN388I | 268 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | IND | 15.5K |
| LFXP15C-3FN256I | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | IND | 15.5K |
| LFXP15C-4FN256I | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | IND | 15.5K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|-----------------|------|--------------|-------|---------|------|-------|-------|
| LFXP20C-3FN484I | 340 | 1.8/2.5/3.3V | -3 | fpBGA | 484 | IND | 19.7K |
| LFXP20C-4FN484I | 340 | 1.8/2.5/3.3V | -4 | fpBGA | 484 | IND | 19.7K |
| LFXP20C-3FN388I | 268 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | IND | 19.7K |
| LFXP20C-4FN388I | 268 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | IND | 19.7K |
| LFXP20C-3FN256I | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | IND | 19.7K |
| LFXP20C-4FN256I | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | IND | 19.7K |

| Part Number | l/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|----------------|------|---------|-------|---------|------|-------|------|
| LFXP3E-3QN208I | 136 | 1.2V | -3 | PQFP | 208 | IND | 3.1K |
| LFXP3E-4QN208I | 136 | 1.2V | -4 | PQFP | 208 | IND | 3.1K |
| LFXP3E-3TN144I | 100 | 1.2V | -3 | TQFP | 144 | IND | 3.1K |
| LFXP3E-4TN144I | 100 | 1.2V | -4 | TQFP | 144 | IND | 3.1K |
| LFXP3E-3TN100I | 62 | 1.2V | -3 | TQFP | 100 | IND | 3.1K |
| LFXP3E-4TN100I | 62 | 1.2V | -4 | TQFP | 100 | IND | 3.1K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|----------------|------|---------|-------|---------|------|-------|------|
| LFXP6E-3FN256I | 188 | 1.2V | -3 | fpBGA | 256 | IND | 5.8K |
| LFXP6E-4FN256I | 188 | 1.2V | -4 | fpBGA | 256 | IND | 5.8K |
| LFXP6E-3QN208I | 142 | 1.2V | -3 | PQFP | 208 | IND | 5.8K |
| LFXP6E-4QN208I | 142 | 1.2V | -4 | PQFP | 208 | IND | 5.8K |
| LFXP6E-3TN144I | 100 | 1.2V | -3 | TQFP | 144 | IND | 5.8K |
| LFXP6E-4TN144I | 100 | 1.2V | -4 | TQFP | 144 | IND | 5.8K |



LatticeXP Family Data Sheet Revision History

November 2007

Revision History

Data Sheet DS1001

| Date | Version | Section | Change Summary |
|----------------|---------|-------------------------------------|--|
| February 2005 | 01.0 | _ | Initial release. |
| April 2005 | 01.1 | Architecture | EBR memory support section updated with clarification. |
| May 2005 | 01.2 | Introduction | Added TransFR Reconfiguration to Features section. |
| | | Architecture | Added TransFR section. |
| June 2005 | 01.3 | Pinout Information | Added pinout information for LFXP3, LFXP6, LFXP15 and LFXP20. |
| July 2005 | 02.0 | Introduction | Updated XP6, XP15 and XP20 EBR SRAM Bits and Block numbers. |
| | | Architecture | Updated Per Quadrant Primary Clock Selection figure. |
| | | | Added Typical I/O Behavior During Power-up section. |
| | | | Updated Device Configuration section under Configuration and Testing. |
| | | DC and Switching | Clarified Hot Socketing Specification |
| | | Characteristics | Updated Supply Current (Standby) Table |
| | | | Updated Initialization Supply Current Table |
| | | | Added Programming and Erase Flash Supply Current table |
| | | | Added LVDS Emulation section. Updated LVDS25E Output Termination Example figure and LVDS25E DC Conditions table. |
| | | | Updated Differential LVPECL diagram and LVPECL DC Conditions table. |
| | | | Deleted 5V Tolerant Input Buffer section. Updated RSDS figure and RSDS DC Conditions table. |
| | | | Updated sysCONFIG Port Timing Specifications |
| | | | Updated JTAG Port Timing Specifications. Added Flash Download Time table. |
| | | Pinout Information | Updated Signal Descriptions table. |
| | | | Updated Logic Signal Connections Dual Function column. |
| | | Ordering Information | Added lead-free ordering part numbers. |
| July 2005 | 02.1 | DC and Switching Characteristics | Clarification of Flash Programming Junction Temperature |
| August 2005 | 02.2 | Introduction | Added Sleep Mode feature. |
| | | Architecture | Added Sleep Mode section. |
| | | DC and Switching | Added Sleep Mode Supply Current Table |
| | | Characteristics | Added Sleep Mode Timing section |
| | | Pinout Information | Added SLEEPN and TOE signal names, descriptions and footnotes. |
| | | | Added SLEEPN and TOE to pinout information and footnotes. |
| | | | Added footnote 3 to Logic Signal Connections tables for clarification on emulated LVDS output. |
| September 2005 | 03.0 | Architecture | Added clarification of PCI clamp. |
| | | | Added clarification to SLEEPN Pin Characteristics section. |
| | | DC and Switching Characteristics | DC Characteristics, added footnote 4 for clarification. Updated Supply Current (Sleep Mode), Supply Current (Standby), Initialization Supply Current, and Programming and Erase Flash Supply Current typical numbers. |

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| Date | Version | Section | Change Summary |
|---------------------------|-----------------|---|---|
| September 2005 (cont.) | 03.0 (cont.) | DC and Switching Characteristics (cont.) | Updated Typical Building Block Function Performance timing numbers. |
| | | | Updated External Switching Characteristics timing numbers. |
| | | | Updated Internal Timing Parameters. |
| | | | Updated LatticeXP Family timing adders. |
| | | | Updated LatticeXP "C" Sleep Mode timing numbers. |
| | | | Updated JTAG Port Timing numbers. |
| | | Pinout Information | Added clarification to SLEEPN and TOE description. |
| | | | Clarification of dedicated LVDS outputs. |
| | | Supplemental Information | Updated list of technical notes. |
| September 2005 | 03.1 | Pinout Information | Power Supply and NC Connections table corrected VCCP1 pin number for 208 PQFP. |
| December 2005 | 04.0 | Introduction | Moved data sheet from Advance to Final. |
| | | Architecture | Added clarification to Typical I/O Behavior During Power-up section. |
| | | DC and Switching Characteristics | Added clarification to Recommended Operating Conditions. |
| | | | Updated timing numbers. |
| | | Pinout Information | Updated Signal Descriptions table. |
| | | | Added clarification to Differential I/O Per Bank. |
| | | | Updated Differential dedicated LVDS output support. |
| | | Ordering Information | Added 208 PQFP lead-free package and ordering part numbers. |
| February 2006 | 04.1 | Pinout Information | Corrected description of Signal Names VREF1(x) and VREF2(x). |
| March 2006 | 04.2 | DC and Switching Characteristics | Corrected condition for IIL and IIH. |
| March 2006 | 04.3 | DC and Switching Characteristics | Added clarification to Recommended Operating Conditions for VCCAUX. |
| April 2006 | 04.4 | Pinout Information | Removed Bank designator "5" from SLEEPN/TOE ball function. |
| May 2006 | 04.5 | DC and Switching Characteristics | Added footnote 2 regarding threshold level for PROGRAMN to sysCON- FIG Port Timing Specifications table. |
| June 2006 | 04.6 | DC and Switching Characteristics | Corrected LVDS25E Output Termination Example. |
| August 2006 | 04.7 | Architecture | Added clarification to Typical I/O Behavior During Power-Up section. |
| | | | Added clarification to Left and Right sysIO Buffer Pair section. |
| | | DC and Switching Characteristics | Changes to LVDS25E Output Termination Example diagram. |
| December 2006 | 04.8 | Architecture | EBR Asynchronous Reset section added. |
| February 2007 | 04.9 | Architecture | Updated EBR Asynchronous Reset section. |
| July 2007 | 05.0 | Introduction | Updated LatticeXP Family Selection Guide table. |
| | | Architecture | Updated Typical I/O Behavior During Power-up text section. |
| | | DC and Switching Characteristics | Updated sysIO Single-Ended DC Electrical Characteristics table. Split out LVCMOS 1.2 by supply voltage. |
| November 2007 | 05.1 | DC and Switching Characteristics | Added JTAG Port Timing Waveforms diagram. |
| | | Pinout Information | Added Thermal Management text section. |
| | | Supplemental Information | Updated title list. |