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## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

### Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15000
Total RAM Bits	331776
Number of I/O	188
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp15c-3fn256i">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp15c-3fn256i</a>

## Features

### ■ Non-volatile, Infinitely Reconfigurable

- Instant-on – powers up in microseconds
- No external configuration memory
- Excellent design security, no bit stream to intercept
- Reconfigure SRAM based logic in milliseconds
- SRAM and non-volatile memory programmable through system configuration and JTAG ports

### ■ Sleep Mode

- Allows up to 1000x static current reduction

### ■ TransFR™ Reconfiguration (TFR)

- In-field logic update while system operates

### ■ Extensive Density and Package Options

- 3.1K to 19.7K LUT4s
- 62 to 340 I/Os
- Density migration supported

### ■ Embedded and Distributed Memory

- 54 Kbits to 396 Kbits sysMEM™ Embedded Block RAM
- Up to 79 Kbits distributed RAM
- Flexible memory resources:
  - Distributed and block memory

### ■ Flexible I/O Buffer

- Programmable sysIO™ buffer supports wide range of interfaces:
  - LVCMOS 3.3/2.5/1.8/1.5/1.2
  - LVTTTL
  - SSTL 18 Class I
  - SSTL 3/2 Class I, II
  - HSTL15 Class I, III
  - HSTL 18 Class I, II, III
  - PCI
  - LVDS, Bus-LVDS, LVPECL, RSDS

### ■ Dedicated DDR Memory Support

- Implements interface up to DDR333 (166MHz)

### ■ sysCLOCK™ PLLs

- Up to 4 analog PLLs per device
- Clock multiply, divide and phase shifting

### ■ System Level Support

- IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
- Onboard oscillator for configuration
- Devices operate with 3.3V, 2.5V, 1.8V or 1.2V power supply

**Table 1-1. LatticeXP Family Selection Guide**

Device	LFXP3	LFXP6	LFXP10	LFXP15	LFXP20
PFU/PFF Rows	16	24	32	40	44
PFU/PFF Columns	24	30	38	48	56
PFU/PFF (Total)	384	720	1216	1932	2464
LUTs (K)	3	6	10	15	20
Distributed RAM (KBits)	12	23	39	61	79
EBR SRAM (KBits)	54	72	216	324	396
EBR SRAM Blocks	6	8	24	36	44
V <sub>CC</sub> Voltage	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V
PLLs	2	2	4	4	4
Max. I/O	136	188	244	300	340
<b>Packages and I/O Combinations:</b>					
100-pin TQFP (14 x 14 mm)	62				
144-pin TQFP (20 x 20 mm)	100	100			
208-pin PQFP (28 x 28 mm)	136	142			
256-ball fpBGA (17 x 17 mm)		188	188	188	188
388-ball fpBGA (23 x 23 mm)			244	268	268
484-ball fpBGA (23 x 23 mm)				300	340

Figure 2-10. PLL Diagram

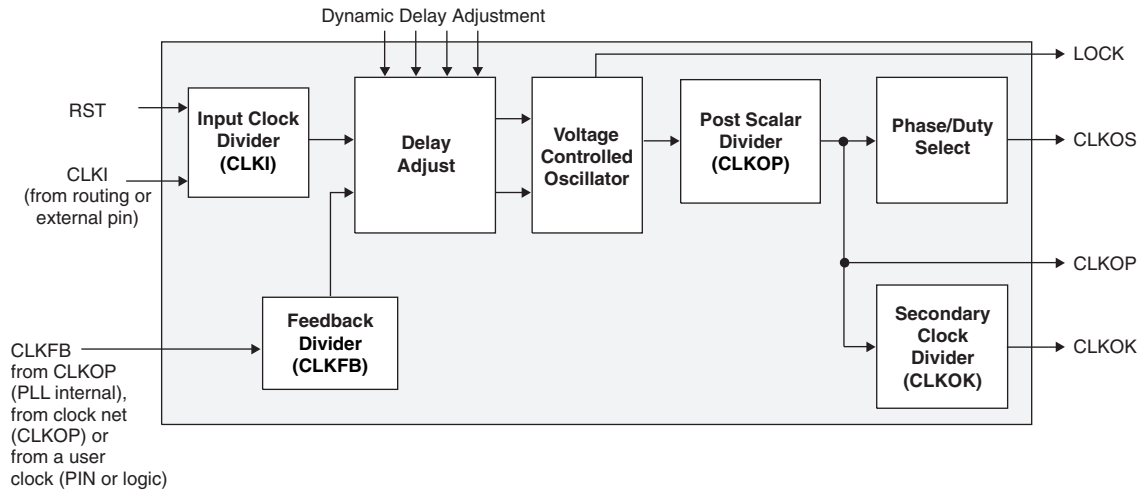


Figure 2-11 shows the available macros for the PLL. Table 2-11 provides signal description of the PLL Block.

Figure 2-11. PLL Primitive

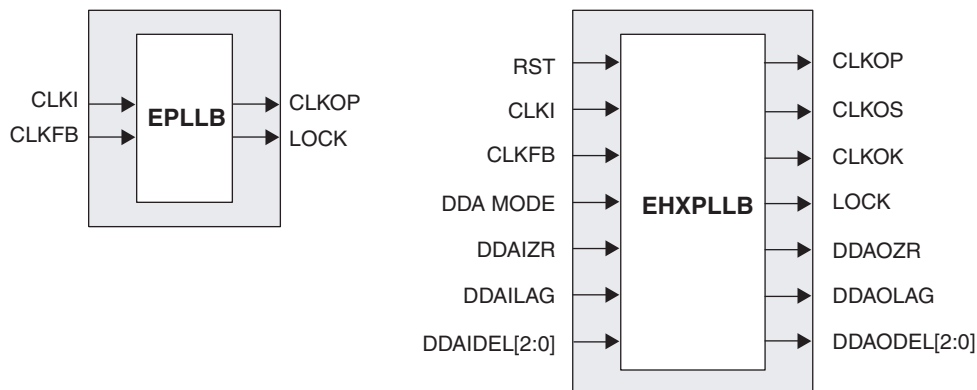


Table 2-5. PLL Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)
RST	I	“1” to reset input clock divider
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (No phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
LOCK	O	“1” indicates PLL LOCK to CLKI
DDAMODE	I	Dynamic Delay Enable. “1” Pin control (dynamic), “0”: Fuse Control (static)
DDAIZR	I	Dynamic Delay Zero. “1”: delay = 0, “0”: delay = on
DDAILAG	I	Dynamic Delay Lag/Lead. “1”: Lag, “0”: Lead
DDAIDEL[2:0]	I	Dynamic Delay Input
DDAOZR	O	Dynamic Delay Zero Output
DDAOLAG	O	Dynamic Delay Lag/Lead Output
DDAODEL[2:0]	O	Dynamic Delay Output

in selected blocks the input to the DQS delay block. If one of the bypass options is not chosen, the signal first passes through an optional delay block. This delay, if selected, ensures no positive input-register hold-time requirement when using a global clock.

The input block allows two modes of operation. In the single data rate (SDR) the data is registered, by one of the registers in the single data rate sync register block, with the system clock. In the DDR Mode two registers are used to sample the data on the positive and negative edges of the DQS signal creating two data streams, D0 and D2. These two data streams are synchronized with the system clock before entering the core. Further discussion on this topic is in the DDR Memory section of this data sheet.

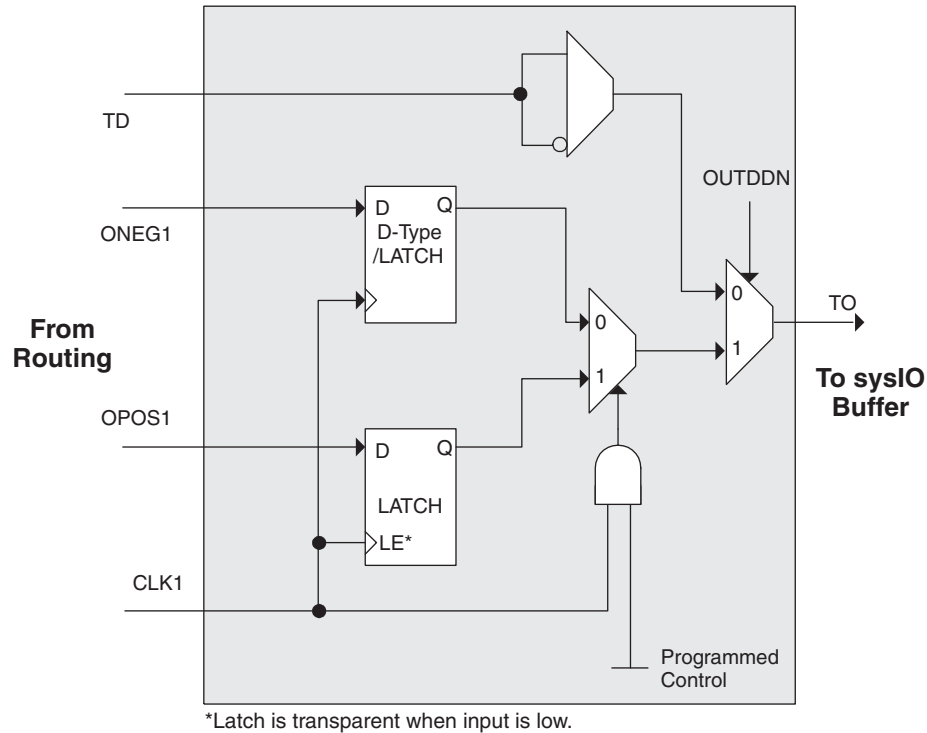
Figure 2-21 shows the input register waveforms for DDR operation and Figure 2-22 shows the design tool primitives. The SDR/SYNC registers have reset and clock enable available.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to the system clock domain. For further discussion of this topic, see the DDR memory section of this data sheet.

**Figure 2-20. Input Register Diagram**



Figure 2-25. Tristate Register Block



**Control Logic Block**

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing and a DQS signal provided from the programmable DQS pin. The clock can optionally be inverted.

The clock enable and local reset signals are selected from the routing and optionally inverted. The global tristate signal is passed through this block.

**DDR Memory Support**

Implementing high performance DDR memory interfaces requires dedicated DDR register structures in the input (for read operations) and in the output (for write operations). As indicated in the PIO Logic section, the LatticeXP devices provide this capability. In addition to these registers, the LatticeXP devices contain two elements to simplify the design of input structures for read operations: the DQS delay block and polarity control logic.

**DLL Calibrated DQS Delay Block**

Source Synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment, however in DDR memories the clock (referred to as DQS) is not free running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds the polarity control logic which controls the polarity of the clock to the sync registers in the input register blocks. Figures 2-26 and 2-27 show how the polarity control logic are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two DLLs on opposite sides of the device. Each DLL compensates DQS Delays in its half of the device as shown in Figure 2-27. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

## DC Electrical Characteristics

### Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{IL}, I_{IH}^{1,2,4}$	Input or I/O Leakage	$0 \leq V_{IN} \leq (V_{CCIO} - 0.2V)$	—	—	10	$\mu A$
		$(V_{CCIO} - 0.2V) < V_{IN} \leq 3.6V$	—	—	40	$\mu A$
$I_{PU}$	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7 V_{CCIO}$	-30	—	-150	$\mu A$
$I_{PD}$	I/O Active Pull-down Current	$V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MAX)$	30	—	150	$\mu A$
$I_{BHLS}$	Bus Hold Low sustaining current	$V_{IN} = V_{IL} (MAX)$	30	—	—	$\mu A$
$I_{BHHS}$	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	-30	—	—	$\mu A$
$I_{BHLO}$	Bus Hold Low Overdrive current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	150	$\mu A$
$I_{BHHO}$	Bus Hold High Overdrive current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	-150	$\mu A$
$V_{BHT}$	Bus Hold trip Points	$0 \leq V_{IN} \leq V_{IH} (MAX)$	$V_{IL} (MAX)$	—	$V_{IH} (MIN)$	V
C1	I/O Capacitance <sup>3</sup>	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,$ $V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—	8	—	pf
C2	Dedicated Input Capacitance <sup>3</sup>	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,$ $V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—	8	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. Not applicable to SLEEPN/TOE pin.
3.  $T_A = 25^\circ C, f = 1.0MHz$
4. When  $V_{IH}$  is higher than  $V_{CCIO}$ , a transient current typically of 30ns in duration or less with a peak current of 6mA can be expected on the high-to-low transition.

## Supply Current (Sleep Mode)<sup>1, 2, 3</sup>

Symbol	Parameter	Device	Typ. <sup>4</sup>	Max	Units
$I_{CC}$	Core Power Supply	LFXP3C	12	65	$\mu A$
		LFXP6C	14	75	$\mu A$
		LFXP10C	16	85	$\mu A$
		LFXP15C	18	95	$\mu A$
		LFXP20C	20	105	$\mu A$
$I_{CCP}$	PLL Power Supply (per PLL)	All LFXP 'C' Devices	1	5	$\mu A$
$I_{CCAUX}$	Auxiliary Power Supply	LFXP3C	2	90	$\mu A$
		LFXP6C	2	100	$\mu A$
		LFXP10C	2	110	$\mu A$
		LFXP15C	3	120	$\mu A$
		LFXP20C	4	130	$\mu A$
$I_{CCIO}$	Bank Power Supply <sup>5</sup>	LFXP3C	2	20	$\mu A$
		LFXP6C	2	22	$\mu A$
		LFXP10C	2	24	$\mu A$
		LFXP15C	3	27	$\mu A$
		LFXP20C	4	30	$\mu A$
$I_{CCJ}$	VCCJ Power Supply	All LFXP 'C' Devices	1	5	$\mu A$

1. Assumes all inputs are configured as LVCMOS and held at the VCCIO or GND.
2. Frequency 0MHz.
3. User pattern: blank.
4.  $T_A = 25^\circ C$ , power supplies at nominal voltage.
5. Per bank.

Figure 3-2. BLVDS Multi-point Output Example

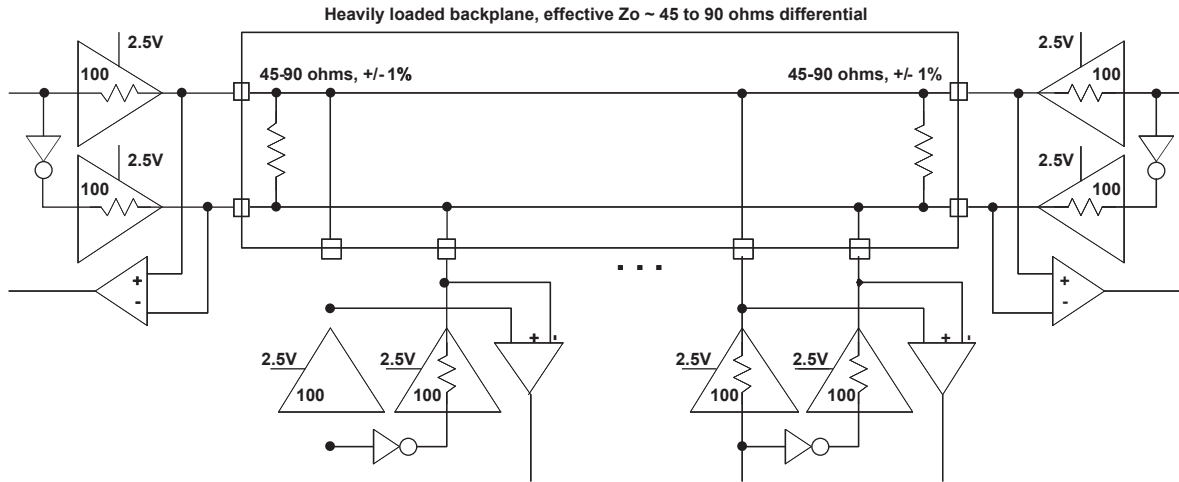


Table 3-2. BLVDS DC Conditions<sup>1</sup>

Over Recommended Operating Conditions

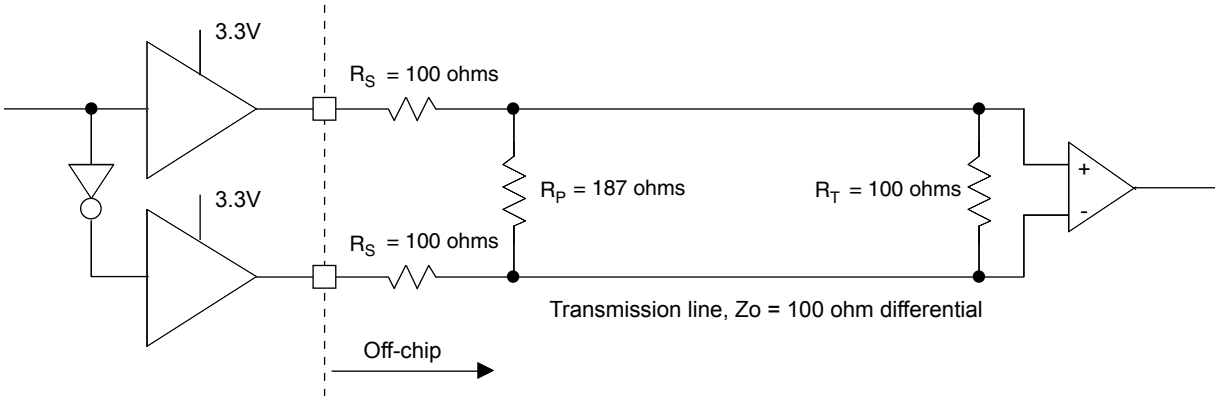
Symbol	Description	Typical		Units
		$Z_o = 45$	$Z_o = 90$	
$Z_{OUT}$	Output impedance	100	100	ohms
$R_{TLEFT}$	Left end termination	45	90	ohms
$R_{TRIGHT}$	Right end termination	45	90	ohms
$V_{OH}$	Output high voltage	1.375	1.48	V
$V_{OL}$	Output low voltage	1.125	1.02	V
$V_{OD}$	Output differential voltage	0.25	0.46	V
$V_{CM}$	Output common mode voltage	1.25	1.25	V
$I_{DC}$	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

**LVPECL**

The LatticeXP devices support differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

**Figure 3-3. Differential LVPECL**



**Table 3-3. LVPECL DC Conditions<sup>1</sup>**

**Over Recommended Operating Conditions**

Symbol	Description	Typical	Units
$Z_{OUT}$	Output impedance	100	ohms
$R_P$	Driver parallel resistor	187	ohms
$R_S$	Driver series resistor	100	ohms
$R_T$	Receiver termination	100	ohms
$V_{OH}$	Output high voltage	2.03	V
$V_{OL}$	Output low voltage	1.27	V
$V_{OD}$	Output differential voltage	0.76	V
$V_{CM}$	Output common mode voltage	1.65	V
$Z_{BACK}$	Back impedance	85.7	ohms
$I_{DC}$	DC output current	12.7	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

**RSDS**

The LatticeXP devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.



Figure 3-4. RSDS (Reduced Swing Differential Standard)

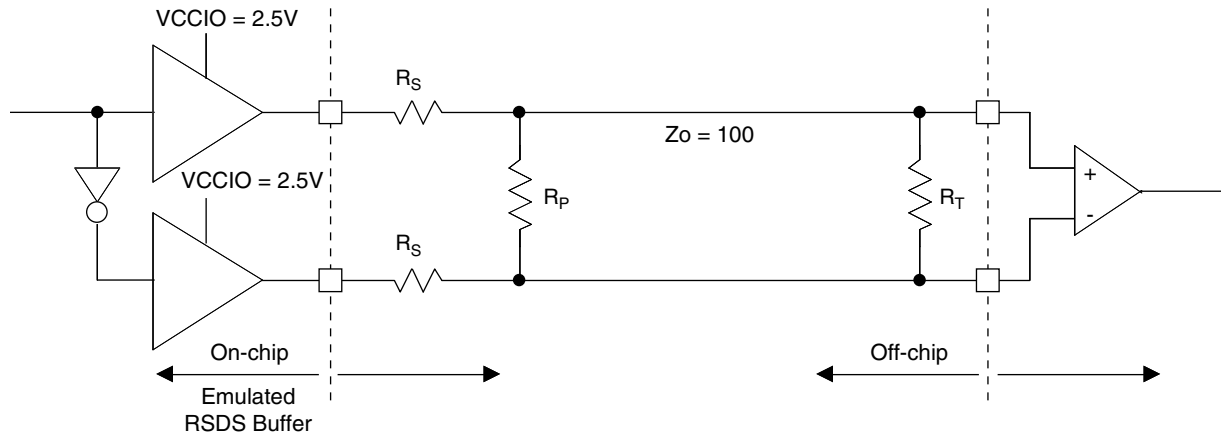


Table 3-4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z <sub>OUT</sub>	Output impedance	20	ohms
R <sub>S</sub>	Driver series resistor	300	ohms
R <sub>P</sub>	Driver parallel resistor	121	ohms
R <sub>T</sub>	Receiver termination	100	ohms
V <sub>OH</sub>	Output high voltage	1.35	V
V <sub>OL</sub>	Output low voltage	1.15	V
V <sub>OD</sub>	Output differential voltage	0.20	V
V <sub>CM</sub>	Output common mode voltage	1.25	V
Z <sub>BACK</sub>	Back impedance	101.5	ohms
I <sub>DC</sub>	DC output current	3.66	mA

LatticeXP Internal Timing Parameters<sup>1</sup>

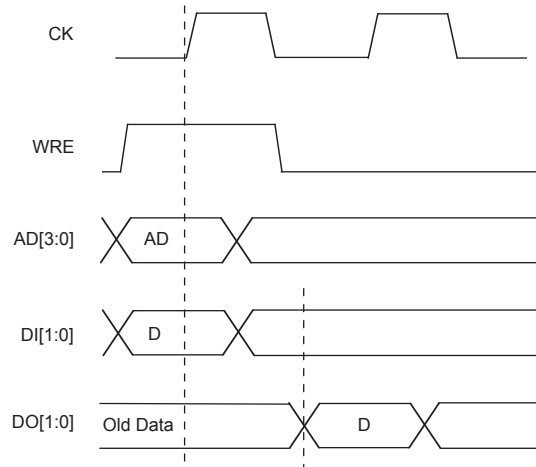
Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>PFU/PFF Logic Mode Timing</b>								
t <sub>LUT4_PFU</sub>	LUT4 Delay (A to D Inputs to F Output)	—	0.28	—	0.34	—	0.40	ns
t <sub>LUT6_PFU</sub>	LUT6 Delay (A to D Inputs to OFX Output)	—	0.44	—	0.53	—	0.63	ns
t <sub>LSR_PFU</sub>	Set/Reset to Output of PFU	—	0.90	—	1.08	—	1.29	ns
t <sub>SUM_PFU</sub>	Clock to Mux (M0,M1) Input Setup Time	0.13	—	0.15	—	0.19	—	ns
t <sub>HM_PFU</sub>	Clock to Mux (M0,M1) Input Hold Time	-0.04	—	-0.03	—	-0.03	—	ns
t <sub>SUD_PFU</sub>	Clock to D Input Setup Time	0.13	—	0.16	—	0.19	—	ns
t <sub>HD_PFU</sub>	Clock to D Input Hold Time	-0.03	—	-0.02	—	-0.02	—	ns
t <sub>CK2Q_PFU</sub>	Clock to Q Delay, D-type Register Configuration	—	0.40	—	0.48	—	0.58	ns
t <sub>LE2Q_PFU</sub>	Clock to Q Delay Latch Configuration	—	0.53	—	0.64	—	0.76	ns
t <sub>LD2Q_PFU</sub>	D to Q Throughput Delay when Latch is Enabled	—	0.55	—	0.66	—	0.79	ns
<b>PFU Dual Port Memory Mode Timing</b>								
t <sub>CORAM_PFU</sub>	Clock to Output	—	0.40	—	0.48	—	0.58	ns
t <sub>SUDATA_PFU</sub>	Data Setup Time	-0.18	—	-0.14	—	-0.11	—	ns
t <sub>HDATA_PFU</sub>	Data Hold Time	0.28	—	0.34	—	0.40	—	ns
t <sub>SUADDR_PFU</sub>	Address Setup Time	-0.46	—	-0.37	—	-0.30	—	ns
t <sub>HADDR_PFU</sub>	Address Hold Time	0.71	—	0.85	—	1.02	—	ns
t <sub>SUWREN_PFU</sub>	Write/Read Enable Setup Time	-0.22	—	-0.17	—	-0.14	—	ns
t <sub>HWREN_PFU</sub>	Write/Read Enable Hold Time	0.33	—	0.40	—	0.48	—	ns
<b>PIC Timing</b>								
<b>PIO Input/Output Buffer Timing</b>								
t <sub>IN_PIO</sub>	Input Buffer Delay	—	0.62	—	0.72	—	0.85	ns
t <sub>OUT_PIO</sub>	Output Buffer Delay	—	2.12	—	2.54	—	3.05	ns
<b>IOLOGIC Input/Output Timing</b>								
t <sub>SUI_PIO</sub>	Input Register Setup Time (Data Before Clock)	1.35	—	1.83	—	2.37	—	ns
t <sub>HI_PIO</sub>	Input Register Hold Time (Data After Clock)	0.05	—	0.05	—	0.05	—	ns
t <sub>COO_PIO</sub>	Output Register Clock to Output Delay	—	0.36	—	0.44	—	0.52	ns
t <sub>SUCE_PIO</sub>	Input Register Clock Enable Setup Time	-0.09	—	-0.07	—	-0.06	—	ns
t <sub>HCE_PIO</sub>	Input Register Clock Enable Hold Time	0.13	—	0.16	—	0.19	—	ns
t <sub>SULSR_PIO</sub>	Set/Reset Setup Time	0.19	—	0.23	—	0.28	—	ns
t <sub>HLSR_PIO</sub>	Set/Reset Hold Time	-0.14	—	-0.11	—	-0.09	—	ns
<b>EBR Timing</b>								
t <sub>CO_EBR</sub>	Clock to Output from Address or Data	—	4.01	—	4.81	—	5.78	ns
t <sub>COO_EBR</sub>	Clock to Output from EBR Output Register	—	0.81	—	0.97	—	1.17	ns
t <sub>SUDATA_EBR</sub>	Setup Data to EBR Memory	-0.26	—	-0.21	—	-0.17	—	ns
t <sub>HDATA_EBR</sub>	Hold Data to EBR Memory	0.41	—	0.49	—	0.59	—	ns
t <sub>SUADDR_EBR</sub>	Setup Address to EBR Memory	-0.26	—	-0.21	—	-0.17	—	ns
t <sub>HADDR_EBR</sub>	Hold Address to EBR Memory	0.41	—	0.49	—	0.59	—	ns
t <sub>SUWREN_EBR</sub>	Setup Write/Read Enable to EBR Memory	-0.17	—	-0.13	—	-0.11	—	ns
t <sub>HWREN_EBR</sub>	Hold Write/Read Enable to EBR Memory	0.26	—	0.31	—	0.37	—	ns
t <sub>SUCE_EBR</sub>	Clock Enable Setup Time to EBR Output Register	0.19	—	0.23	—	0.28	—	ns
t <sub>HCE_EBR</sub>	Clock Enable Hold Time to EBR Output Register	-0.13	—	-0.10	—	-0.08	—	ns

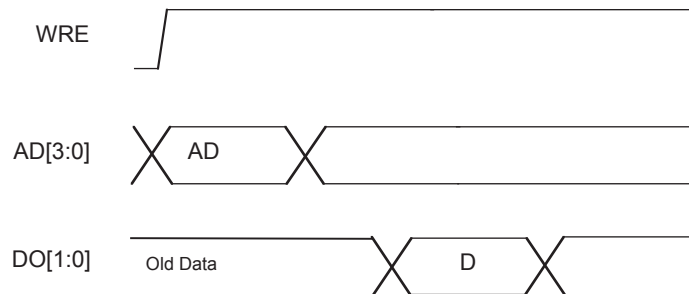
## Timing Diagrams

### PFU Timing Diagrams

**Figure 3-6. Slice Single/Dual Port Write Cycle Timing**



**Figure 3-7. Slice Single /Dual Port Read Cycle Timing**



**PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin**

PICs Associated with DQS Strobe	PIO within PIC	Polarity	DDR Strobe (DQS) and Data (DQ) Pins
P[Edge] [n-4]	A	True	DQ
	B	Complement	DQ
P[Edge] [n-3]	A	True	DQ
	B	Complement	DQ
P[Edge] [n-2]	A	True	DQ
	B	Complement	DQ
P[Edge] [n-1]	A	True	DQ
P[Edge] [n]			
	B	Complement	DQ
P[Edge] [n+1]	A	True	[Edge]DQSn
	B	Complement	DQ
P[Edge] [n+2]	A	True	DQ
	B	Complement	DQ
P[Edge] [n+3]	A	True	DQ
	B	Complement	DQ

Notes:

1. "n" is a row/column PIC number.
2. The DDR interface is designed for memories that support one DQS strobe per eight bits of data. In some packages, all the potential DDR data (DQ) pins may not be available.
3. The definition of the PIC numbering is provided in the Signal Names column of the Signal Descriptions table in this data sheet.

**Pin Information Summary<sup>1</sup> (Cont.)**

Pin Type		XP10		XP15			XP20		
		256 fpBGA	388 fpBGA	256 fpBGA	388 fpBGA	484 fpBGA	256 fpBGA	388 fpBGA	484 fpBGA
Single Ended User I/O		188	244	188	268	300	188	268	340
Differential Pair User I/O <sup>2</sup>		76	104	76	112	128	76	112	144
Configuration	Dedicated	11	11	11	11	11	11	11	11
	Muxed	14	14	14	14	14	14	14	14
TAP		5	5	5	5	5	5	5	5
Dedicated (total without supplies)		6	6	6	6	6	6	6	6
V <sub>CC</sub>		8	14	8	14	28	8	14	28
V <sub>CCAUX</sub>		4	4	4	4	12	4	4	12
V <sub>CCPLL</sub>		2	2	2	2	2	2	2	2
V <sub>CCIO</sub>	Bank0	2	5	2	5	4	2	5	4
	Bank1	2	5	2	5	4	2	5	4
	Bank2	2	4	2	4	4	2	4	4
	Bank3	2	4	2	4	4	2	4	4
	Bank4	2	5	2	5	4	2	5	4
	Bank5	2	5	2	5	4	2	5	4
	Bank6	2	4	2	4	4	2	4	4
	Bank7	2	4	2	4	4	2	4	4
GND		24	50	24	50	56	24	50	56
GND <sub>PLL</sub>		2	2	2	2	2	2	2	2
NC		0	24	0	0	40	0	0	0
Single Ended/ Differential I/O per Bank <sup>2</sup>	Bank0	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank1	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank2	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank3	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank4	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank5	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank6	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank7	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
V <sub>CCJ</sub>		1	1	1	1	1	1	1	1

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
2. The differential I/O per bank includes both dedicated LVDS and emulated LVDS pin pairs. Please see the Logic Signal Connections table for more information.

**LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)**

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
93	PB19B	4	C	VREF1_4	PB22B	4	C	VREF1_4
94	PB20A	4	T	-	PB23A	4	T	-
95	PB20B	4	C	-	PB23B	4	C	-
96	PB21A	4	T	-	PB24A	4	T	-
97	VCCIO4	4	-	-	VCCIO4	4	-	-
98	PB21B	4	C	-	PB24B	4	C	-
99	PB22A	4	T	-	PB25A	4	T	-
100	PB22B	4	C	-	PB25B	4	C	-
101	PB23A	4	T	-	PB26A	4	T	-
102	PB23B	4	C	-	PB26B	4	C	-
103	PB24A	4	T	VREF2_4	PB27A	4	-	VREF2_4
104	PB24B	4	C	-	PB30A	4	T	DQS
105	PB25A	4	-	-	PB30B	4	C	-
106	GND	-	-	-	GND	-	-	-
107	VCC	-	-	-	VCC	-	-	-
108	PR18B	3	C <sup>3</sup>	-	PR26B	3	C <sup>3</sup>	-
109	GNDIO3	3	-	-	GNDIO3	3	-	-
110	PR18A	3	T <sup>3</sup>	-	PR26A	3	T <sup>3</sup>	-
111	PR17B	3	C	-	PR25B	3	C	-
112	PR17A	3	T	-	PR25A	3	T	-
113	PR16B	3	C <sup>3</sup>	-	PR24B	3	C <sup>3</sup>	-
114	PR16A	3	T <sup>3</sup>	DQS	PR24A	3	T <sup>3</sup>	DQS
115	VCCIO3	3	-	-	VCCIO3	3	-	-
116	PR15B	3	-	VREF1_3	PR23B	3	-	VREF1_3
117	PR14A	3	-	VREF2_3	PR22A	3	-	VREF2_3
118	GNDIO3	3	-	-	GNDIO3	3	-	-
119	PR13B	3	C	-	PR21B	3	C <sup>3</sup>	-
120	PR13A	3	T	-	PR21A	3	T <sup>3</sup>	-
121	GND	-	-	-	GND	-	-	-
122	PR12B	3	C	-	PR20B	3	C	-
123	PR12A	3	T	-	PR20A	3	T	-
124	PR11B	3	C	-	PR19B	3	C <sup>3</sup>	-
125	VCCIO3	3	-	-	VCCIO3	3	-	-
126	PR11A	3	T	-	PR19A	3	T <sup>3</sup>	-
127	GNDP1	-	-	-	GNDP1	-	-	-
128	VCCP1	-	-	-	VCCP1	-	-	-
129	NC	-	-	-	PR13A	2	-	-
130	GND	-	-	-	GND	-	-	-
131	PR9B	2	C	PCLKC2_0	PR12B	2	C	PCLKC2_0
132	PR9A	2	T	PCLKT2_0	PR12A	2	T	PCLKT2_0
133	NC	-	-	-	PR11B	2	C <sup>3</sup>	-
134	NC	-	-	-	PR11A	2	T <sup>3</sup>	-
135	GNDIO2	2	-	-	GNDIO2	2	-	-
136	PR8B	2	C	RUM0_PLLC_IN_A	PR8B	2	C	RUM0_PLLC_IN_A
137	PR8A	2	T	RUM0_PLLT_IN_A	PR8A	2	T	RUM0_PLLT_IN_A
138	PR7B	2	C <sup>3</sup>	-	PR7B	2	C <sup>3</sup>	-

**LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)**

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
139	PR7A	2	T <sup>3</sup>	DQS	PR7A	2	T <sup>3</sup>	DQS
140	VCCIO2	2	-	-	VCCIO2	2	-	-
141	PR6B	2	-	VREF1_2	PR6B	2	-	VREF1_2
142	PR5A	2	-	VREF2_2	PR5A	2	-	VREF2_2
143	GNDIO2	2	-	-	GNDIO2	2	-	-
144	PR4B	2	C <sup>3</sup>	-	PR4B	2	C <sup>3</sup>	-
145	PR4A	2	T <sup>3</sup>	-	PR4A	2	T <sup>3</sup>	-
146	PR3B	2	C	RUM0_PLLC_FB_A	PR3B	2	C	RUM0_PLLC_FB_A
147	PR3A	2	T	RUM0_PLLT_FB_A	PR3A	2	T	RUM0_PLLT_FB_A
148	PR2B	2	C <sup>3</sup>	-	PR2B	2	C <sup>3</sup>	-
149	VCCIO2	2	-	-	VCCIO2	2	-	-
150	PR2A	2	T <sup>3</sup>	-	PR2A	2	T <sup>3</sup>	-
151	VCC	-	-	-	VCC	-	-	-
152	VCCAUX	-	-	-	VCCAUX	-	-	-
153	TDO	-	-	-	TDO	-	-	-
154	VCCJ	-	-	-	VCCJ	-	-	-
155	TDI	-	-	-	TDI	-	-	-
156	TMS	-	-	-	TMS	-	-	-
157	TCK	-	-	-	TCK	-	-	-
158	VCC	-	-	-	VCC	-	-	-
159	PT25A	1	-	VREF1_1	PT28A	1	-	VREF1_1
160	PT24B	1	C	-	PT27B	1	C	-
161	PT24A	1	T	-	PT27A	1	T	-
162	PT23A	1	-	D0	PT26A	1	-	D0
163	GNDIO1	1	-	-	GNDIO1	1	-	-
164	PT22B	1	C	D1	PT25B	1	C	D1
165	PT22A	1	T	VREF2_1	PT25A	1	T	VREF2_1
166	PT21A	1	-	D2	PT24A	1	-	D2
167	VCCIO1	1	-	-	VCCIO1	1	-	-
168	PT20B	1	C	D3	PT23B	1	C	D3
169	PT20A	1	T	-	PT23A	1	T	-
170	PT19B	1	C	-	PT22B	1	C	-
171	PT19A	1	T	DQS	PT22A	1	T	DQS
172	GNDIO1	1	-	-	GNDIO1	1	-	-
173	PT18B	1	-	-	PT21B	1	-	-
174	PT17A	1	-	D4	PT20A	1	-	D4
175	PT16B	1	C	-	PT19B	1	C	-
176	PT16A	1	T	D5	PT19A	1	T	D5
177	VCCIO1	1	-	-	VCCIO1	1	-	-
178	PT15B	1	C	D6	PT18B	1	C	D6
179	PT15A	1	T	-	PT18A	1	T	-
180	PT14B	1	-	D7	PT17B	1	-	D7
181	GND	-	-	-	GND	-	-	-
182	VCC	-	-	-	VCC	-	-	-
183	PT13B	0	C	BUSY	PT16B	0	C	BUSY
184	GNDIO0	0	-	-	GNDIO0	0	-	-

**LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA**

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
C2	PROGRAMN	7	-	-	PROGRAMN	7	-	-
C1	CCLK	7	-	-	CCLK	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
D2	PL7A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A
D3	PL7B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A
D1	PL9A	7	-	-	PL9A	7	-	-
E2	PL10B	7	-	VREF1_7	PL10B	7	-	VREF1_7
E1	PL11A	7	T <sup>3</sup>	DQS	PL11A	7	T <sup>3</sup>	DQS
F1	PL11B	7	C <sup>3</sup>	-	PL11B	7	C <sup>3</sup>	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
E3	PL12A	7	T	-	PL12A	7	T	-
F4	PL12B	7	C	-	PL12B	7	C	-
F3	PL13A	7	T <sup>3</sup>	-	PL13A	7	T <sup>3</sup>	-
F2	PL13B	7	C <sup>3</sup>	-	PL13B	7	C <sup>3</sup>	-
G1	PL15B	7	-	-	PL15B	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
G3	PL16A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A
G2	PL16B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A
H1	PL17A	7	T <sup>3</sup>	-	PL17A	7	T <sup>3</sup>	-
H2	PL17B	7	C <sup>3</sup>	-	PL17B	7	C <sup>3</sup>	-
G4	PL18A	7	-	VREF2_7	PL18A	7	-	VREF2_7
G5	PL19B	7	-	-	PL19B	7	-	-
J1	PL20A	7	T <sup>3</sup>	DQS	PL20A	7	T <sup>3</sup>	DQS
-	GNDIO7	7	-	-	GNDIO7	7	-	-
J2	PL20B	7	C <sup>3</sup>	-	PL20B	7	C <sup>3</sup>	-
H3	PL22A	7	T <sup>3</sup>	-	PL22A	7	T <sup>3</sup>	-
J3	PL22B	7	C <sup>3</sup>	-	PL22B	7	C <sup>3</sup>	-
H4	VCCP0	-	-	-	VCCP0	-	-	-
H5	GNDP0	-	-	-	GNDP0	-	-	-
K1	PL24A	6	T	PCLKT6_0	PL28A	6	T	PCLKT6_0
-	GNDIO6	6	-	-	GNDIO6	6	-	-
K2	PL24B	6	C	PCLKC6_0	PL28B	6	C	PCLKC6_0
J4	PL26A	6	-	-	PL30A	6	-	-
J5	PL27B	6	-	VREF1_6	PL31B	6	-	VREF1_6
L1	PL28A	6	T <sup>3</sup>	DQS	PL32A	6	T <sup>3</sup>	DQS
L2	PL28B	6	C <sup>3</sup>	-	PL32B	6	C <sup>3</sup>	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
M1	PL29A	6	T	LLM0_PLLT_IN_A	PL33A	6	T	LLM0_PLLT_IN_A
M2	PL29B	6	C	LLM0_PLLC_IN_A	PL33B	6	C	LLM0_PLLC_IN_A
K3	PL30A	6	T <sup>3</sup>	-	PL34A	6	T <sup>3</sup>	-
L3	PL30B	6	C <sup>3</sup>	-	PL34B	6	C <sup>3</sup>	-



**LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)**

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
G10	GND	-	-	-	GND	-	-	-
G7	GND	-	-	-	GND	-	-	-
G8	GND	-	-	-	GND	-	-	-
G9	GND	-	-	-	GND	-	-	-
H10	GND	-	-	-	GND	-	-	-
H7	GND	-	-	-	GND	-	-	-
H8	GND	-	-	-	GND	-	-	-
H9	GND	-	-	-	GND	-	-	-
J10	GND	-	-	-	GND	-	-	-
J7	GND	-	-	-	GND	-	-	-
J8	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-
K10	GND	-	-	-	GND	-	-	-
K7	GND	-	-	-	GND	-	-	-
K8	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-
L6	GND	-	-	-	GND	-	-	-
T1	GND	-	-	-	GND	-	-	-
T16	GND	-	-	-	GND	-	-	-
D13	VCC	-	-	-	VCC	-	-	-
D4	VCC	-	-	-	VCC	-	-	-
E12	VCC	-	-	-	VCC	-	-	-
E5	VCC	-	-	-	VCC	-	-	-
M12	VCC	-	-	-	VCC	-	-	-
M5	VCC	-	-	-	VCC	-	-	-
N13	VCC	-	-	-	VCC	-	-	-
N4	VCC	-	-	-	VCC	-	-	-
E13	VCCAUX	-	-	-	VCCAUX	-	-	-
E4	VCCAUX	-	-	-	VCCAUX	-	-	-
M13	VCCAUX	-	-	-	VCCAUX	-	-	-
M4	VCCAUX	-	-	-	VCCAUX	-	-	-
F7	VCCIO0	0	-	-	VCCIO0	0	-	-
F8	VCCIO0	0	-	-	VCCIO0	0	-	-
F10	VCCIO1	1	-	-	VCCIO1	1	-	-
F9	VCCIO1	1	-	-	VCCIO1	1	-	-
G11	VCCIO2	2	-	-	VCCIO2	2	-	-
H11	VCCIO2	2	-	-	VCCIO2	2	-	-
J11	VCCIO3	3	-	-	VCCIO3	3	-	-
K11	VCCIO3	3	-	-	VCCIO3	3	-	-
L10	VCCIO4	4	-	-	VCCIO4	4	-	-
L9	VCCIO4	4	-	-	VCCIO4	4	-	-

**LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)**

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
U1	PL25A	6	T	LLM0_PLLT_IN_A	PL29A	6	T	LLM0_PLLT_IN_A	PL33A	6	T	LLM0_PLLT_IN_A
T2	PL25B	6	C	LLM0_PLLC_IN_A	PL29B	6	C	LLM0_PLLC_IN_A	PL33B	6	C	LLM0_PLLC_IN_A
V1	PL26A	6	T <sup>3</sup>	-	PL30A	6	T <sup>3</sup>	-	PL34A	6	T <sup>3</sup>	-
U2	PL26B	6	C <sup>3</sup>	-	PL30B	6	C <sup>3</sup>	-	PL34B	6	C <sup>3</sup>	-
W1	PL28A	6	T <sup>3</sup>	-	PL32A	6	T <sup>3</sup>	-	PL36A	6	T <sup>3</sup>	-
V2	PL28B	6	C <sup>3</sup>	-	PL32B	6	C <sup>3</sup>	-	PL36B	6	C <sup>3</sup>	-
-	GNDIO6	6	-	-	GNDIO6	-	-	-	GNDIO6	6	-	-
P3	PL29A	6	T	-	PL33A	6	T	-	PL37A	6	T	-
P4	PL29B	6	C	-	PL33B	6	C	-	PL37B	6	C	-
Y1	PL30A	6	T <sup>3</sup>	-	PL34A	6	T <sup>3</sup>	-	PL38A	6	T <sup>3</sup>	-
W2	PL30B	6	C <sup>3</sup>	-	PL34B	6	C <sup>3</sup>	-	PL38B	6	C <sup>3</sup>	-
R3	PL31A	6	-	VREF2_6	PL35A	6	-	VREF2_6	PL39A	6	-	VREF2_6
R4	PL32B	6	-	-	PL36B	6	-	-	PL40B	6	-	-
T3	PL33A	6	T <sup>3</sup>	DQS	PL37A	6	T <sup>3</sup>	DQS	PL41A	6	T <sup>3</sup>	DQS
T4	PL33B	6	C <sup>3</sup>	-	PL37B	6	C <sup>3</sup>	-	PL41B	6	C <sup>3</sup>	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
V4	PL34A	6	T	LLM0_PLLT_FB_A	PL38A	6	T	LLM0_PLLT_FB_A	PL42A	6	T	LLM0_PLLT_FB_A
V3	PL34B	6	C	LLM0_PLLC_FB_A	PL38B	6	C	LLM0_PLLC_FB_A	PL42B	6	C	LLM0_PLLC_FB_A
U4	PL35A	6	T <sup>3</sup>	-	PL39A	6	T <sup>3</sup>	-	PL43A	6	T <sup>3</sup>	-
U3	PL35B	6	C <sup>3</sup>	-	PL39B	6	C <sup>3</sup>	-	PL43B	6	C <sup>3</sup>	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
W5	SLEEPN <sup>1</sup> / TOE <sup>2</sup>	-	-	-	SLEEPN <sup>1</sup> / TOE <sup>2</sup>	-	-	-	SLEEPN <sup>1</sup> / TOE <sup>2</sup>	-	-	-
Y2	INITN	5	-	-	INITN	5	-	-	INITN	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y3	-	-	-	-	PB3B	5	-	-	PB7B	5	-	-
W3	-	-	-	-	PB4A	5	T	-	PB8A	5	T	-
W4	-	-	-	-	PB4B	5	C	-	PB8B	5	C	-
AA2	-	-	-	-	PB5A	5	-	-	PB9A	5	-	-
AA1	-	-	-	-	PB6B	5	-	-	PB10B	5	-	-
W6	PB2A	5	-	-	PB7A	5	T	DQS	PB11A	5	T	DQS
W7	-	-	-	-	PB7B	5	C	-	PB11B	5	C	-
Y4	PB3A	5	T	-	PB8A	5	T	-	PB12A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y5	PB3B	5	C	-	PB8B	5	C	-	PB12B	5	C	-
AB2	PB4A	5	T	-	PB9A	5	T	-	PB13A	5	T	-
AA3	PB4B	5	C	-	PB9B	5	C	-	PB13B	5	C	-
AB3	PB5A	5	T	-	PB10A	5	T	-	PB14A	5	T	-
AA4	PB5B	5	C	-	PB10B	5	C	-	PB14B	5	C	-
W8	PB6A	5	T	-	PB11A	5	T	-	PB15A	5	T	-
W9	PB6B	5	C	-	PB11B	5	C	-	PB15B	5	C	-
AB4	PB7A	5	T	VREF1_5	PB12A	5	T	VREF1_5	PB16A	5	T	VREF1_5
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
AA5	PB7B	5	C	-	PB12B	5	C	-	PB16B	5	C	-
AB5	PB8A	5	-	-	PB13A	5	-	-	PB17A	5	-	-
Y6	PB9B	5	-	-	PB14B	5	-	-	PB18B	5	-	-
AA6	PB10A	5	T	DQS	PB15A	5	T	DQS	PB19A	5	T	DQS
AB6	PB10B	5	C	-	PB15B	5	C	-	PB19B	5	C	-
Y9	PB11A	5	T	-	PB16A	5	T	-	PB20A	5	T	-

**LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)**

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
AB19	PB37A	4	-	-	PB41A	4	-	-
AB20	PB38B	4	-	-	PB42B	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
V15	PB39A	4	T	DQS	PB43A	4	T	DQS
U15	PB39B	4	C	-	PB43B	4	C	-
Y15	PB40A	4	T	-	PB44A	4	T	-
W15	PB40B	4	C	-	PB44B	4	C	-
AA16	PB41A	4	T	-	PB45A	4	T	-
AA17	PB41B	4	C	-	PB45B	4	C	-
AA18	PB42A	4	T	-	PB46A	4	T	-
AA19	PB42B	4	C	-	PB46B	4	C	-
Y16	PB43A	4	T	-	PB47A	4	T	-
W16	PB43B	4	C	-	PB47B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA20	PB44A	4	T	-	PB48A	4	T	-
AA21	PB44B	4	C	-	PB48B	4	C	-
Y17	PB45A	4	-	-	PB49A	4	-	-
Y18	PB46B	4	-	-	PB50B	4	-	-
Y19	PB47A	4	T	DQS	PB51A	4	T	DQS
Y20	PB47B	4	C	-	PB51B	4	C	-
V16	PB48A	4	T	-	PB52A	4	T	-
U16	PB48B	4	C	-	PB52B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
U18	-	-	-	-	PB53A	4	T	-
V18	-	-	-	-	PB53B	4	C	-
W19	-	-	-	-	PB54A	4	T	-
W18	-	-	-	-	PB54B	4	C	-
U17	-	-	-	-	PB55A	4	T	-
V17	-	-	-	-	PB55B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
W17	-	-	-	-	PB56A	4	-	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
V19	PR43A	3	-	-	PR47A	3	-	-
U20	PR42B	3	C <sup>3</sup>	-	PR46B	3	C <sup>3</sup>	-
U19	PR42A	3	T <sup>3</sup>	-	PR46A	3	T <sup>3</sup>	-
V20	PR41B	3	C	-	PR45B	3	C	-
W20	PR41A	3	T	-	PR45A	3	T	-
T17	PR40B	3	C <sup>3</sup>	-	PR44B	3	C <sup>3</sup>	-
T18	PR40A	3	T <sup>3</sup>	-	PR44A	3	T <sup>3</sup>	-
T19	PR39B	3	C <sup>3</sup>	-	PR43B	3	C <sup>3</sup>	-
T20	PR39A	3	T <sup>3</sup>	-	PR43A	3	T <sup>3</sup>	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-

**LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)**

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
B3	PT8B	0	C	-	PT12B	0	C	-
A3	PT8A	0	T	-	PT12A	0	T	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
D7	PT7B	0	C	-	PT11B	0	C	-
C7	PT7A	0	T	DQS	PT11A	0	T	DQS
B2	PT6B	0	-	-	PT10B	0	-	-
C2	PT5A	0	-	-	PT9A	0	-	-
C3	PT4B	0	C	-	PT8B	0	C	-
D3	PT4A	0	T	-	PT8A	0	T	-
F7	PT3B	0	C	-	PT7B	0	C	-
E7	PT3A	0	T	-	PT7A	0	T	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
C6	-	-	-	-	PT6B	0	C	-
D6	-	-	-	-	PT6A	0	T	-
C5	-	-	-	-	PT5B	0	C	-
C4	-	-	-	-	PT5A	0	T	-
F6	-	-	-	-	PT4B	0	C	-
E6	-	-	-	-	PT4A	0	T	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
E4	-	-	-	-	PT3B	0	-	-
E5	CFG0	0	-	-	CFG0	0	-	-
D4	CFG1	0	-	-	CFG1	0	-	-
D5	DONE	0	-	-	DONE	0	-	-
A1	GND	-	-	-	GND	-	-	-
A2	GND	-	-	-	GND	-	-	-
A21	GND	-	-	-	GND	-	-	-
A22	GND	-	-	-	GND	-	-	-
AA1	GND	-	-	-	GND	-	-	-
AA22	GND	-	-	-	GND	-	-	-
AB1	GND	-	-	-	GND	-	-	-
AB2	GND	-	-	-	GND	-	-	-
AB21	GND	-	-	-	GND	-	-	-
AB22	GND	-	-	-	GND	-	-	-
B1	GND	-	-	-	GND	-	-	-
B22	GND	-	-	-	GND	-	-	-
H14	GND	-	-	-	GND	-	-	-
H9	GND	-	-	-	GND	-	-	-
J10	GND	-	-	-	GND	-	-	-
J11	GND	-	-	-	GND	-	-	-
J12	GND	-	-	-	GND	-	-	-
J13	GND	-	-	-	GND	-	-	-
J14	GND	-	-	-	GND	-	-	-

## Commercial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20E-3F484C	340	1.2V	-3	fpBGA	484	COM	19.7K
LFXP20E-4F484C	340	1.2V	-4	fpBGA	484	COM	19.7K
LFXP20E-5F484C	340	1.2V	-5	fpBGA	484	COM	19.7K
LFXP20E-3F388C	268	1.2V	-3	fpBGA	388	COM	19.7K
LFXP20E-4F388C	268	1.2V	-4	fpBGA	388	COM	19.7K
LFXP20E-5F388C	268	1.2V	-5	fpBGA	388	COM	19.7K
LFXP20E-3F256C	188	1.2V	-3	fpBGA	256	COM	19.7K
LFXP20E-4F256C	188	1.2V	-4	fpBGA	256	COM	19.7K
LFXP20E-5F256C	188	1.2V	-5	fpBGA	256	COM	19.7K

## Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3C-3Q208I	136	1.8/2.5/3.3V	-3	PQFP	208	IND	3.1K
LFXP3C-4Q208I	136	1.8/2.5/3.3V	-4	PQFP	208	IND	3.1K
LFXP3C-3T144I	100	1.8/2.5/3.3V	-3	TQFP	144	IND	3.1K
LFXP3C-4T144I	100	1.8/2.5/3.3V	-4	TQFP	144	IND	3.1K
LFXP3C-3T100I	62	1.8/2.5/3.3V	-3	TQFP	100	IND	3.1K
LFXP3C-4T100I	62	1.8/2.5/3.3V	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6C-3F256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	5.8K
LFXP6C-4F256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	5.8K
LFXP6C-3Q208I	142	1.8/2.5/3.3V	-3	PQFP	208	IND	5.8K
LFXP6C-4Q208I	142	1.8/2.5/3.3V	-4	PQFP	208	IND	5.8K
LFXP6C-3T144I	100	1.8/2.5/3.3V	-3	TQFP	144	IND	5.8K
LFXP6C-4T144I	100	1.8/2.5/3.3V	-4	TQFP	144	IND	5.8K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10C-3F388I	244	1.8/2.5/3.3V	-3	fpBGA	388	IND	9.7K
LFXP10C-4F388I	244	1.8/2.5/3.3V	-4	fpBGA	388	IND	9.7K
LFXP10C-3F256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	9.7K
LFXP10C-4F256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	9.7K