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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15000
Total RAM Bits	331776
Number of I/O	188
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp15e-3f256i

LatticeXP Family Data Sheet Introduction

July 2007 Data Sheet DS1001

Features

- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on – powers up in microseconds
  - No external configuration memory
  - Excellent design security, no bit stream to intercept
  - Reconfigure SRAM based logic in milliseconds
  - SRAM and non-volatile memory programmable through system configuration and JTAG ports
- **Sleep Mode**
  - Allows up to 1000x static current reduction
- **TransFR™ Reconfiguration (TFR)**
  - In-field logic update while system operates
- **Extensive Density and Package Options**
  - 3.1K to 19.7K LUT4s
  - 62 to 340 I/Os
  - Density migration supported
- **Embedded and Distributed Memory**
  - 54 Kbits to 396 Kbits sysMEM™ Embedded Block RAM
  - Up to 79 Kbits distributed RAM
  - Flexible memory resources:
    - Distributed and block memory
- **Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - SSTL 18 Class I
    - SSTL 3/2 Class I, II
    - HSTL15 Class I, III
    - HSTL 18 Class I, II, III
    - PCI
    - LVDS, Bus-LVDS, LVPECL, RSDS
- **Dedicated DDR Memory Support**
  - Implements interface up to DDR333 (166MHz)
- **sysCLOCK™ PLLs**
  - Up to 4 analog PLLs per device
  - Clock multiply, divide and phase shifting
- **System Level Support**
  - IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
  - Onboard oscillator for configuration
  - Devices operate with 3.3V, 2.5V, 1.8V or 1.2V power supply

Table 1-1. LatticeXP Family Selection Guide

Device	LFXP3	LFXP6	LFXP10	LFXP15	LFXP20
PFU/PFF Rows	16	24	32	40	44
PFU/PFF Columns	24	30	38	48	56
PFU/PFF (Total)	384	720	1216	1932	2464
LUTs (K)	3	6	10	15	20
Distributed RAM (KBits)	12	23	39	61	79
EBR SRAM (KBits)	54	72	216	324	396
EBR SRAM Blocks	6	8	24	36	44
V_{CC} Voltage	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V
PLLs	2	2	4	4	4
Max. I/O	136	188	244	300	340
Packages and I/O Combinations:					
100-pin TQFP (14 x 14 mm)	62				
144-pin TQFP (20 x 20 mm)	100	100			
208-pin PQFP (28 x 28 mm)	136	142			
256-ball fpBGA (17 x 17 mm)		188	188	188	188
388-ball fpBGA (23 x 23 mm)			244	268	268
484-ball fpBGA (23 x 23 mm)				300	340

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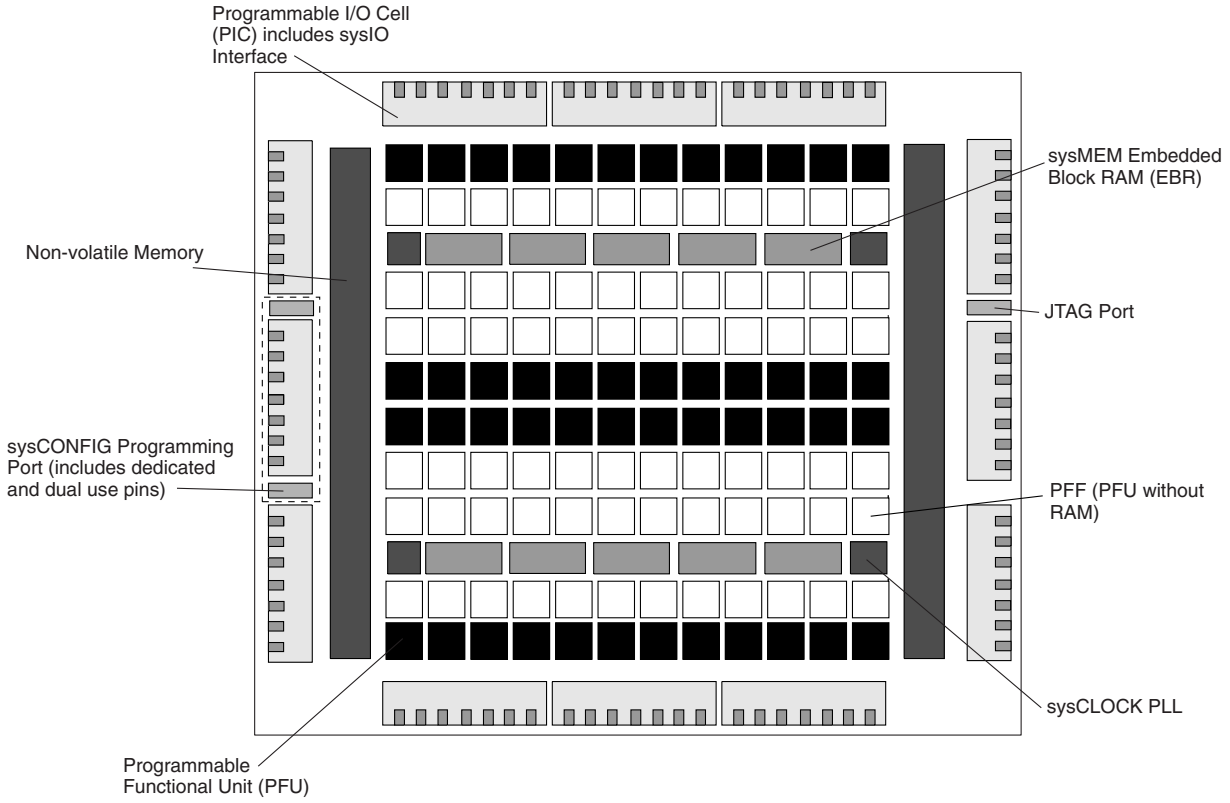
Figure 2-1. LatticeXP Top Level Block Diagram



PFU and PFF Blocks

The core of the LatticeXP devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of the data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-2. All the interconnections to and from PFU blocks are from routing. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-2. PFU Diagram

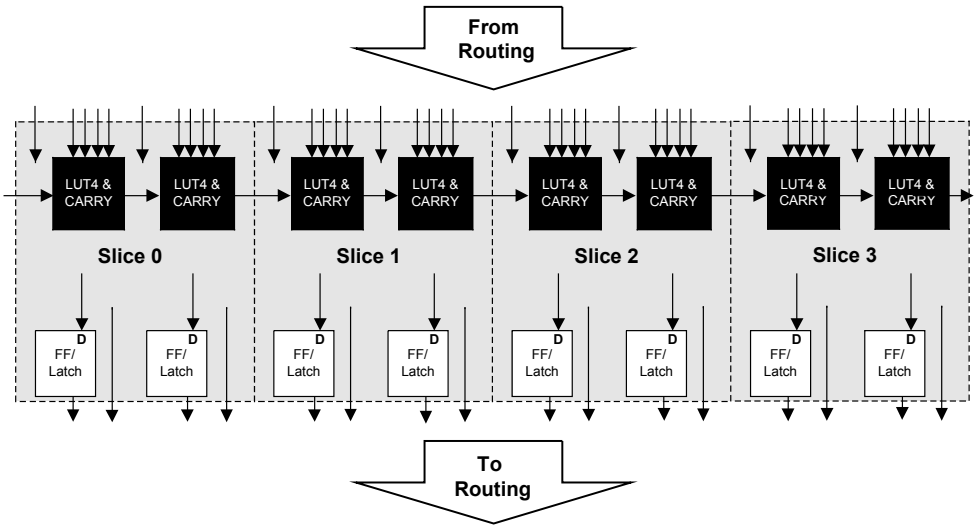


Figure 2-8. Per Quadrant Secondary Clock Selection

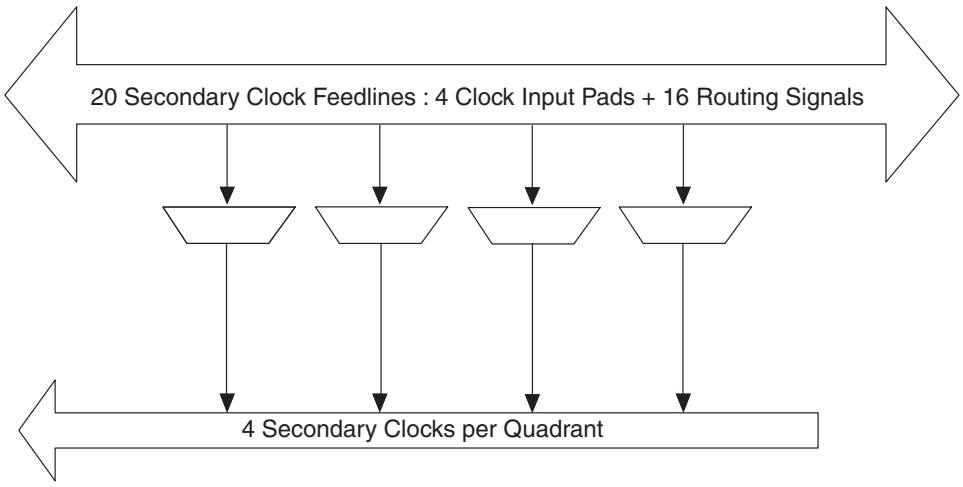
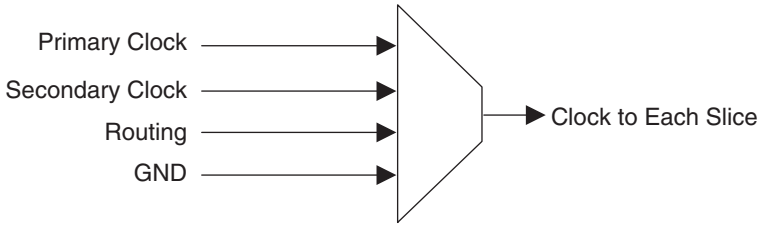


Figure 2-9. Slice Clock Selection



sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signals to the feedback divider: from CLKOP (PLL internal), from clock net (CLKOP or CLKOS) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the t_{LOCK} parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved irrespective of where the select signal is toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-12 illustrates the DCS Block Macro.

Figure 2-12. DCS Block Primitive

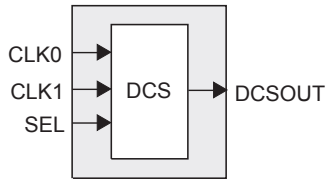
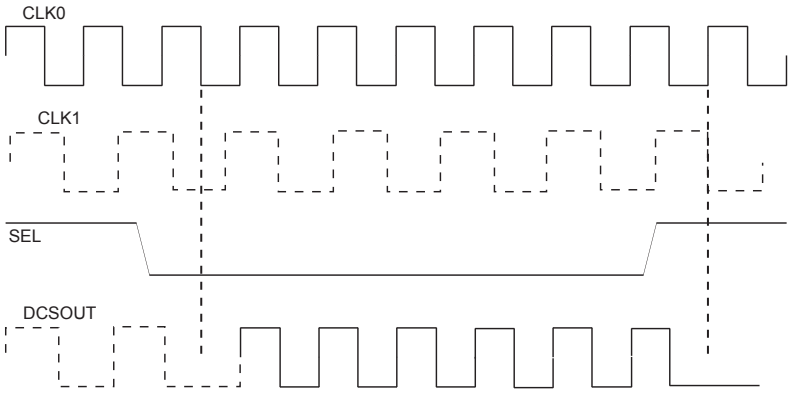


Figure 2-13 shows timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information on the DCS, please see details of additional technical documentation at the end of this data sheet.

Figure 2-13. DCS Waveforms



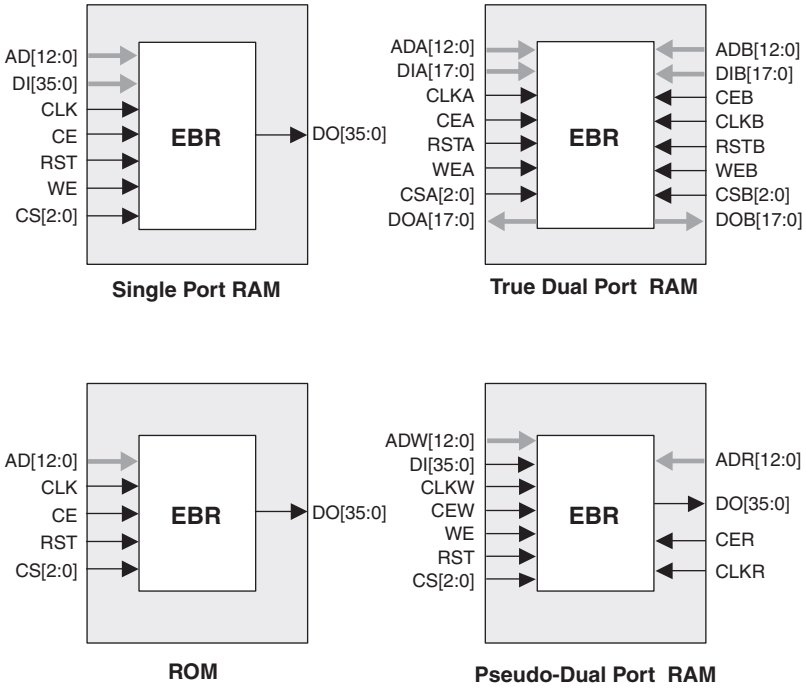
sysMEM Memory

The LatticeXP family of devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-6.

Figure 2-14. sysMEM Memory Primitives



The EBR memory supports three forms of write behavior for single port or dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

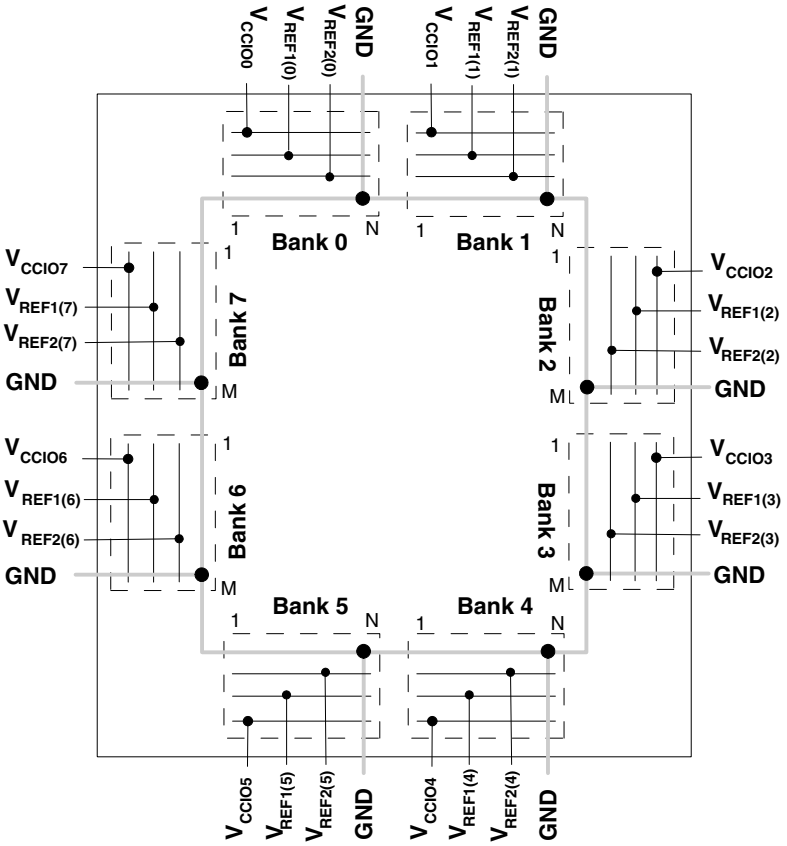
2. **Write Through** -þa copy of the input data appears at the output of the same port during a write cycle.þThis mode is supported for all data widths.

3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-15.

Figure 2-28. LatticeXP Banks



Note: N and M are the maximum number of I/Os per bank.

LatticeXP devices contain two types of sysIO buffer pairs.

1. **Top and Bottom sysIO Buffer Pair (Single-Ended Outputs Only)**
   The sysIO buffer pairs in the top and bottom banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

   Only the I/Os on the top and bottom banks have PCI clamps. Note that the PCI clamp is enabled after V_{CC}, V_{CCAUX} and V_{CCIO} are at valid operating levels and the device has been configured.

2. **Left and Right sysIO Buffer Pair (Differential and Single-Ended Outputs)**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. The referenced input buffer can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

   Select I/Os in the left and right banks have LVDS differential output drivers. Refer to the Logic Signal Connections tables for more information.

LatticeXP Family Data Sheet DC and Switching Characteristics

November 2007 Data Sheet DS1001

Absolute Maximum Ratings[1, 2, 3, 4]

	XPE (1.2V)	XPC (1.8V/2.5V/3.3V)
Supply Voltage V_{CC}	-0.5 to 1.32V	-0.5 to 3.75V
Supply Voltage V_{CCP}	-0.5 to 1.32V	-0.5 to 3.75V
Supply Voltage V_{CCAUX}	-0.5 to 3.75V	-0.5 to 3.75V
Supply Voltage V_{CCJ}	-0.5 to 3.75V	-0.5 to 3.75V
Output Supply Voltage V_{CCIO}	-0.5 to 3.75V	-0.5 to 3.75V
I/O Tristate Voltage Applied[5]	-0.5 to 3.75V	-0.5 to 3.75V
Dedicated Input Voltage Applied [5]	-0.5 to 3.75V	-0.5 to 4.25V
Storage Temperature (Ambient)	-65 to 150°C	-65 to 150°C
Junction Temp. (Tj)	+125°C	+125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions outside of those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. All chip grounds are connected together to a common package GND plane.
5. Overshoot and undershoot of -2V to (V_{IHMAX} + 2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions[3]

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Core Supply Voltage for 1.2V Devices	1.14	1.26	V
	Core Supply Voltage for 1.8V/2.5V/3.3V Devices	1.71	3.465	V
V_{CCP}	Supply Voltage for PLL for 1.2V Devices	1.14	1.26	V
	Supply Voltage for PLL for 1.8V/2.5V/3.3V Devices	1.71	3.465	V
V_{CCAUX}[4]	Auxiliary Supply Voltage	3.135	3.465	V
V_{CCIO}[1, 2]	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}[1]	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	85	C
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	C
$t_{JFLASHCOM}$	Junction Temperature, Flash Programming, Commercial	0	85	C
$t_{JFLASHIND}$	Junction Temperature, Flash Programming, Industrial	0	85	C

1. If V_{CCIO} or V_{CCJ} is set to 3.3V, they must be connected to the same power supply as V_{CCAUX}. For the XPE devices (1.2V V_{CC}), if V_{CCIO} or V_{CCJ} is set to 1.2V, they must be connected to the same power supply as V_{CC}.
2. See recommended voltages by I/O standard in subsequent table.
3. The system designer must ensure that the FPGA design stays within the specified junction temperature and package thermal capabilities of the device based on the expected operating frequency, activity factor and environment conditions of the system.
4. V_{CCAUX} ramp rate must not exceed 30mV/µs during power up when transitioning between 0V and 3.3V.

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Initialization Supply Current[1, 2, 3, 4, 5, 6]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[7]	Units
I_{CC}	Core Power Supply	LFXP3E	40	mA
		LFXP6E	50	mA
		LFXP10E	110	mA
		LFXP15E	140	mA
		LFXP20E	250	mA
		LFXP3C	60	mA
		LFXP6C	70	mA
		LFXP10C	150	mA
		LFXP15C	180	mA
		LFXP20C	290	mA
I_{CCAUX}	Auxiliary Power Supply V_{CCAUX} = 3.3V	LFXP3E/C	50	mA
		LFXP6E/C	60	mA
		LFXP10E/C	90	mA
		LFXP15 /C	110	mA
		LFXP20E/C	130	mA
I_{CCJ}	V_{CCJ} Power Supply	All	2	mA

1. Until DONE signal is active.
2. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
4. Frequency 0MHz.
5. Typical user pattern.
6. Assume normal bypass capacitor/decoupling capacitor across the supply.
7. T_A=25°C, power supplies at nominal voltage.

sysIO Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.5	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	8, 4	-8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2 (“C” Version)	-0.3	0.42	0.78	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2 (“E” Version)	-0.3	$0.35V_{CC}$	$0.65V_{CC}$	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
PCI	-0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	-0.5
SSTL3 class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCIO} - 1.1	8	-8
SSTL3 class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCIO} - 0.9	16	-16
SSTL2 class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	7.6	-7.6
SSTL2 class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCIO} - 0.43	15.2	-15.2
SSTL18 class I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.4	V_{CCIO} - 0.4	6.7	-6.7
HSTL15 class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	8	-8
HSTL15 class III	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	24	-8
HSTL18 class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	9.6	-9.6
HSTL18 class II	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	16	-16
HSTL18 class III	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	24	-8

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

Timing Diagrams

PFU Timing Diagrams

Figure 3-6. Slice Single/Dual Port Write Cycle Timing

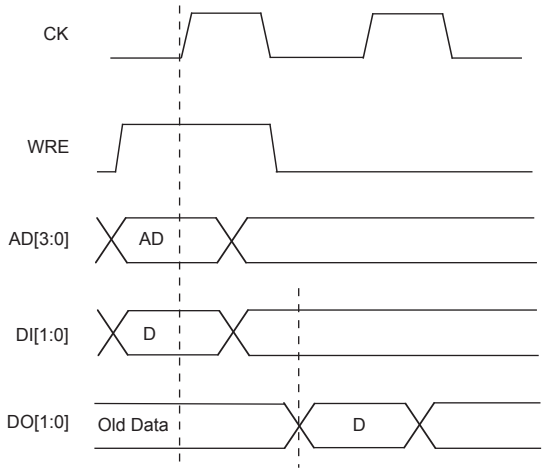
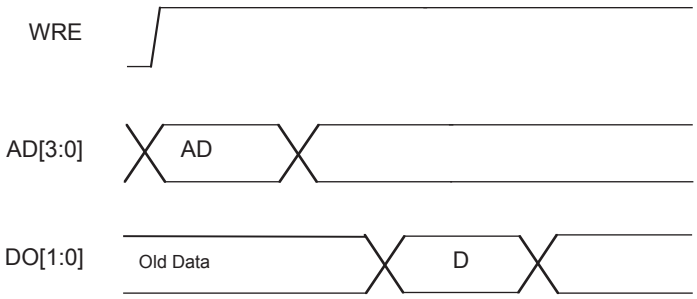


Figure 3-7. Slice Single /Dual Port Read Cycle Timing



Switching Test Conditions

Figure 3-13 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Figure 3-5.

Figure 3-13. Output Test Load, LVTTL and LVCMOS Standards

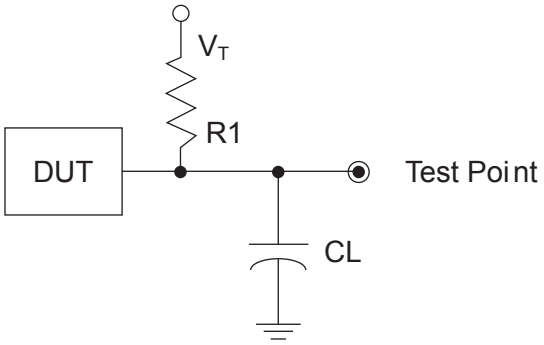


Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	0pF	LVCMOS 3.3 = 1.5V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	188	0pF	$V_{CCIO}/2$	V_{OL}
LVCMOS 2.5 I/O (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVCMOS 2.5 I/O (H -> Z)			V_{OH} - 0.15	V_{OL}
LVCMOS 2.5 I/O (L -> Z)			V_{OL} + 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO within PIC	Polarity	DDR Strobe (DQS) and Data (DQ) Pins
P[Edge] [n-4]	A	True	DQ
	B	Complement	DQ
P[Edge] [n-3]	A	True	DQ
	B	Complement	DQ
P[Edge] [n-2]	A	True	DQ
	B	Complement	DQ
P[Edge] [n-1]	A	True	DQ
P[Edge] [n]			
	B	Complement	DQ
P[Edge] [n+1]	A	True	[Edge]DQSn
	B	Complement	DQ
P[Edge] [n+2]	A	True	DQ
	B	Complement	DQ
P[Edge] [n+3]	A	True	DQ
	B	Complement	DQ

Notes:
1. “n” is a row/column PIC number.
2. The DDR interface is designed for memories that support one DQS strobe per eight bits of data. In some packages, all the potential DDR data (DQ) pins may not be available.
3. The definition of the PIC numbering is provided in the Signal Names column of the Signal Descriptions table in this data sheet.

Power Supply and NC Connections

Signals	100 TQFP	144 TQFP	208 PQFP	256 fpBGA	388 fpBGA	484 fpBGA
V_{CC}	28, 77	14, 39, 73, 112	19, 35, 53, 80, 107, 151, 158, 182	D4, D13, E5, E12, M5, M12, N4, N13	H9, J8, J15, K8, K15, L8, L15, M8, M15, N8, N15, P8, P15, R9	F10, F13, G9, G10, G13, G14, H8, H15, J7, J16, K6, K7, K16, K17, N6, N7, N16, N17, P7, P16, R8, R15, T9, T10, T13, T14, U10, U13
V_{CCIO0}	94	133	189, 199	F7, F8	G8, G9, G10, G11, H8	F11, G11, H10, H11
V_{CCIO1}	82	119	167, 177	F9, F10	G12, G13, G14, G15, H15	F12, G12, H12, H13
V_{CCIO2}	65	98	140, 149	G11, H11	H16, J16, K16, L16	K15, L15, L16, L17
V_{CCIO3}	58	88	115, 125	J11, K11	M16, N16, P16, R16	M15, M16, M17, N15
V_{CCIO4}	47	61, 68	87, 97	L9, L10	R15, T12, T13, T14, T15	R12, R13, T12, U12
V_{CCIO5}	38	49	64, 74	L7, L8	R8, T8, T9, T10, T11	R10, R11, T11, U11
V_{CCIO6}	22	21	28, 41	J6, K6	M7, N7, P7, R7	M6, M7, M8, N8
V_{CCIO7}	7	8	13, 23	G6, H6	H7, J7, K7, L7	K8, L6, L7, L8
V_{CCJ}	73	108	154	D16	E20	E20
V_{CCP0}	17	19	25	H4	M2	L5
V_{CCP1}	60	91	128	J12	M21	L18
V_{CCAUX}	25, 71	36, 106	50, 152	E4, E13, M4, M13	G7, G16, T7, T16	G7, G8, G15, G16, H7, H16, R7, R16, T7, T8, T15, T16
GND[1]	10, 18, 21, 33, 43, 44, 52, 59, 68, 84, 90, 99	3, 11, 20, 28, 44, 54, 56, 64, 75, 85, 90, 101, 121, 127, 136	5, 7, 16, 26, 38, 47, 49, 59, 69, 79, 82, 92, 106, 109, 118, 121, 127, 130, 135, 143, 163, 172, 181, 184, 194, 207	A1, A16, F6, F11, G7, G8, G9, G10, H5, H7, H8, H9, H10, J7, J8, J9, J10, J13, K7, K8, K9, K10, L6, L11, T1, T16	A1, A22, H10, H11, H12, H13, H14, J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N1, N9, N10, N11, N12, N13, N14, N22, P9, P10, P11, P12, P13, P14, R10, R11, R12, R13, R14, AB1, AB22	A1, A2, A21, A22, B1, B22, H9, H14, J8, J9, J10, J11, J12, J13, J14, J15, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, M20, N2, N9, N10, N11, N12, N13, N14, P8, P9, P10, P11, P12, P13, P14, P15, R9, R14, AA1, AA22, AB1, AB2, AB21, AB22
NC[2]	—	—	XP3: 27, 33, 34, 129, 133, 134	—	XP10: C2, C15, C16, C17, D4, D5, D6, D7, D16, D17, E4, E19, W3, W4, W7, W17, W18, W19, W20, Y3, Y15, Y16, AA1, AA2	XP15: B21, C4, C5, C6, C18, C19, C20, C21, D6, D18, E4, E6, E18, F6, L1, L19, L20, M1, M2, M19, M21, N1, N21, N22, P1, P2, U5, U6, U17, U18, V5, V6, V17, V18, W17, W18, W19, Y3, Y4, Y5

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{CC} or GND.

LFXP3 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	Pin Function	Bank	Differential	Dual Function
88	PT14B	1	-	D7
89	PT13B	0	C	BUSY
90	GNDIO0	0	-	-
91	PT13A	0	T	CS1N
92	PT12B	0	C	PCLKC0_0
93	PT12A	0	T	PCLKT0_0
94	VCCIO0	0	-	-
95	PT9A	0	-	DOUT
96	PT8A	0	-	WRITEN
97	PT6A	0	-	DI
98	PT5A	0	-	CSN
99	GND	-	-	-
100	CFG0	0	-	-

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
93	PR9A	2	T	PCLKT2_0	PR12A	2	T	PCLKT2_0
94	PR8B	2	C	RUM0_PLLC_IN_A	PR8B	2	C	RUM0_PLLC_IN_A
95	PR8A	2	T	RUM0_PLLT_IN_A	PR8A	2	T	RUM0_PLLT_IN_A
96	PR7B	2	C[3]	-	PR7B	2	C[3]	-
97	PR7A	2	T[3]	DQS	PR7A	2	T[3]	DQS
98	VCCIO2	2	-	-	VCCIO2	2	-	-
99	PR6B	2	-	VREF1_2	PR6B	2	-	VREF1_2
100	PR5A	2	-	VREF2_2	PR5A	2	-	VREF2_2
101	GNDIO2	2	-	-	GNDIO2	2	-	-
102	PR3B	2	C	RUM0_PLLC_FB_A	PR3B	2	C	RUM0_PLLC_FB_A
103	PR3A	2	T	RUM0_PLLT_FB_A	PR3A	2	T	RUM0_PLLT_FB_A
104	PR2B	2	C[3]	-	PR2B	2	C[3]	-
105	PR2A	2	T[3]	-	PR2A	2	T[3]	-
106	VCCAUX	-	-	-	VCCAUX	-	-	-
107	TDO	-	-	-	TDO	-	-	-
108	VCCJ	-	-	-	VCCJ	-	-	-
109	TDI	-	-	-	TDI	-	-	-
110	TMS	-	-	-	TMS	-	-	-
111	TCK	-	-	-	TCK	-	-	-
112	VCC	-	-	-	VCC	-	-	-
113	PT25A	1	-	VREF1_1	PT28A	1	-	VREF1_1
114	PT24A	1	-	-	PT27A	1	-	-
115	PT23A	1	-	D0	PT26A	1	-	D0
116	PT22B	1	C	D1	PT25B	1	C	D1
117	PT22A	1	T	VREF2_1	PT25A	1	T	VREF2_1
118	PT21A	1	-	D2	PT24A	1	-	D2
119	VCCIO1	1	-	-	VCCIO1	1	-	-
120	PT20B	1	-	D3	PT23B	1	-	D3
121	GNDIO1	1	-	-	GNDIO1	1	-	-
122	PT17A	1	-	D4	PT20A	1	-	D4
123	PT16A	1	-	D5	PT19A	1	-	D5
124	PT15B	1	C	D6	PT18B	1	C	D6
125	PT15A	1	T	-	PT18A	1	T	-
126	PT14B	1	-	D7	PT17B	1	-	D7
127	GND	-	-	-	GND	-	-	-
128	PT13B	0	C	BUSY	PT16B	0	C	BUSY
129	PT13A	0	T	CS1N	PT16A	0	T	CS1N
130	PT12B	0	C	PCLKC0_0	PT15B	0	C	PCLKC0_0
131	PT12A	0	T	PCLKT0_0	PT15A	0	T	PCLKT0_0
132	PT11B	0	C	-	PT14B	0	C	-
133	VCCIO0	0	-	-	VCCIO0	0	-	-
134	PT11A	0	T	DQS	PT14A	0	T	DQS
135	PT9A	0	-	DOUT	PT12A	0	-	DOUT
136	GNDIO0	0	-	-	GNDIO0	0	-	-
137	PT8A	0	-	WRITEN	PT11A	0	-	WRITEN
138	PT7A	0	-	VREF1_0	PT10A	0	-	VREF1_0

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
47	GNDIO6	6	-	-	GNDIO6	6	-	-
48	PL18B	6	C[3]	-	PL26B	6	C[3]	-
49	GND	-	-	-	GND	-	-	-
50	VCCAUX	-	-	-	VCCAUX	-	-	-
51	SLEEPN[1]/TOE[2]	-	-	-	SLEEPN[1]/TOE[2]	-	-	-
52	INITN	5	-	-	INITN	5	-	-
53	VCC	-	-	-	VCC	-	-	-
54	PB2B	5	-	VREF1_5	PB5B	5	-	VREF1_5
55	PB3A	5	T	-	PB6A	5	T	DQS
56	PB3B	5	C	-	PB6B	5	C	-
57	PB4A	5	T	-	PB7A	5	T	-
58	PB4B	5	C	-	PB7B	5	C	-
59	GNDIO5	5	-	-	GNDIO5	5	-	-
60	PB5A	5	T	-	PB8A	5	T	-
61	PB5B	5	C	VREF2_5	PB8B	5	C	VREF2_5
62	PB6A	5	T	-	PB9A	5	T	-
63	PB6B	5	C	-	PB9B	5	C	-
64	VCCIO5	5	-	-	VCCIO5	5	-	-
65	PB7A	5	T	-	PB10A	5	T	-
66	PB7B	5	C	-	PB10B	5	C	-
67	PB8A	5	T	-	PB11A	5	T	-
68	PB8B	5	C	-	PB11B	5	C	-
69	GNDIO5	5	-	-	GNDIO5	5	-	-
70	PB9A	5	-	-	PB12A	5	-	-
71	PB10B	5	-	-	PB13B	5	-	-
72	PB11A	5	T	DQS	PB14A	5	T	DQS
73	PB11B	5	C	-	PB14B	5	C	-
74	VCCIO5	5	-	-	VCCIO5	5	-	-
75	PB12A	5	T	-	PB15A	5	T	-
76	PB12B	5	C	-	PB15B	5	C	-
77	PB13A	5	T	-	PB16A	5	T	-
78	PB13B	5	C	-	PB16B	5	C	-
79	GND	-	-	-	GND	-	-	-
80	VCC	-	-	-	VCC	-	-	-
81	PB14A	4	T	-	PB17A	4	T	-
82	GNDIO4	4	-	-	GNDIO4	4	-	-
83	PB14B	4	C	-	PB17B	4	C	-
84	PB15A	4	T	PCLKT4_0	PB18A	4	T	PCLKT4_0
85	PB15B	4	C	PCLKC4_0	PB18B	4	C	PCLKC4_0
86	PB16A	4	T	-	PB19A	4	T	-
87	VCCIO4	4	-	-	VCCIO4	4	-	-
88	PB16B	4	C	-	PB19B	4	C	-
89	PB17A	4	-	-	PB20A	4	-	-
90	PB18B	4	-	-	PB21B	4	-	-
91	PB19A	4	T	DQS	PB22A	4	T	DQS
92	GNDIO4	4	-	-	GNDIO4	4	-	-

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
93	PB19B	4	C	VREF1_4	PB22B	4	C	VREF1_4
94	PB20A	4	T	-	PB23A	4	T	-
95	PB20B	4	C	-	PB23B	4	C	-
96	PB21A	4	T	-	PB24A	4	T	-
97	VCCIO4	4	-	-	VCCIO4	4	-	-
98	PB21B	4	C	-	PB24B	4	C	-
99	PB22A	4	T	-	PB25A	4	T	-
100	PB22B	4	C	-	PB25B	4	C	-
101	PB23A	4	T	-	PB26A	4	T	-
102	PB23B	4	C	-	PB26B	4	C	-
103	PB24A	4	T	VREF2_4	PB27A	4	-	VREF2_4
104	PB24B	4	C	-	PB30A	4	T	DQS
105	PB25A	4	-	-	PB30B	4	C	-
106	GND	-	-	-	GND	-	-	-
107	VCC	-	-	-	VCC	-	-	-
108	PR18B	3	C[3]	-	PR26B	3	C[3]	-
109	GNDIO3	3	-	-	GNDIO3	3	-	-
110	PR18A	3	T[3]	-	PR26A	3	T[3]	-
111	PR17B	3	C	-	PR25B	3	C	-
112	PR17A	3	T	-	PR25A	3	T	-
113	PR16B	3	C[3]	-	PR24B	3	C[3]	-
114	PR16A	3	T[3]	DQS	PR24A	3	T[3]	DQS
115	VCCIO3	3	-	-	VCCIO3	3	-	-
116	PR15B	3	-	VREF1_3	PR23B	3	-	VREF1_3
117	PR14A	3	-	VREF2_3	PR22A	3	-	VREF2_3
118	GNDIO3	3	-	-	GNDIO3	3	-	-
119	PR13B	3	C	-	PR21B	3	C[3]	-
120	PR13A	3	T	-	PR21A	3	T[3]	-
121	GND	-	-	-	GND	-	-	-
122	PR12B	3	C	-	PR20B	3	C	-
123	PR12A	3	T	-	PR20A	3	T	-
124	PR11B	3	C	-	PR19B	3	C[3]	-
125	VCCIO3	3	-	-	VCCIO3	3	-	-
126	PR11A	3	T	-	PR19A	3	T[3]	-
127	GNDP1	-	-	-	GNDP1	-	-	-
128	VCCP1	-	-	-	VCCP1	-	-	-
129	NC	-	-	-	PR13A	2	-	-
130	GND	-	-	-	GND	-	-	-
131	PR9B	2	C	PCLKC2_0	PR12B	2	C	PCLKC2_0
132	PR9A	2	T	PCLKT2_0	PR12A	2	T	PCLKT2_0
133	NC	-	-	-	PR11B	2	C[3]	-
134	NC	-	-	-	PR11A	2	T[3]	-
135	GNDIO2	2	-	-	GNDIO2	2	-	-
136	PR8B	2	C	RUM0_PLLC_IN_A	PR8B	2	C	RUM0_PLLC_IN_A
137	PR8A	2	T	RUM0_PLLT_IN_A	PR8A	2	T	RUM0_PLLT_IN_A
138	PR7B	2	C[3]	-	PR7B	2	C[3]	-

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L7	VCCIO5	5	-	-	VCCIO5	5	-	-
L8	VCCIO5	5	-	-	VCCIO5	5	-	-
J6	VCCIO6	6	-	-	VCCIO6	6	-	-
K6	VCCIO6	6	-	-	VCCIO6	6	-	-
G6	VCCIO7	7	-	-	VCCIO7	7	-	-
H6	VCCIO7	7	-	-	VCCIO7	7	-	-

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
J15	GND	-	-	-	GND	-	-	-
J8	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-
K10	GND	-	-	-	GND	-	-	-
K11	GND	-	-	-	GND	-	-	-
K12	GND	-	-	-	GND	-	-	-
K13	GND	-	-	-	GND	-	-	-
K14	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-
L10	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-
L12	GND	-	-	-	GND	-	-	-
L13	GND	-	-	-	GND	-	-	-
L14	GND	-	-	-	GND	-	-	-
L9	GND	-	-	-	GND	-	-	-
M10	GND	-	-	-	GND	-	-	-
M11	GND	-	-	-	GND	-	-	-
M12	GND	-	-	-	GND	-	-	-
M13	GND	-	-	-	GND	-	-	-
M14	GND	-	-	-	GND	-	-	-
M9	GND	-	-	-	GND	-	-	-
N10	GND	-	-	-	GND	-	-	-
N11	GND	-	-	-	GND	-	-	-
N12	GND	-	-	-	GND	-	-	-
N13	GND	-	-	-	GND	-	-	-
N14	GND	-	-	-	GND	-	-	-
N9	GND	-	-	-	GND	-	-	-
P10	GND	-	-	-	GND	-	-	-
P11	GND	-	-	-	GND	-	-	-
P12	GND	-	-	-	GND	-	-	-
P13	GND	-	-	-	GND	-	-	-
P14	GND	-	-	-	GND	-	-	-
P15	GND	-	-	-	GND	-	-	-
P8	GND	-	-	-	GND	-	-	-
P9	GND	-	-	-	GND	-	-	-
R14	GND	-	-	-	GND	-	-	-
R9	GND	-	-	-	GND	-	-	-
F10	VCC	-	-	-	VCC	-	-	-
F13	VCC	-	-	-	VCC	-	-	-
G10	VCC	-	-	-	VCC	-	-	-
G13	VCC	-	-	-	VCC	-	-	-
G14	VCC	-	-	-	VCC	-	-	-

LatticeXP Family Data Sheet Revision History

November 2007 **Data Sheet DS1001**

Revision History

Date	Version	Section	Change Summary
February 2005	01.0	—	Initial release.
April 2005	01.1	Architecture	EBR memory support section updated with clarification.
May 2005	01.2	Introduction	Added TransFR Reconfiguration to Features section.
		Architecture	Added TransFR section.
June 2005	01.3	Pinout Information	Added pinout information for LFXP3, LFXP6, LFXP15 and LFXP20.
July 2005	02.0	Introduction	Updated XP6, XP15 and XP20 EBR SRAM Bits and Block numbers.
		Architecture	Updated Per Quadrant Primary Clock Selection figure.
			Added Typical I/O Behavior During Power-up section.
			Updated Device Configuration section under Configuration and Testing.
		DC and Switching Characteristics	Clarified Hot Socketing Specification
			Updated Supply Current (Standby) Table
			Updated Initialization Supply Current Table
			Added Programming and Erase Flash Supply Current table
			Added LVDS Emulation section. Updated LVDS25E Output Termination Example figure and LVDS25E DC Conditions table.
			Updated Differential LVPECL diagram and LVPECL DC Conditions table.
			Deleted 5V Tolerant Input Buffer section. Updated RSDS figure and RSDS DC Conditions table.
			Updated sysCONFIG Port Timing Specifications
			Updated JTAG Port Timing Specifications. Added Flash Download Time table.
		Pinout Information	Updated Signal Descriptions table.
			Updated Logic Signal Connections Dual Function column.
		Ordering Information	Added lead-free ordering part numbers.
July 2005	02.1	DC and Switching Characteristics	Clarification of Flash Programming Junction Temperature
August 2005	02.2	Introduction	Added Sleep Mode feature.
		Architecture	Added Sleep Mode section.
		DC and Switching Characteristics	Added Sleep Mode Supply Current Table
			Added Sleep Mode Timing section
		Pinout Information	Added SLEEPN and TOE signal names, descriptions and footnotes.
			Added SLEEPN and TOE to pinout information and footnotes.
			Added footnote 3 to Logic Signal Connections tables for clarification on emulated LVDS output.
September 2005	03.0	Architecture	Added clarification of PCI clamp.
			Added clarification to SLEEPN Pin Characteristics section.
		DC and Switching Characteristics	DC Characteristics, added footnote 4 for clarification. Updated Supply Current (Sleep Mode), Supply Current (Standby), Initialization Supply Current, and Programming and Erase Flash Supply Current typical numbers.

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