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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

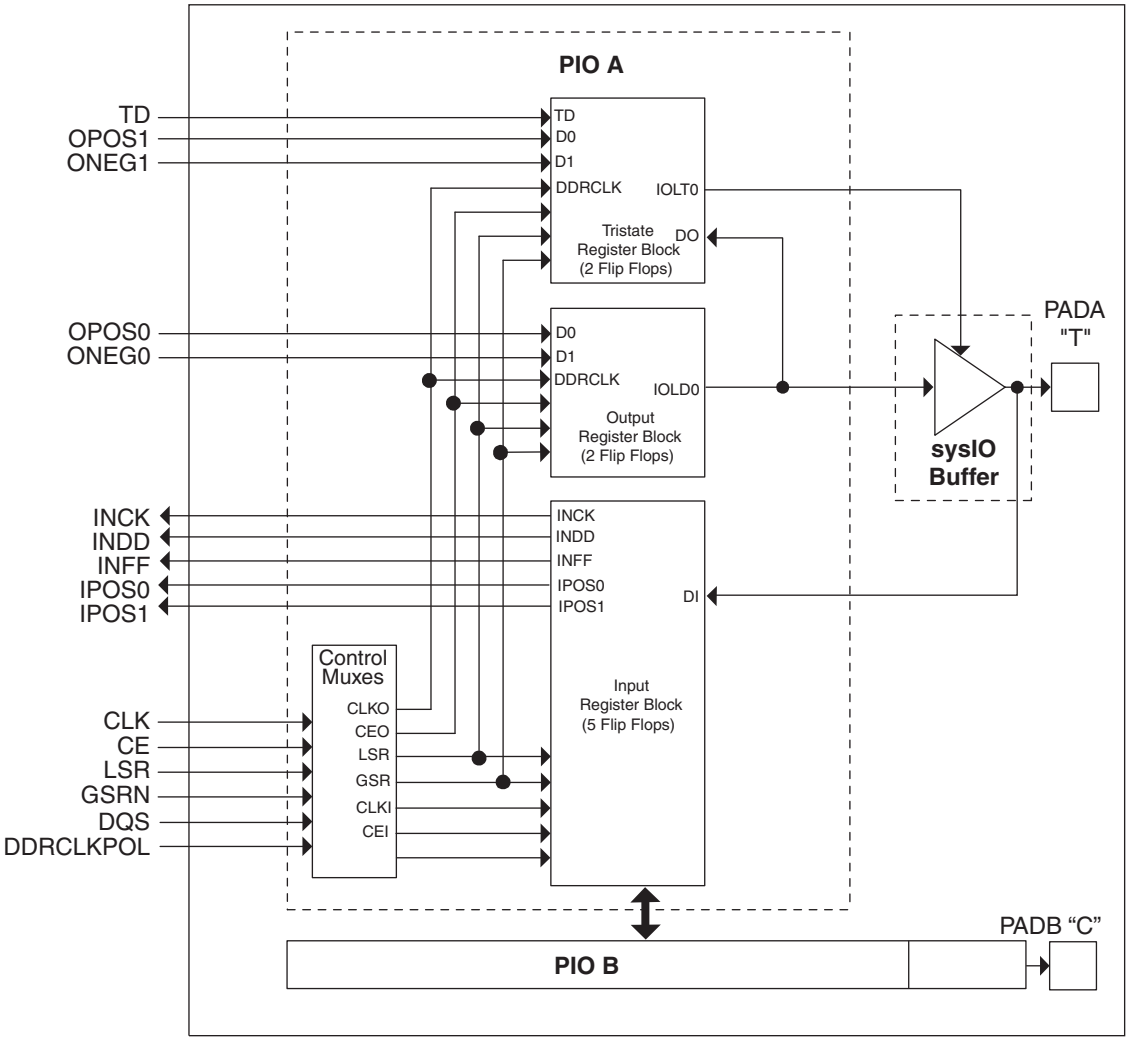
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 15000 |
| Total RAM Bits | 331776 |
| Number of I/O | 300 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp15e-3f484i |

*Figure 2-17. PIC Diagram*




In the LatticeXP family, seven PIOs or four (3.5) PICs are grouped together to provide two LVDS differential pairs, one PIC pair and one single I/O, as shown in Figure 2-18.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”). The PAD Labels “T” and “C” distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 14 PIOs (a group of 8 PICs) contains a delay element to facilitate the generation of DQS signals as shown in Figure 2-19. The DQS signal feeds the DQS bus which spans the set of 13 PIOs (8 PICs). The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table in this data sheet.

## Absolute Maximum Ratings[1, 2, 3, 4]

| | XPE (1.2V) | XPC (1.8V/2.5V/3.3V) |
|---|---|---|
| Supply Voltage $V_{CC}$ | -0.5 to 1.32V | -0.5 to 3.75V |
| Supply Voltage $V_{CCP}$ | -0.5 to 1.32V | -0.5 to 3.75V |
| Supply Voltage $V_{CCAUX}$ | -0.5 to 3.75V | -0.5 to 3.75V |
| Supply Voltage $V_{CCJ}$ | -0.5 to 3.75V | -0.5 to 3.75V |
| Output Supply Voltage $V_{CCIO}$ | -0.5 to 3.75V | -0.5 to 3.75V |
| I/O Tristate Voltage Applied[5] | -0.5 to 3.75V | -0.5 to 3.75V |
| Dedicated Input Voltage Applied [5] | -0.5 to 3.75V | -0.5 to 4.25V |
| Storage Temperature (Ambient) | -65 to 150°C | -65 to 150°C |
| Junction Temp. (Tj) | +125°C | +125°C |

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions outside of those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. All chip grounds are connected together to a common package GND plane.
5. Overshoot and undershoot of -2V to ($V_{IHMAX}$ + 2) volts is permitted for a duration of <20ns.

## Recommended Operating Conditions[3]

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage for 1.2V Devices | 1.14 | 1.26 | V |
| | Core Supply Voltage for 1.8V/2.5V/3.3V Devices | 1.71 | 3.465 | V |
| $V_{CCP}$ | Supply Voltage for PLL for 1.2V Devices | 1.14 | 1.26 | V |
| | Supply Voltage for PLL for 1.8V/2.5V/3.3V Devices | 1.71 | 3.465 | V |
| $V_{CCAUX}$[4] | Auxiliary Supply Voltage | 3.135 | 3.465 | V |
| $V_{CCIO}$[1, 2] | I/O Driver Supply Voltage | 1.14 | 3.465 | V |
| $V_{CCJ}$[1] | Supply Voltage for IEEE 1149.1 Test Access Port | 1.14 | 3.465 | V |
| $t_{JCOM}$ | Junction Temperature, Commercial Operation | 0 | 85 | C |
| $t_{JIND}$ | Junction Temperature, Industrial Operation | -40 | 100 | C |
| $t_{JFLASHCOM}$ | Junction Temperature, Flash Programming, Commercial | 0 | 85 | C |
| $t_{JFLASHIND}$ | Junction Temperature, Flash Programming, Industrial | 0 | 85 | C |

1. If $V_{CCIO}$ or $V_{CCJ}$ is set to 3.3V, they must be connected to the same power supply as $V_{CCAUX}$. For the XPE devices (1.2V $V_{CC}$), if $V_{CCIO}$ or $V_{CCJ}$ is set to 1.2V, they must be connected to the same power supply as $V_{CC}$.
2. See recommended voltages by I/O standard in subsequent table.
3. The system designer must ensure that the FPGA design stays within the specified junction temperature and package thermal capabilities of the device based on the expected operating frequency, activity factor and environment conditions of the system.
4. $V_{CCAUX}$ ramp rate must not exceed 30mV/µs during power up when transitioning between 0V and 3.3V.

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# sysIO Differential Electrical Characteristics

## LVDS

**Over Recommended Operating Conditions**

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{INP}$, $V_{INM}$ | Input Voltage | | 0 | — | 2.4 | V |
| $V_{THD}$ | Differential Input Threshold | | +/-100 | — | — | mV |
| $V_{CM}$ | Input Common Mode Voltage | 100mV ≤ $V_{THD}$ | $V_{THD}$/2 | 1.2 | 1.8 | V |
| | | 200mV ≤ $V_{THD}$ | $V_{THD}$/2 | 1.2 | 1.9 | V |
| | | 350mV ≤ $V_{THD}$ | $V_{THD}$/2 | 1.2 | 2.0 | V |
| $I_{IN}$ | Input current | Power on or power off | — | — | +/-10 | µA |
| $V_{OH}$ | Output high voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 ohms | — | 1.38 | 1.60 | V |
| $V_{OL}$ | Output low voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 ohms | 0.9V | 1.03 | — | V |
| $V_{OD}$ | Output voltage differential | ($V_{OP}$ - $V_{OM}$), $R_T$ = 100 ohms | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ between high and low | | — | — | 50 | mV |
| $V_{OS}$ | Output voltage offset | ($V_{OP}$ - $V_{OM}$)/2, $R_T$ = 100 ohms | 1.125 | 1.25 | 1.375 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ between H and L | | — | — | 50 | mV |
| $I_{OSD}$ | Output short circuit current | $V_{OD}$ = 0V Driver outputs shorted | — | — | 6 | mA |

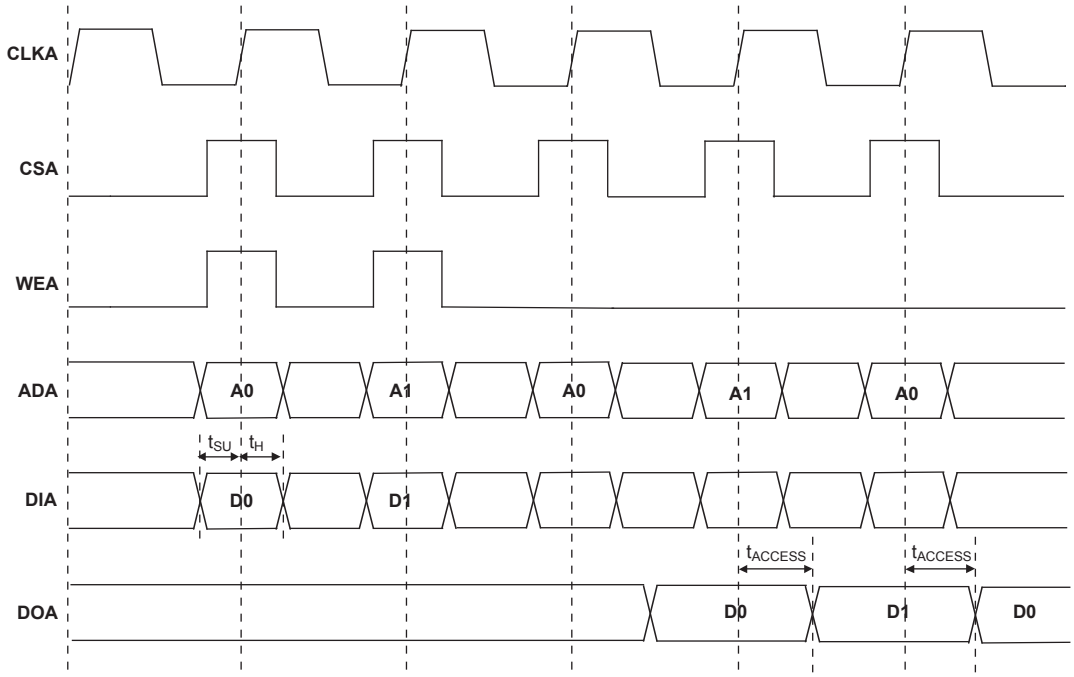
# LatticeXP Internal Timing Parameters[1]

**Over Recommended Operating Conditions**

| Parameter | Description | -5 | | -4 | | -3 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **PFU/PFF Logic Mode Timing** | | | | | | | | |
| $t_{LUT4_PFU}$ | LUT4 Delay (A to D Inputs to F Output) | — | 0.28 | — | 0.34 | — | 0.40 | ns |
| $t_{LUT6_PFU}$ | LUT6 Delay (A to D Inputs to OFX Output) | — | 0.44 | — | 0.53 | — | 0.63 | ns |
| $t_{LSR_PFU}$ | Set/Reset to Output of PFU | — | 0.90 | — | 1.08 | — | 1.29 | ns |
| $t_{SUM_PFU}$ | Clock to Mux (M0,M1) Input Setup Time | 0.13 | — | 0.15 | — | 0.19 | — | ns |
| $t_{HM_PFU}$ | Clock to Mux (M0,M1) Input Hold Time | -0.04 | — | -0.03 | — | -0.03 | — | ns |
| $t_{SUD_PFU}$ | Clock to D Input Setup Time | 0.13 | — | 0.16 | — | 0.19 | — | ns |
| $t_{HD_PFU}$ | Clock to D Input Hold Time | -0.03 | — | -0.02 | — | -0.02 | — | ns |
| $t_{CK2Q_PFU}$ | Clock to Q Delay, D-type Register Configuration | — | 0.40 | — | 0.48 | — | 0.58 | ns |
| $t_{LE2Q_PFU}$ | Clock to Q Delay Latch Configuration | — | 0.53 | — | 0.64 | — | 0.76 | ns |
| $t_{LD2Q_PFU}$ | D to Q Throughput Delay when Latch is Enabled | — | 0.55 | — | 0.66 | — | 0.79 | ns |
| **PFU Dual Port Memory Mode Timing** | | | | | | | | |
| $t_{CORAM_PFU}$ | Clock to Output | — | 0.40 | — | 0.48 | — | 0.58 | ns |
| $t_{SUDATA_PFU}$ | Data Setup Time | -0.18 | — | -0.14 | — | -0.11 | — | ns |
| $t_{HDATA_PFU}$ | Data Hold Time | 0.28 | — | 0.34 | — | 0.40 | — | ns |
| $t_{SUADDR_PFU}$ | Address Setup Time | -0.46 | — | -0.37 | — | -0.30 | — | ns |
| $t_{HADDR_PFU}$ | Address Hold Time | 0.71 | — | 0.85 | — | 1.02 | — | ns |
| $t_{SUWREN_PFU}$ | Write/Read Enable Setup Time | -0.22 | — | -0.17 | — | -0.14 | — | ns |
| $t_{HWREN_PFU}$ | Write/Read Enable Hold Time | 0.33 | — | 0.40 | — | 0.48 | — | ns |
| **PIC Timing** | | | | | | | | |
| **PIO Input/Output Buffer Timing** | | | | | | | | |
| $t_{IN_PIO}$ | Input Buffer Delay | — | 0.62 | — | 0.72 | — | 0.85 | ns |
| $t_{OUT_PIO}$ | Output Buffer Delay | — | 2.12 | — | 2.54 | — | 3.05 | ns |
| **IOLOGIC Input/Output Timing** | | | | | | | | |
| $t_{SUI_PIO}$ | Input Register Setup Time (Data Before Clock) | 1.35 | — | 1.83 | — | 2.37 | — | ns |
| $t_{HI_PIO}$ | Input Register Hold Time (Data After Clock) | 0.05 | — | 0.05 | — | 0.05 | — | ns |
| $t_{COO_PIO}$ | Output Register Clock to Output Delay | — | 0.36 | — | 0.44 | — | 0.52 | ns |
| $t_{SUCE_PIO}$ | Input Register Clock Enable Setup Time | -0.09 | — | -0.07 | — | -0.06 | — | ns |
| $t_{HCE_PIO}$ | Input Register Clock Enable Hold Time | 0.13 | — | 0.16 | — | 0.19 | — | ns |
| $t_{SULSR_PIO}$ | Set/Reset Setup Time | 0.19 | — | 0.23 | — | 0.28 | — | ns |
| $t_{HLSR_PIO}$ | Set/Reset Hold Time | -0.14 | — | -0.11 | — | -0.09 | — | ns |
| **EBR Timing** | | | | | | | | |
| $t_{CO_EBR}$ | Clock to Output from Address or Data | — | 4.01 | — | 4.81 | — | 5.78 | ns |
| $t_{COO_EBR}$ | Clock to Output from EBR Output Register | — | 0.81 | — | 0.97 | — | 1.17 | ns |
| $t_{SUDATA_EBR}$ | Setup Data to EBR Memory | -0.26 | — | -0.21 | — | -0.17 | — | ns |
| $t_{HDATA_EBR}$ | Hold Data to EBR Memory | 0.41 | — | 0.49 | — | 0.59 | — | ns |
| $t_{SUADDR_EBR}$ | Setup Address to EBR Memory | -0.26 | — | -0.21 | — | -0.17 | — | ns |
| $t_{HADDR_EBR}$ | Hold Address to EBR Memory | 0.41 | — | 0.49 | — | 0.59 | — | ns |
| $t_{SUWREN_EBR}$ | Setup Write/Read Enable to EBR Memory | -0.17 | — | -0.13 | — | -0.11 | — | ns |
| $t_{HWREN_EBR}$ | Hold Write/Read Enable to EBR Memory | 0.26 | — | 0.31 | — | 0.37 | — | ns |
| $t_{SUCE_EBR}$ | Clock Enable Setup Time to EBR Output Register | 0.19 | — | 0.23 | — | 0.28 | — | ns |
| $t_{HCE_EBR}$ | Clock Enable Hold Time to EBR Output Register | -0.13 | — | -0.10 | — | -0.08 | — | ns |

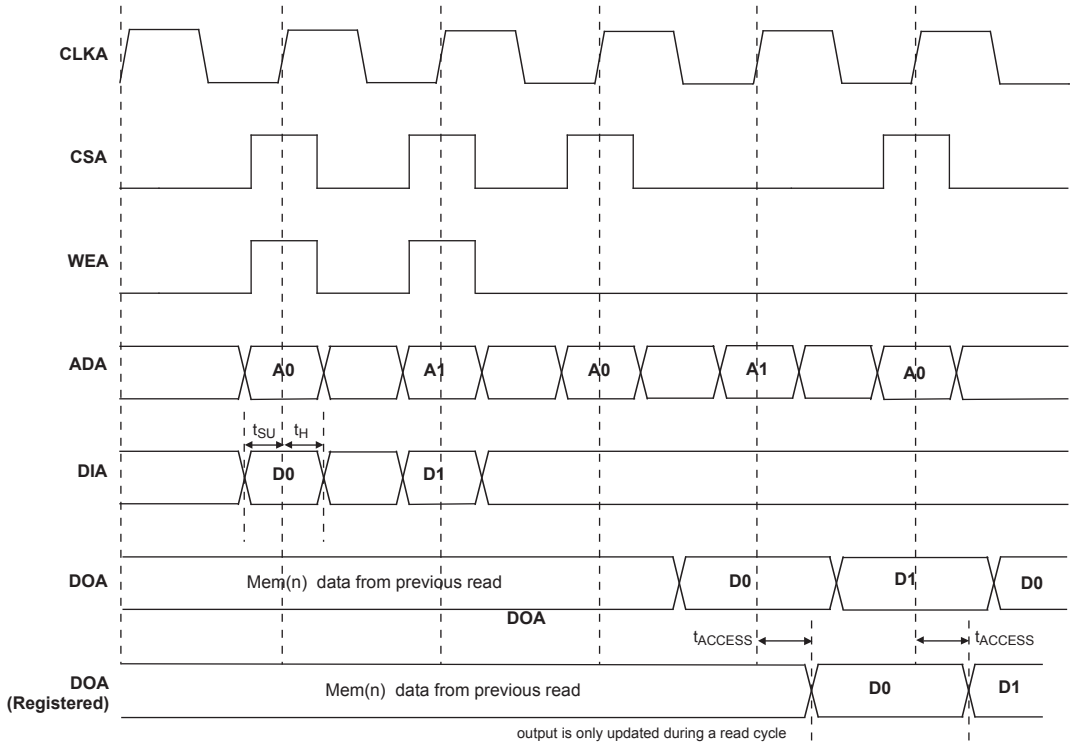
# EBR Memory Timing Diagrams

***Figure 3-8. Read Mode (Normal)***




Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

***Figure 3-9. Read Mode with Input and Output Registers***



# LatticeXP Family Timing Adders[1] (Continued)

**Over Recommended Operating Conditions**

| Buffer Type | Description | -5 | -4 | -3 | Units |
|---|---|---|---|---|---|
| HSTL15_I | HSTL_15 class I | 0.2 | 0.2 | 0.2 | ns |
| HSTL15_III | HSTL_15 class III | 0.2 | 0.2 | 0.2 | ns |
| HSTL15D_I | Differential HSTL 15 class I | 0.2 | 0.2 | 0.2 | ns |
| HSTL15D_III | Differential HSTL 15 class III | 0.2 | 0.2 | 0.2 | ns |
| SSTL33_I | SSTL_3 class I | 0.1 | 0.1 | 0.1 | ns |
| SSTL33_II | SSTL_3 class II | 0.3 | 0.3 | 0.3 | ns |
| SSTL33D_I | Differential SSTL_3 class I | 0.1 | 0.1 | 0.1 | ns |
| SSTL33D_II | Differential SSTL_3 class II | 0.3 | 0.3 | 0.3 | ns |
| SSTL25_I | SSTL_2 class I | -0.1 | -0.1 | -0.1 | ns |
| SSTL25_II | SSTL_2 class II | 0.3 | 0.3 | 0.3 | ns |
| SSTL25D_I | Differential SSTL_2 class I | -0.1 | -0.1 | -0.1 | ns |
| SSTL25D_II | Differential SSTL_2 class II | 0.3 | 0.3 | 0.3 | ns |
| SSTL18_I | SSTL_1.8 class I | 0.1 | 0.1 | 0.1 | ns |
| SSTL18D_I | Differential SSTL_1.8 class I | 0.1 | 0.1 | 0.1 | ns |
| LVTTL33_4mA | LVTTL 4mA drive | 0.8 | 0.8 | 0.8 | ns |
| LVTTL33_8mA | LVTTL 8mA drive | 0.5 | 0.5 | 0.5 | ns |
| LVTTL33_12mA | LVTTL 12mA drive | 0.3 | 0.3 | 0.3 | ns |
| LVTTL33_16mA | LVTTL 16mA drive | 0.4 | 0.4 | 0.4 | ns |
| LVTTL33_20mA | LVTTL 20mA drive | 0.3 | 0.3 | 0.3 | ns |
| LVCMOS33_2mA | LVCMOS 3.3 2mA drive | 0.8 | 0.8 | 0.8 | ns |
| LVCMOS33_4mA | LVCMOS 3.3 4mA drive | 0.8 | 0.8 | 0.8 | ns |
| LVCMOS33_8mA | LVCMOS 3.3 8mA drive | 0.5 | 0.5 | 0.5 | ns |
| LVCMOS33_12mA | LVCMOS 3.3 12mA drive | 0.3 | 0.3 | 0.3 | ns |
| LVCMOS33_16mA | LVCMOS 3.3 16mA drive | 0.4 | 0.4 | 0.4 | ns |
| LVCMOS33_20mA | LVCMOS 3.3 20mA drive | 0.3 | 0.3 | 0.3 | ns |
| LVCMOS25_2mA | LVCMOS 2.5 2mA drive | 0.7 | 0.7 | 0.7 | ns |
| LVCMOS25_4mA | LVCMOS 2.5 4mA drive | 0.7 | 0.7 | 0.7 | ns |
| LVCMOS25_8mA | LVCMOS 2.5 8mA drive | 0.4 | 0.4 | 0.4 | ns |
| LVCMOS25_12mA | LVCMOS 2.5 12mA drive | 0.0 | 0.0 | 0.0 | ns |
| LVCMOS25_16mA | LVCMOS 2.5 16mA drive | 0.2 | 0.2 | 0.2 | ns |
| LVCMOS25_20mA | LVCMOS 2.5 20mA drive | 0.4 | 0.4 | 0.4 | ns |
| LVCMOS18_2mA | LVCMOS 1.8 2mA drive | 0.6 | 0.6 | 0.6 | ns |
| LVCMOS18_4mA | LVCMOS 1.8 4mA drive | 0.6 | 0.6 | 0.6 | ns |
| LVCMOS18_8mA | LVCMOS 1.8 8mA drive | 0.4 | 0.4 | 0.4 | ns |
| LVCMOS18_12mA | LVCMOS 1.8 12mA drive | 0.2 | 0.2 | 0.2 | ns |
| LVCMOS18_16mA | LVCMOS 1.8 16mA drive | 0.2 | 0.2 | 0.2 | ns |
| LVCMOS15_2mA | LVCMOS 1.5 2mA drive | 0.6 | 0.6 | 0.6 | ns |
| LVCMOS15_4mA | LVCMOS 1.5 4mA drive | 0.6 | 0.6 | 0.6 | ns |
| LVCMOS15_8mA | LVCMOS 1.5 8mA drive | 0.2 | 0.2 | 0.2 | ns |
| LVCMOS12_2mA | LVCMOS 1.2 2mA drive | 0.4 | 0.4 | 0.4 | ns |
| LVCMOS12_6mA | LVCMOS 1.2 6mA drive | 0.4 | 0.4 | 0.4 | ns |
| PCI33 | PCI33 | 0.3 | 0.3 | 0.3 | ns |

1. General timing numbers based on LVCMOS 2.5, 12mA.

Timing v.F0.11

# Pin Information Summary[1]

| Pin Type | | XP3 | | | XP6 | | |
|---|---|---|---|---|---|---|---|
| | | 100 TQFP | 144 TQFP | 208 PQFP | 144 TQFP | 208 PQFP | 256 fpBGA |
| Single Ended User I/O | | 62 | 100 | 136 | 100 | 142 | 188 |
| Differential Pair User I/O[2] | | 19 | 35 | 56 | 35 | 58 | 80 |
| Configuration | Dedicated | 11 | 11 | 11 | 11 | 11 | 11 |
| | Muxed | 14 | 14 | 14 | 14 | 14 | 14 |
| TAP | | 5 | 5 | 5 | 5 | 5 | 5 |
| Dedicated (total without supplies) | | 6 | 6 | 6 | 6 | 6 | 6 |
| $V_{CC}$ | | 2 | 4 | 8 | 4 | 8 | 8 |
| $V_{CCAUX}$ | | 2 | 2 | 2 | 2 | 2 | 4 |
| $V_{CCPLL}$ | | 2 | 2 | 2 | 2 | 2 | 2 |
| $V_{CCIO}$ | Bank0 | 1 | 1 | 2 | 1 | 2 | 2 |
| | Bank1 | 1 | 1 | 2 | 1 | 2 | 2 |
| | Bank2 | 1 | 1 | 2 | 1 | 2 | 2 |
| | Bank3 | 1 | 1 | 2 | 1 | 2 | 2 |
| | Bank4 | 1 | 2 | 2 | 2 | 2 | 2 |
| | Bank5 | 1 | 1 | 2 | 1 | 2 | 2 |
| | Bank6 | 1 | 1 | 2 | 1 | 2 | 2 |
| | Bank7 | 1 | 1 | 2 | 1 | 2 | 2 |
| GND | | 10 | 13 | 24 | 13 | 24 | 24 |
| $GND_{PLL}$ | | 2 | 2 | 2 | 2 | 2 | 2 |
| NC | | 0 | 0 | 6 | 0 | 0 | 0 |
| Single Ended/Differential I/O per Bank[2] | Bank0 | 8/2 | 12/3 | 20/8 | 12/3 | 20/8 | 26/11 |
| | Bank1 | 9/0 | 12/2 | 18/6 | 12/2 | 18/6 | 26/11 |
| | Bank2 | 8/3 | 12/5 | 14/6 | 12/5 | 17/7 | 21/9 |
| | Bank3 | 6/2 | 13/5 | 14/6 | 13/5 | 14/6 | 21/9 |
| | Bank4 | 5/2 | 14/6 | 21/9 | 14/6 | 21/9 | 26/11 |
| | Bank5 | 12/4 | 12/4 | 21/9 | 12/4 | 21/9 | 26/11 |
| | Bank6 | 4/2 | 13/5 | 14/6 | 13/5 | 17/7 | 21/9 |
| | Bank7 | 10/4 | 12/5 | 14/6 | 12/5 | 14/6 | 21/9 |
| $V_{CCJ}$ | | 1 | 1 | 1 | 1 | 1 | 1 |

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
2. The differential I/O per bank includes both dedicated LVDS and emulated LVDS pin pairs. Please see the Logic Signal Connections table for more information.

# Pin Information Summary[1] (Cont.)

| Pin Type | | XP10 | | XP15 | | | XP20 | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 256 fpBGA | 388 fpBGA | 256 fpBGA | 388 fpBGA | 484 fpBGA | 256 fpBGA | 388 fpBGA | 484 fpBGA |
| Single Ended User I/O | | 188 | 244 | 188 | 268 | 300 | 188 | 268 | 340 |
| Differential Pair User I/O[2] | | 76 | 104 | 76 | 112 | 128 | 76 | 112 | 144 |
| Configuration | Dedicated | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 11 |
| | Muxed | 14 | 14 | 14 | 14 | 14 | 14 | 14 | 14 |
| TAP | | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| Dedicated (total without supplies) | | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 |
| $V_{CC}$ | | 8 | 14 | 8 | 14 | 28 | 8 | 14 | 28 |
| $V_{CCAUX}$ | | 4 | 4 | 4 | 4 | 12 | 4 | 4 | 12 |
| $V_{CCPLL}$ | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| $V_{CCIO}$ | Bank0 | 2 | 5 | 2 | 5 | 4 | 2 | 5 | 4 |
| | Bank1 | 2 | 5 | 2 | 5 | 4 | 2 | 5 | 4 |
| | Bank2 | 2 | 4 | 2 | 4 | 4 | 2 | 4 | 4 |
| | Bank3 | 2 | 4 | 2 | 4 | 4 | 2 | 4 | 4 |
| | Bank4 | 2 | 5 | 2 | 5 | 4 | 2 | 5 | 4 |
| | Bank5 | 2 | 5 | 2 | 5 | 4 | 2 | 5 | 4 |
| | Bank6 | 2 | 4 | 2 | 4 | 4 | 2 | 4 | 4 |
| | Bank7 | 2 | 4 | 2 | 4 | 4 | 2 | 4 | 4 |
| GND | | 24 | 50 | 24 | 50 | 56 | 24 | 50 | 56 |
| $GND_{PLL}$ | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| NC | | 0 | 24 | 0 | 0 | 40 | 0 | 0 | 0 |
| Single Ended/ Differential I/O per Bank[2] | Bank0 | 26/11 | 33/14 | 26/11 | 39/16 | 40/17 | 26/11 | 39/16 | 47/20 |
| | Bank1 | 26/11 | 33/14 | 26/11 | 39/16 | 40/17 | 26/11 | 39/16 | 47/20 |
| | Bank2 | 21/8 | 28/12 | 21/8 | 28/12 | 35/15 | 21/8 | 28/12 | 38/16 |
| | Bank3 | 21/8 | 28/12 | 21/8 | 28/12 | 35/15 | 21/8 | 28/12 | 38/16 |
| | Bank4 | 26/11 | 33/14 | 26/11 | 39/16 | 40/17 | 26/11 | 39/16 | 47/20 |
| | Bank5 | 26/11 | 33/14 | 26/11 | 39/16 | 40/17 | 26/11 | 39/16 | 47/20 |
| | Bank6 | 21/8 | 28/12 | 21/8 | 28/12 | 35/15 | 21/8 | 28/12 | 38/16 |
| | Bank7 | 21/8 | 28/12 | 21/8 | 28/12 | 35/15 | 21/8 | 28/12 | 38/16 |
| $V_{CCJ}$ | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
2. The differential I/O per bank includes both dedicated LVDS and emulated LVDS pin pairs. Please see the Logic Signal Connections table for more information.

# LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

| Pin Number | LFXP3 | | | | LFXP6 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | Differential | Dual Function | Pin Function | Bank | Differential | Dual Function |
| 47 | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| 48 | PL18B | 6 | C[3] | - | PL26B | 6 | C[3] | - |
| 49 | GND | - | - | - | GND | - | - | - |
| 50 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| 51 | SLEEPN[1]/TOE[2] | - | - | - | SLEEPN[1]/TOE[2] | - | - | - |
| 52 | INITN | 5 | - | - | INITN | 5 | - | - |
| 53 | VCC | - | - | - | VCC | - | - | - |
| 54 | PB2B | 5 | - | VREF1_5 | PB5B | 5 | - | VREF1_5 |
| 55 | PB3A | 5 | T | - | PB6A | 5 | T | DQS |
| 56 | PB3B | 5 | C | - | PB6B | 5 | C | - |
| 57 | PB4A | 5 | T | - | PB7A | 5 | T | - |
| 58 | PB4B | 5 | C | - | PB7B | 5 | C | - |
| 59 | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| 60 | PB5A | 5 | T | - | PB8A | 5 | T | - |
| 61 | PB5B | 5 | C | VREF2_5 | PB8B | 5 | C | VREF2_5 |
| 62 | PB6A | 5 | T | - | PB9A | 5 | T | - |
| 63 | PB6B | 5 | C | - | PB9B | 5 | C | - |
| 64 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| 65 | PB7A | 5 | T | - | PB10A | 5 | T | - |
| 66 | PB7B | 5 | C | - | PB10B | 5 | C | - |
| 67 | PB8A | 5 | T | - | PB11A | 5 | T | - |
| 68 | PB8B | 5 | C | - | PB11B | 5 | C | - |
| 69 | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| 70 | PB9A | 5 | - | - | PB12A | 5 | - | - |
| 71 | PB10B | 5 | - | - | PB13B | 5 | - | - |
| 72 | PB11A | 5 | T | DQS | PB14A | 5 | T | DQS |
| 73 | PB11B | 5 | C | - | PB14B | 5 | C | - |
| 74 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| 75 | PB12A | 5 | T | - | PB15A | 5 | T | - |
| 76 | PB12B | 5 | C | - | PB15B | 5 | C | - |
| 77 | PB13A | 5 | T | - | PB16A | 5 | T | - |
| 78 | PB13B | 5 | C | - | PB16B | 5 | C | - |
| 79 | GND | - | - | - | GND | - | - | - |
| 80 | VCC | - | - | - | VCC | - | - | - |
| 81 | PB14A | 4 | T | - | PB17A | 4 | T | - |
| 82 | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| 83 | PB14B | 4 | C | - | PB17B | 4 | C | - |
| 84 | PB15A | 4 | T | PCLKT4_0 | PB18A | 4 | T | PCLKT4_0 |
| 85 | PB15B | 4 | C | PCLKC4_0 | PB18B | 4 | C | PCLKC4_0 |
| 86 | PB16A | 4 | T | - | PB19A | 4 | T | - |
| 87 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| 88 | PB16B | 4 | C | - | PB19B | 4 | C | - |
| 89 | PB17A | 4 | - | - | PB20A | 4 | - | - |
| 90 | PB18B | 4 | - | - | PB21B | 4 | - | - |
| 91 | PB19A | 4 | T | DQS | PB22A | 4 | T | DQS |
| 92 | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |

# LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

| Pin Number | LFXP3 | | | | LFXP6 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | Differential | Dual Function | Pin Function | Bank | Differential | Dual Function |
| 93 | PB19B | 4 | C | VREF1_4 | PB22B | 4 | C | VREF1_4 |
| 94 | PB20A | 4 | T | - | PB23A | 4 | T | - |
| 95 | PB20B | 4 | C | - | PB23B | 4 | C | - |
| 96 | PB21A | 4 | T | - | PB24A | 4 | T | - |
| 97 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| 98 | PB21B | 4 | C | - | PB24B | 4 | C | - |
| 99 | PB22A | 4 | T | - | PB25A | 4 | T | - |
| 100 | PB22B | 4 | C | - | PB25B | 4 | C | - |
| 101 | PB23A | 4 | T | - | PB26A | 4 | T | - |
| 102 | PB23B | 4 | C | - | PB26B | 4 | C | - |
| 103 | PB24A | 4 | T | VREF2_4 | PB27A | 4 | - | VREF2_4 |
| 104 | PB24B | 4 | C | - | PB30A | 4 | T | DQS |
| 105 | PB25A | 4 | - | - | PB30B | 4 | C | - |
| 106 | GND | - | - | - | GND | - | - | - |
| 107 | VCC | - | - | - | VCC | - | - | - |
| 108 | PR18B | 3 | C[3] | - | PR26B | 3 | C[3] | - |
| 109 | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| 110 | PR18A | 3 | T[3] | - | PR26A | 3 | T[3] | - |
| 111 | PR17B | 3 | C | - | PR25B | 3 | C | - |
| 112 | PR17A | 3 | T | - | PR25A | 3 | T | - |
| 113 | PR16B | 3 | C[3] | - | PR24B | 3 | C[3] | - |
| 114 | PR16A | 3 | T[3] | DQS | PR24A | 3 | T[3] | DQS |
| 115 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| 116 | PR15B | 3 | - | VREF1_3 | PR23B | 3 | - | VREF1_3 |
| 117 | PR14A | 3 | - | VREF2_3 | PR22A | 3 | - | VREF2_3 |
| 118 | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| 119 | PR13B | 3 | C | - | PR21B | 3 | C[3] | - |
| 120 | PR13A | 3 | T | - | PR21A | 3 | T[3] | - |
| 121 | GND | - | - | - | GND | - | - | - |
| 122 | PR12B | 3 | C | - | PR20B | 3 | C | - |
| 123 | PR12A | 3 | T | - | PR20A | 3 | T | - |
| 124 | PR11B | 3 | C | - | PR19B | 3 | C[3] | - |
| 125 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| 126 | PR11A | 3 | T | - | PR19A | 3 | T[3] | - |
| 127 | GNDP1 | - | - | - | GNDP1 | - | - | - |
| 128 | VCCP1 | - | - | - | VCCP1 | - | - | - |
| 129 | NC | - | - | - | PR13A | 2 | - | - |
| 130 | GND | - | - | - | GND | - | - | - |
| 131 | PR9B | 2 | C | PCLKC2_0 | PR12B | 2 | C | PCLKC2_0 |
| 132 | PR9A | 2 | T | PCLKT2_0 | PR12A | 2 | T | PCLKT2_0 |
| 133 | NC | - | - | - | PR11B | 2 | C[3] | - |
| 134 | NC | - | - | - | PR11A | 2 | T[3] | - |
| 135 | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| 136 | PR8B | 2 | C | RUM0_PLLC_IN_A | PR8B | 2 | C | RUM0_PLLC_IN_A |
| 137 | PR8A | 2 | T | RUM0_PLLT_IN_A | PR8A | 2 | T | RUM0_PLLT_IN_A |
| 138 | PR7B | 2 | C[3] | - | PR7B | 2 | C[3] | - |

# LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

| Pin Number | LFXP3 | | | | LFXP6 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | Differential | Dual Function | Pin Function | Bank | Differential | Dual Function |
| 139 | PR7A | 2 | T[3] | DQS | PR7A | 2 | T[3] | DQS |
| 140 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| 141 | PR6B | 2 | - | VREF1_2 | PR6B | 2 | - | VREF1_2 |
| 142 | PR5A | 2 | - | VREF2_2 | PR5A | 2 | - | VREF2_2 |
| 143 | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| 144 | PR4B | 2 | C[3] | - | PR4B | 2 | C[3] | - |
| 145 | PR4A | 2 | T[3] | - | PR4A | 2 | T[3] | - |
| 146 | PR3B | 2 | C | RUM0_PLLC_FB_A | PR3B | 2 | C | RUM0_PLLC_FB_A |
| 147 | PR3A | 2 | T | RUM0_PLLT_FB_A | PR3A | 2 | T | RUM0_PLLT_FB_A |
| 148 | PR2B | 2 | C[3] | - | PR2B | 2 | C[3] | - |
| 149 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| 150 | PR2A | 2 | T[3] | - | PR2A | 2 | T[3] | - |
| 151 | VCC | - | - | - | VCC | - | - | - |
| 152 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| 153 | TDO | - | - | - | TDO | - | - | - |
| 154 | VCCJ | - | - | - | VCCJ | - | - | - |
| 155 | TDI | - | - | - | TDI | - | - | - |
| 156 | TMS | - | - | - | TMS | - | - | - |
| 157 | TCK | - | - | - | TCK | - | - | - |
| 158 | VCC | - | - | - | VCC | - | - | - |
| 159 | PT25A | 1 | - | VREF1_1 | PT28A | 1 | - | VREF1_1 |
| 160 | PT24B | 1 | C | - | PT27B | 1 | C | - |
| 161 | PT24A | 1 | T | - | PT27A | 1 | T | - |
| 162 | PT23A | 1 | - | D0 | PT26A | 1 | - | D0 |
| 163 | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| 164 | PT22B | 1 | C | D1 | PT25B | 1 | C | D1 |
| 165 | PT22A | 1 | T | VREF2_1 | PT25A | 1 | T | VREF2_1 |
| 166 | PT21A | 1 | - | D2 | PT24A | 1 | - | D2 |
| 167 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| 168 | PT20B | 1 | C | D3 | PT23B | 1 | C | D3 |
| 169 | PT20A | 1 | T | - | PT23A | 1 | T | - |
| 170 | PT19B | 1 | C | - | PT22B | 1 | C | - |
| 171 | PT19A | 1 | T | DQS | PT22A | 1 | T | DQS |
| 172 | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| 173 | PT18B | 1 | - | - | PT21B | 1 | - | - |
| 174 | PT17A | 1 | - | D4 | PT20A | 1 | - | D4 |
| 175 | PT16B | 1 | C | - | PT19B | 1 | C | - |
| 176 | PT16A | 1 | T | D5 | PT19A | 1 | T | D5 |
| 177 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| 178 | PT15B | 1 | C | D6 | PT18B | 1 | C | D6 |
| 179 | PT15A | 1 | T | - | PT18A | 1 | T | - |
| 180 | PT14B | 1 | - | D7 | PT17B | 1 | - | D7 |
| 181 | GND | - | - | - | GND | - | - | - |
| 182 | VCC | - | - | - | VCC | - | - | - |
| 183 | PT13B | 0 | C | BUSY | PT16B | 0 | C | BUSY |
| 184 | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |

# LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

| Pin Number | LFXP3 | | | | LFXP6 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | Differential | Dual Function | Pin Function | Bank | Differential | Dual Function |
| 185 | PT13A | 0 | T | CS1N | PT16A | 0 | T | CS1N |
| 186 | PT12B | 0 | C | PCLKC0_0 | PT15B | 0 | C | PCLKC0_0 |
| 187 | PT12A | 0 | T | PCLKT0_0 | PT15A | 0 | T | PCLKT0_0 |
| 188 | PT11B | 0 | C | - | PT14B | 0 | C | - |
| 189 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| 190 | PT11A | 0 | T | DQS | PT14A | 0 | T | DQS |
| 191 | PT10B | 0 | - | - | PT13B | 0 | - | - |
| 192 | PT9A | 0 | - | DOUT | PT12A | 0 | - | DOUT |
| 193 | PT8B | 0 | C | - | PT11B | 0 | C | - |
| 194 | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| 195 | PT8A | 0 | T | WRITEN | PT11A | 0 | T | WRITEN |
| 196 | PT7B | 0 | C | - | PT10B | 0 | C | - |
| 197 | PT7A | 0 | T | VREF1_0 | PT10A | 0 | T | VREF1_0 |
| 198 | PT6B | 0 | C | - | PT9B | 0 | C | - |
| 199 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| 200 | PT6A | 0 | T | DI | PT9A | 0 | T | DI |
| 201 | PT5B | 0 | C | - | PT8B | 0 | C | - |
| 202 | PT5A | 0 | T | CSN | PT8A | 0 | T | CSN |
| 203 | PT4B | 0 | C | - | PT7B | 0 | C | - |
| 204 | PT4A | 0 | T | - | PT7A | 0 | T | - |
| 205 | PT3B | 0 | - | VREF2_0 | PT6B | 0 | - | VREF2_0 |
| 206 | PT2B | 0 | - | - | PT5B | 0 | - | - |
| 207 | GND | - | - | - | GND | - | - | - |
| 208 | CFG0 | 0 | - | - | CFG0 | 0 | - | - |

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

# LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

| | LFXP6 | | | | LFXP10 | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| R8 | PB16A | 5 | T | - | PB20A | 5 | T | - |
| T9 | PB16B | 5 | C | - | PB20B | 5 | C | - |
| R9 | PB17A | 4 | T | - | PB21A | 4 | T | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| P9 | PB17B | 4 | C | - | PB21B | 4 | C | - |
| T10 | PB18A | 4 | T | PCLKT4_0 | PB22A | 4 | T | PCLKT4_0 |
| T11 | PB18B | 4 | C | PCLKC4_0 | PB22B | 4 | C | PCLKC4_0 |
| R10 | PB19A | 4 | T | - | PB23A | 4 | T | - |
| P10 | PB19B | 4 | C | - | PB23B | 4 | C | - |
| N9 | PB20A | 4 | - | - | PB24A | 4 | - | - |
| M9 | PB21B | 4 | - | - | PB25B | 4 | - | - |
| R12 | PB22A | 4 | T | DQS | PB26A | 4 | T | DQS |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| T12 | PB22B | 4 | C | VREF1_4 | PB26B | 4 | C | VREF1_4 |
| P13 | PB23A | 4 | T | - | PB27A | 4 | T | - |
| R13 | PB23B | 4 | C | - | PB27B | 4 | C | - |
| M11 | PB24A | 4 | T | - | PB28A | 4 | T | - |
| N11 | PB24B | 4 | C | - | PB28B | 4 | C | - |
| N10 | PB25A | 4 | T | - | PB29A | 4 | T | - |
| M10 | PB25B | 4 | C | - | PB29B | 4 | C | - |
| T13 | PB26A | 4 | T | - | PB30A | 4 | T | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| P14 | PB26B | 4 | C | - | PB30B | 4 | C | - |
| R11 | PB27A | 4 | T | VREF2_4 | PB31A | 4 | T | VREF2_4 |
| P12 | PB27B | 4 | C | - | PB31B | 4 | C | - |
| T14 | PB28A | 4 | - | - | PB32A | 4 | - | - |
| R14 | PB29B | 4 | - | - | PB33B | 4 | - | - |
| P11 | PB30A | 4 | T | DQS | PB34A | 4 | T | DQS |
| N12 | PB30B | 4 | C | - | PB34B | 4 | C | - |
| T15 | PB31A | 4 | T | - | PB35A | 4 | T | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| R15 | PB31B | 4 | C | - | PB35B | 4 | C | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| P15 | PR26B | 3 | C[3] | - | PR34B | 3 | C | RLM0_PLLC_FB_A |
| N15 | PR26A | 3 | T[3] | - | PR34A | 3 | T | RLM0_PLLT_FB_A |
| P16 | PR24B | 3 | C[3] | - | PR33B | 3 | C[3] | - |
| R16 | PR24A | 3 | T[3] | DQS | PR33A | 3 | T[3] | DQS |
| M15 | PR15B | 3 | - | - | PR32B | 3 | - | - |
| N14 | PR23B | 3 | - | VREF1_3 | PR31A | 3 | - | VREF1_3 |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| M14 | PR25B | 3 | C | - | PR29B | 3 | C | - |
| L13 | PR25A | 3 | T | - | PR29A | 3 | T | - |

## LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

| | LFXP6 | | | | LFXP10 | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| L15 | PR21B | 3 | C[3] | - | PR28B | 3 | C[3] | - |
| L14 | PR21A | 3 | T[3] | - | PR28A | 3 | T[3] | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| L12 | PR17B | 3 | C | - | PR26A | 3 | - | - |
| M16 | PR20B | 3 | C | - | PR25B | 3 | C | RLM0_PLLC_IN_A |
| N16 | PR20A | 3 | T | - | PR25A | 3 | T | RLM0_PLLT_IN_A |
| K14 | PR19B | 3 | C[3] | - | PR24B | 3 | C[3] | - |
| K15 | PR19A | 3 | T[3] | - | PR24A | 3 | T[3] | DQS |
| K12 | PR17A | 3 | T | - | PR23B | 3 | - | - |
| K13 | PR22A | 3 | - | VREF2_3 | PR22A | 3 | - | VREF2_3 |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| L16 | PR18B | 3 | C[3] | - | PR21B | 3 | C[3] | - |
| K16 | PR18A | 3 | T[3] | - | PR21A | 3 | T[3] | - |
| J15 | PR16B | 3 | C[3] | - | PR19B | 3 | C[3] | - |
| J14 | PR16A | 3 | T[3] | - | PR19A | 3 | T[3] | - |
| J13 | GNDP1 | - | - | - | GNDP1 | - | - | - |
| J12 | VCCP1 | - | - | - | VCCP1 | - | - | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| J16 | PR12B | 2 | C | PCLKC2_0 | PR17B | 2 | C | PCLKC2_0 |
| H16 | PR12A | 2 | T | PCLKT2_0 | PR17A | 2 | T | PCLKT2_0 |
| H13 | PR13B | 2 | C[3] | - | PR16B | 2 | C[3] | - |
| H12 | PR13A | 2 | T[3] | - | PR16A | 2 | T[3] | DQS |
| H15 | PR2B | 2 | C[3] | - | PR15B | 2 | - | - |
| H14 | PR6B | 2 | - | VREF1_2 | PR14A | 2 | - | VREF1_2 |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| G15 | PR11B | 2 | C[3] | - | PR13B | 2 | C[3] | - |
| G14 | PR11A | 2 | T[3] | - | PR13A | 2 | T[3] | - |
| G16 | PR8B | 2 | C | RUM0_PLLC_IN_A | PR12B | 2 | C | RUM0_PLLC_IN_A |
| F16 | PR8A | 2 | T | RUM0_PLLT_IN_A | PR12A | 2 | T | RUM0_PLLT_IN_A |
| G13 | PR2A | 2 | T[3] | - | PR11B | 2 | - | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| G12 | PR9B | 2 | C[3] | - | PR8B | 2 | C | - |
| F13 | PR9A | 2 | T[3] | - | PR8A | 2 | T | - |
| B16 | PR7B | 2 | C[3] | - | PR7B | 2 | C[3] | - |
| C16 | PR7A | 2 | T[3] | DQS | PR7A | 2 | T[3] | DQS |
| F15 | PR14A | 2 | - | - | PR6B | 2 | - | - |
| E15 | PR5A | 2 | - | VREF2_2 | PR5A | 2 | - | VREF2_2 |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| F14 | PR4B | 2 | C[3] | - | PR4B | 2 | C[3] | - |
| E14 | PR4A | 2 | T[3] | - | PR4A | 2 | T[3] | - |
| D15 | PR3B | 2 | C | RUM0_PLLC_FB_A | PR3B | 2 | C | RUM0_PLLC_FB_A |
| C15 | PR3A | 2 | T | RUM0_PLLT_FB_A | PR3A | 2 | T | RUM0_PLLT_FB_A |

## LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

| | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| P16 | PR37B | 3 | C[3] | - | PR41B | 3 | C[3] | - |
| R16 | PR37A | 3 | T[3] | DQS | PR41A | 3 | T[3] | DQS |
| M15 | PR36B | 3 | - | - | PR40B | 3 | - | - |
| N14 | PR35A | 3 | - | VREF1_3 | PR39A | 3 | - | VREF1_3 |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| M14 | PR33B | 3 | C | - | PR37B | 3 | C | - |
| L13 | PR33A | 3 | T | - | PR37A | 3 | T | - |
| L15 | PR32B | 3 | C[3] | - | PR36B | 3 | C[3] | - |
| L14 | PR32A | 3 | T[3] | - | PR36A | 3 | T[3] | - |
| L12 | PR30A | 3 | - | - | PR34A | 3 | - | - |
| M16 | PR29B | 3 | C | RLM0_PLLC_IN_A | PR33B | 3 | C | RLM0_PLLC_IN_A |
| N16 | PR29A | 3 | T | RLM0_PLLT_IN_A | PR33A | 3 | T | RLM0_PLLT_IN_A |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| K14 | PR28B | 3 | C[3] | - | PR32B | 3 | C[3] | - |
| K15 | PR28A | 3 | T[3] | DQS | PR32A | 3 | T[3] | DQS |
| K12 | PR27B | 3 | - | - | PR31B | 3 | - | - |
| K13 | PR26A | 3 | - | VREF2_3 | PR30A | 3 | - | VREF2_3 |
| L16 | PR25B | 3 | C[3] | - | PR29B | 3 | C[3] | - |
| K16 | PR25A | 3 | T[3] | - | PR29A | 3 | T[3] | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| J15 | PR23B | 3 | C[3] | - | PR27B | 3 | C[3] | - |
| J14 | PR23A | 3 | T[3] | - | PR27A | 3 | T[3] | - |
| J13 | GNDP1 | - | - | - | GNDP1 | - | - | - |
| J12 | VCCP1 | - | - | - | VCCP1 | - | - | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| J16 | PR21B | 2 | C | PCLKC2_0 | PR21B | 2 | C | PCLKC2_0 |
| H16 | PR21A | 2 | T | PCLKT2_0 | PR21A | 2 | T | PCLKT2_0 |
| H13 | PR20B | 2 | C[3] | - | PR20B | 2 | C[3] | - |
| H12 | PR20A | 2 | T[3] | DQS | PR20A | 2 | T[3] | DQS |
| H15 | PR19B | 2 | - | - | PR19B | 2 | - | - |
| H14 | PR18A | 2 | - | VREF1_2 | PR18A | 2 | - | VREF1_2 |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| G15 | PR17B | 2 | C[3] | - | PR17B | 2 | C[3] | - |
| G14 | PR17A | 2 | T[3] | - | PR17A | 2 | T[3] | - |
| G16 | PR16B | 2 | C | RUM0_PLLC_IN_A | PR16B | 2 | C | RUM0_PLLC_IN_A |
| F16 | PR16A | 2 | T | RUM0_PLLT_IN_A | PR16A | 2 | T | RUM0_PLLT_IN_A |
| G13 | PR15B | 2 | - | - | PR15B | 2 | - | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| G12 | PR12B | 2 | C | - | PR12B | 2 | C | - |
| F13 | PR12A | 2 | T | - | PR12A | 2 | T | - |
| B16 | PR11B | 2 | C[3] | - | PR11B | 2 | C[3] | - |
| C16 | PR11A | 2 | T[3] | DQS | PR11A | 2 | T[3] | DQS |

# LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

| | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| A9 | PT27A | 1 | T | - | PT31A | 1 | T | - |
| C9 | PT26B | 1 | C | D7 | PT30B | 1 | C | D7 |
| C8 | PT26A | 1 | T | - | PT30A | 1 | T | - |
| E9 | PT25B | 0 | C | BUSY | PT29B | 0 | C | BUSY |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| B8 | PT25A | 0 | T | CS1N | PT29A | 0 | T | CS1N |
| A8 | PT24B | 0 | C | PCLKC0_0 | PT28B | 0 | C | PCLKC0_0 |
| A7 | PT24A | 0 | T | PCLKT0_0 | PT28A | 0 | T | PCLKT0_0 |
| B7 | PT23B | 0 | C | - | PT27B | 0 | C | - |
| C7 | PT23A | 0 | T | DQS | PT27A | 0 | T | DQS |
| E8 | PT22B | 0 | - | - | PT26B | 0 | - | - |
| D8 | PT21A | 0 | - | DOUT | PT25A | 0 | - | DOUT |
| A6 | PT20B | 0 | C | - | PT24B | 0 | C | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C6 | PT20A | 0 | T | WRITEN | PT24A | 0 | T | WRITEN |
| E7 | PT19B | 0 | C | - | PT23B | 0 | C | - |
| D7 | PT19A | 0 | T | VREF1_0 | PT23A | 0 | T | VREF1_0 |
| A5 | PT18B | 0 | C | - | PT22B | 0 | C | - |
| B5 | PT18A | 0 | T | DI | PT22A | 0 | T | DI |
| A4 | PT17B | 0 | C | - | PT21B | 0 | C | - |
| B6 | PT17A | 0 | T | CSN | PT21A | 0 | T | CSN |
| E6 | PT16B | 0 | C | - | PT20B | 0 | C | - |
| D6 | PT16A | 0 | T | - | PT20A | 0 | T | - |
| D5 | PT15B | 0 | C | VREF2_0 | PT19B | 0 | C | VREF2_0 |
| A3 | PT15A | 0 | T | DQS | PT19A | 0 | T | DQS |
| B3 | PT14B | 0 | - | - | PT18B | 0 | - | - |
| B2 | PT13A | 0 | - | - | PT17A | 0 | - | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| A2 | PT12B | 0 | C | - | PT16B | 0 | C | - |
| B1 | PT12A | 0 | T | - | PT16A | 0 | T | - |
| F5 | PT11B | 0 | C | - | PT15B | 0 | C | - |
| C5 | PT11A | 0 | T | - | PT15A | 0 | T | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C4 | CFG0 | 0 | - | - | CFG0 | 0 | - | - |
| B4 | CFG1 | 0 | - | - | CFG1 | 0 | - | - |
| C3 | DONE | 0 | - | - | DONE | 0 | - | - |
| A1 | GND | - | - | - | GND | - | - | - |
| A16 | GND | - | - | - | GND | - | - | - |
| F11 | GND | - | - | - | GND | - | - | - |
| F6 | GND | - | - | - | GND | - | - | - |

# LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| L1 | - | - | - | - | PL23A | 7 | T[3] | - |
| M1 | - | - | - | - | PL23B | 7 | C[3] | - |
| M2 | - | - | - | - | PL24A | 7 | - | - |
| L5 | VCCP0 | - | - | - | VCCP0 | - | - | - |
| N2 | GNDP0 | - | - | - | GNDP0 | - | - | - |
| N1 | - | - | - | - | PL25B | 6 | - | - |
| P2 | - | - | - | - | PL26A | 6 | T[3] | - |
| P1 | - | - | - | - | PL26B | 6 | C[3] | - |
| M4 | PL23A | 6 | T[3] | - | PL27A | 6 | T[3] | - |
| M3 | PL23B | 6 | C[3] | - | PL27B | 6 | C[3] | - |
| R2 | PL24A | 6 | T | PCLKT6_0 | PL28A | 6 | T | PCLKT6_0 |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| R1 | PL24B | 6 | C | PCLKC6_0 | PL28B | 6 | C | PCLKC6_0 |
| N3 | PL25A | 6 | T[3] | - | PL29A | 6 | T[3] | - |
| N4 | PL25B | 6 | C[3] | - | PL29B | 6 | C[3] | - |
| M5 | PL26A | 6 | - | - | PL30A | 6 | - | - |
| N5 | PL27B | 6 | - | VREF1_6 | PL31B | 6 | - | VREF1_6 |
| T2 | PL28A | 6 | T[3] | DQS | PL32A | 6 | T[3] | DQS |
| T1 | PL28B | 6 | C[3] | - | PL32B | 6 | C[3] | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| U2 | PL29A | 6 | T | LLM0_PLLT_IN_A | PL33A | 6 | T | LLM0_PLLT_IN_A |
| U1 | PL29B | 6 | C | LLM0_PLLC_IN_A | PL33B | 6 | C | LLM0_PLLC_IN_A |
| P3 | PL30A | 6 | T[3] | - | PL34A | 6 | T[3] | - |
| P4 | PL30B | 6 | C[3] | - | PL34B | 6 | C[3] | - |
| P6 | PL32A | 6 | T[3] | - | PL36A | 6 | T[3] | - |
| P5 | PL32B | 6 | C[3] | - | PL36B | 6 | C[3] | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| V2 | PL33A | 6 | T | - | PL37A | 6 | T | - |
| V1 | PL33B | 6 | C | - | PL37B | 6 | C | - |
| W2 | PL34A | 6 | T[3] | - | PL38A | 6 | T[3] | - |
| W1 | PL34B | 6 | C[3] | - | PL38B | 6 | C[3] | - |
| R3 | PL35A | 6 | - | VREF2_6 | PL39A | 6 | - | VREF2_6 |
| R4 | PL36B | 6 | - | - | PL40B | 6 | - | - |
| R6 | PL37A | 6 | T[3] | DQS | PL41A | 6 | T[3] | DQS |
| R5 | PL37B | 6 | C[3] | - | PL41B | 6 | C[3] | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| Y2 | PL38A | 6 | T | LLM0_PLLT_FB_A | PL42A | 6 | T | LLM0_PLLT_FB_A |
| Y1 | PL38B | 6 | C | LLM0_PLLC_FB_A | PL42B | 6 | C | LLM0_PLLC_FB_A |
| T3 | PL39A | 6 | T[3] | - | PL43A | 6 | T[3] | - |
| T4 | PL39B | 6 | C[3] | - | PL43B | 6 | C[3] | - |
| W3 | PL40A | 6 | T[3] | - | PL44A | 6 | T[3] | - |
| V3 | PL40B | 6 | C[3] | - | PL44B | 6 | C[3] | - |

# LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| H13 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| K15 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| L15 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| L16 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| L17 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| M15 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| M16 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| M17 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| N15 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| R12 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| R13 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| T12 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| U12 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| R10 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| R11 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| T11 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| U11 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| M6 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| M7 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| M8 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| N8 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| K8 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| L6 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| L7 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| L8 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

# Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

## For Further Information

For further information regarding Thermal Management, refer to the following located on the Lattice website at www.latticesemi.com.

- Thermal Management document
- Technical Note TN1052 - Power Estimation and Management for LatticeECP/EC and LatticeXP Devices
- Power Calculator tool included with Lattice's ispLEVER design tool, or as a standalone download from www.latticesemi.com/software

# LatticeXP Family Data Sheet Revision History

November 2007 | Data Sheet DS1001

## Revision History

| Date | Version | Section | Change Summary |
|---|---|---|---|
| February 2005 | 01.0 | — | Initial release. |
| April 2005 | 01.1 | Architecture | EBR memory support section updated with clarification. |
| May 2005 | 01.2 | Introduction | Added TransFR Reconfiguration to Features section. |
| | | Architecture | Added TransFR section. |
| June 2005 | 01.3 | Pinout Information | Added pinout information for LFXP3, LFXP6, LFXP15 and LFXP20. |
| July 2005 | 02.0 | Introduction | Updated XP6, XP15 and XP20 EBR SRAM Bits and Block numbers. |
| | | Architecture | Updated Per Quadrant Primary Clock Selection figure. |
| | | | Added Typical I/O Behavior During Power-up section. |
| | | | Updated Device Configuration section under Configuration and Testing. |
| | | DC and Switching Characteristics | Clarified Hot Socketing Specification |
| | | | Updated Supply Current (Standby) Table |
| | | | Updated Initialization Supply Current Table |
| | | | Added Programming and Erase Flash Supply Current table |
| | | | Added LVDS Emulation section. Updated LVDS25E Output Termination Example figure and LVDS25E DC Conditions table. |
| | | | Updated Differential LVPECL diagram and LVPECL DC Conditions table. |
| | | | Deleted 5V Tolerant Input Buffer section. Updated RSDS figure and RSDS DC Conditions table. |
| | | | Updated sysCONFIG Port Timing Specifications |
| | | | Updated JTAG Port Timing Specifications. Added Flash Download Time table. |
| | | Pinout Information | Updated Signal Descriptions table. |
| | | | Updated Logic Signal Connections Dual Function column. |
| | | Ordering Information | Added lead-free ordering part numbers. |
| July 2005 | 02.1 | DC and Switching Characteristics | Clarification of Flash Programming Junction Temperature |
| August 2005 | 02.2 | Introduction | Added Sleep Mode feature. |
| | | Architecture | Added Sleep Mode section. |
| | | DC and Switching Characteristics | Added Sleep Mode Supply Current Table |
| | | | Added Sleep Mode Timing section |
| | | Pinout Information | Added SLEEPN and TOE signal names, descriptions and footnotes. |
| | | | Added SLEEPN and TOE to pinout information and footnotes. |
| | | | Added footnote 3 to Logic Signal Connections tables for clarification on emulated LVDS output. |
| September 2005 | 03.0 | Architecture | Added clarification of PCI clamp. |
| | | | Added clarification to SLEEPN Pin Characteristics section. |
| | | DC and Switching Characteristics | DC Characteristics, added footnote 4 for clarification. Updated Supply Current (Sleep Mode), Supply Current (Standby), Initialization Supply Current, and Programming and Erase Flash Supply Current typical numbers. |

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