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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15000
Total RAM Bits	331776
Number of I/O	188
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp15e-3fn256i

Slice

Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from adjacent slice or PFU). There are 7 outputs: 6 to routing and one to carry-chain (to adjacent PFU). Table 2-1 lists the signals associated with each slice.

Figure 2-3. Slice Diagram

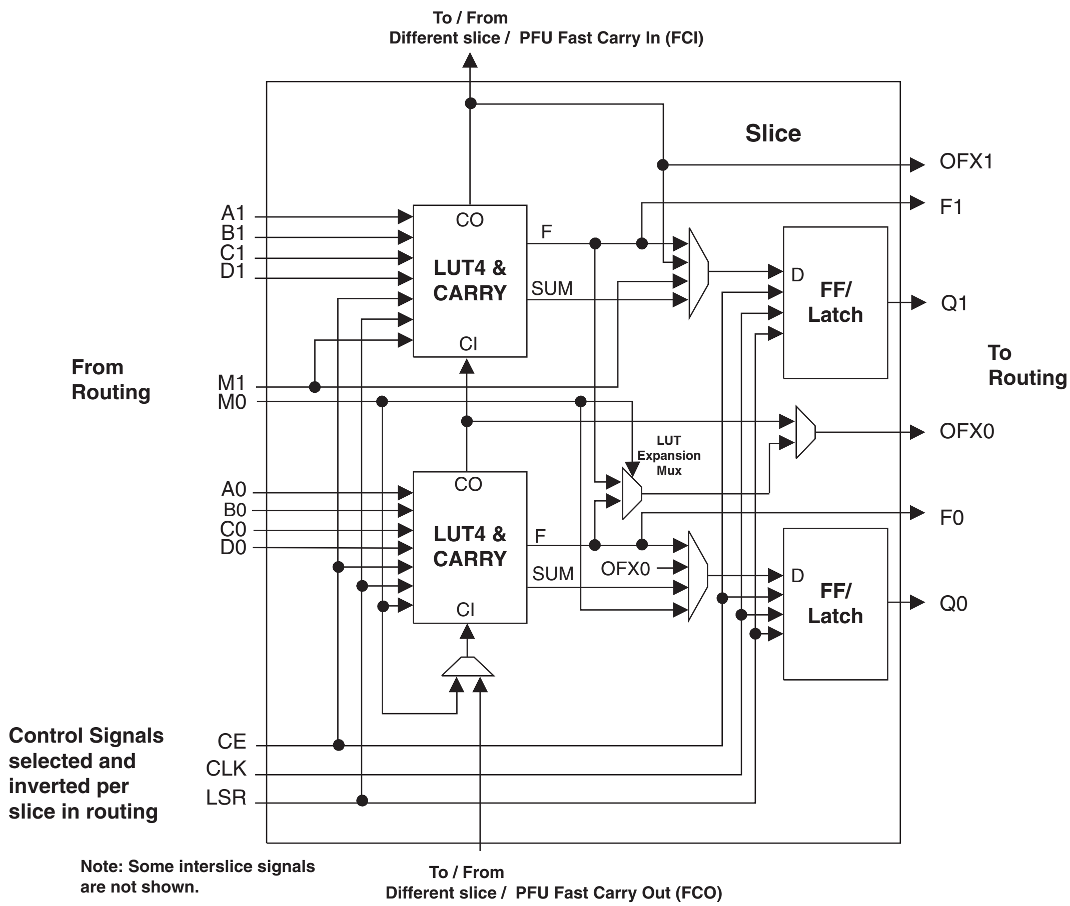
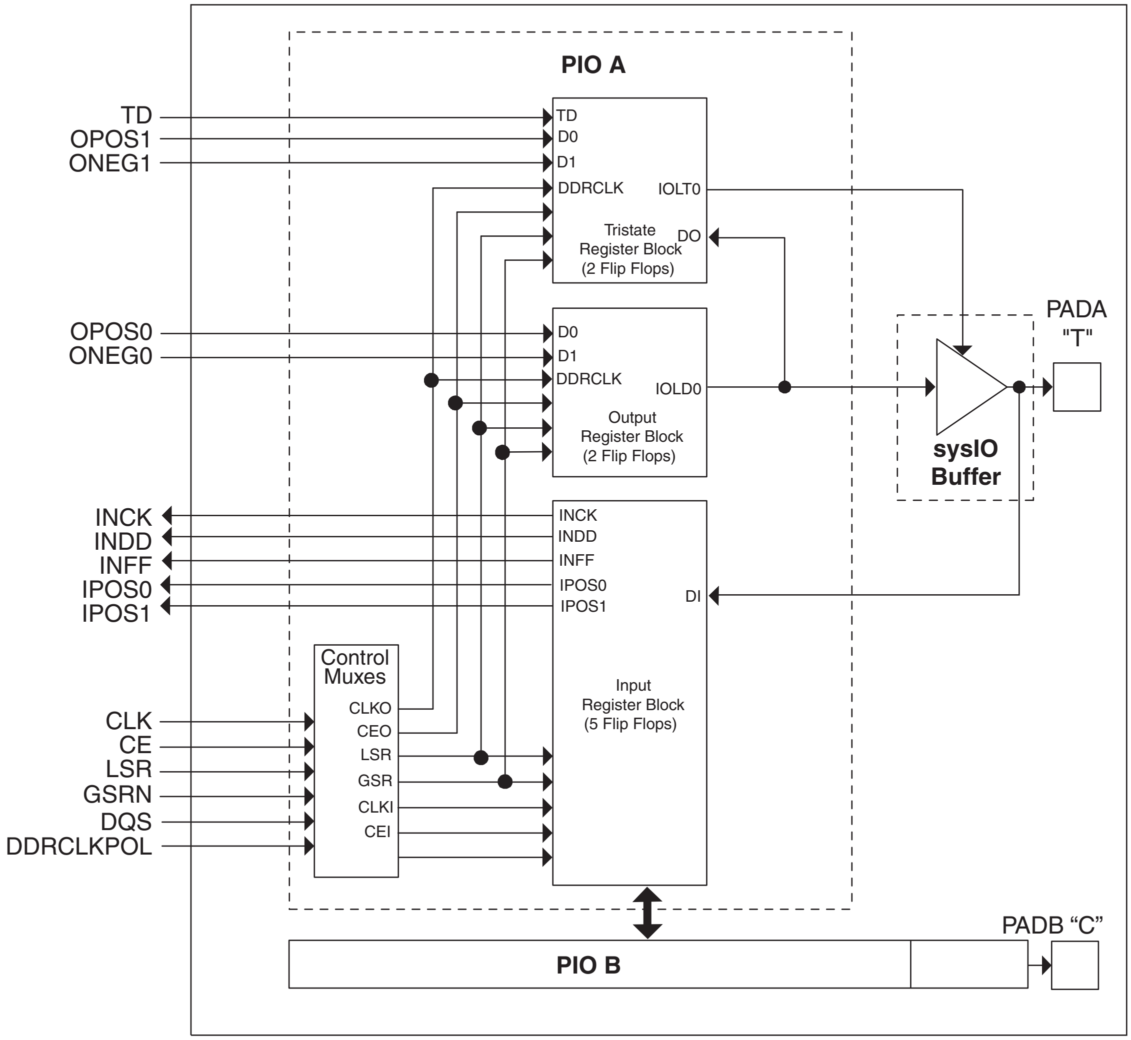


Figure 2-17. PIC Diagram



In the LatticeXP family, seven PIOs or four (3.5) PICs are grouped together to provide two LVDS differential pairs, one PIC pair and one single I/O, as shown in Figure 2-18.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”). The PAD Labels “T” and “C” distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 14 PIOs (a group of 8 PICs) contains a delay element to facilitate the generation of DQS signals as shown in Figure 2-19. The DQS signal feeds the DQS bus which spans the set of 13 PIOs (8 PICs). The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table in this data sheet.

Figure 2-21. Input Register DDR Waveforms

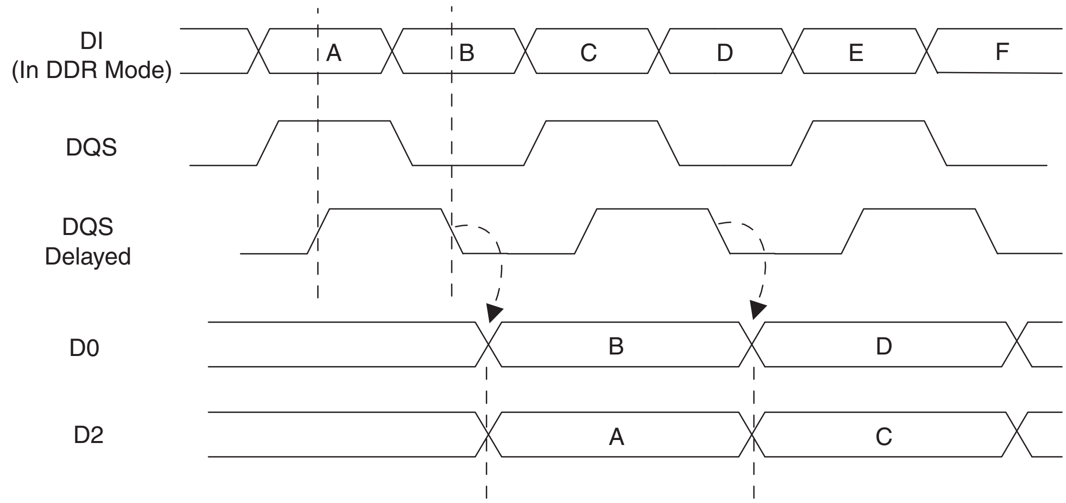
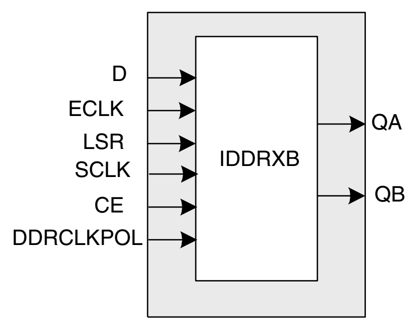


Figure 2-22. INDDRXB Primitive



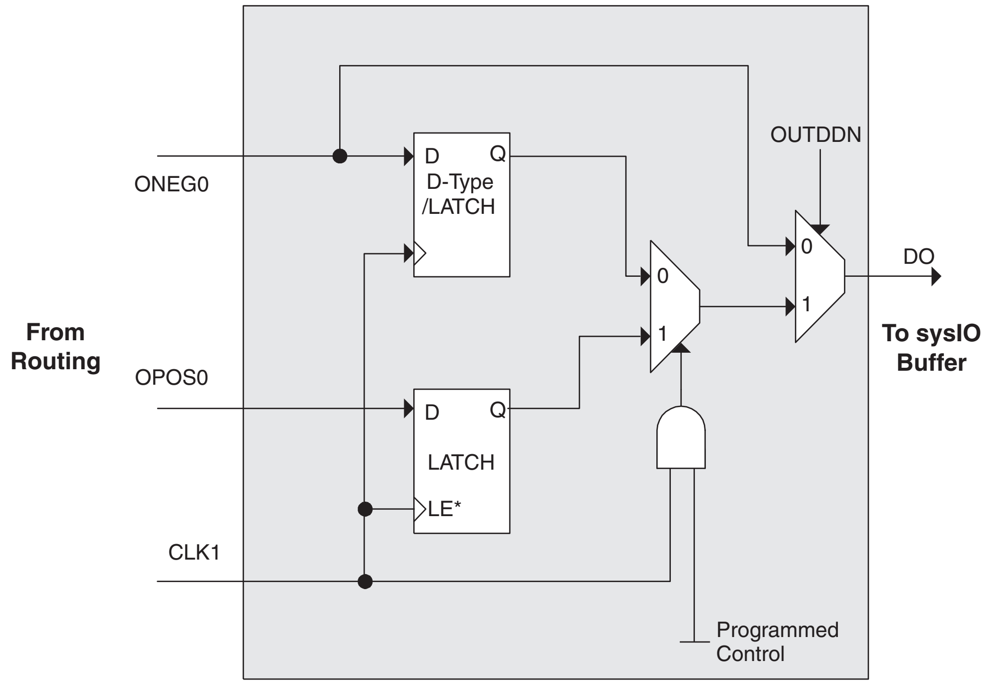
Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-23 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or as a latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

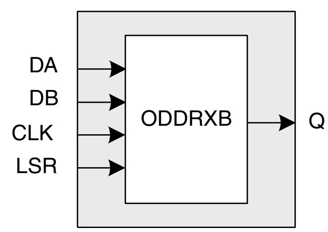
Figure 2-24 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

Figure 2-23. Output Register Block



*Latch is transparent when input is low.

Figure 2-24. ODDRXB Primitive



Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-25 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-29 provides a pictorial representation of the different programming ports and modes available in the LatticeXP devices.

On power-up, the FPGA SRAM is ready to be configured with the sysCONFIG port active. The IEEE 1149.1 serial mode can be activated any time after power-up by sending the appropriate command through the TAP port.

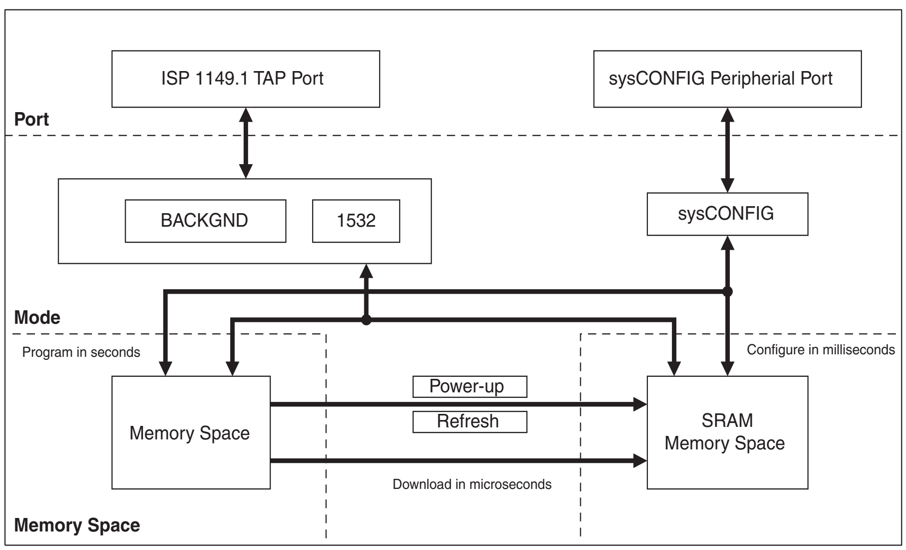
Leave Alone I/O
When using 1532 mode for non-volatile memory programming, users may specify I/Os as high, low, tristated or held at current value. This provides excellent flexibility for implementing systems where reprogramming occurs on-the-fly.

TransFR (Transparent Field Reconfiguration)
TransFR (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. See Lattice technical note #TN1087, *Minimizing System Interruption During Configuration Using TransFR Technology,* for details.

Security
The LatticeXP devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile memory spaces. Once set, the only way to clear security bits is to erase the memory space.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

Figure 2-29. ispXP Block Diagram



Internal Logic Analyzer Capability (ispTRACY)

All LatticeXP devices support an internal logic analyzer diagnostic feature. The diagnostic features provide capabilities similar to an external logic analyzer, such as programmable event and trigger condition and deep trace memory. This feature is enabled by Lattice's ispTRACY. The ispTRACY utility is added into the user design at compile time.

For more information on ispTRACY, please see information regarding additional technical documentation at the end of this data sheet.

Oscillator

Every LatticeXP device has an internal CMOS oscillator which is used to derive a master serial clock for configuration. The oscillator and the master serial clock run continuously in the configuration mode. The default value of the

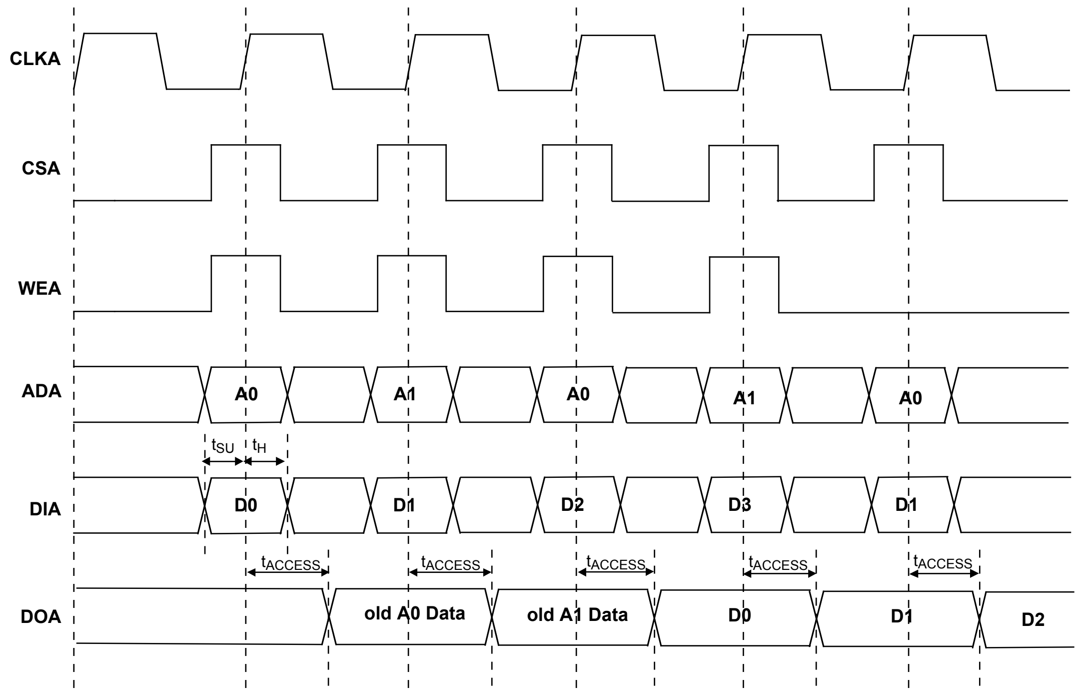
Initialization Supply Current[1, 2, 3, 4, 5, 6]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[7]	Units
I_{CC}	Core Power Supply	LFXP3E	40	mA
		LFXP6E	50	mA
		LFXP10E	110	mA
		LFXP15E	140	mA
		LFXP20E	250	mA
		LFXP3C	60	mA
		LFXP6C	70	mA
		LFXP10C	150	mA
		LFXP15C	180	mA
		LFXP20C	290	mA
I_{CCAUX}	Auxiliary Power Supply V_{CCAUX} = 3.3V	LFXP3E/C	50	mA
		LFXP6E/C	60	mA
		LFXP10E/C	90	mA
		LFXP15 /C	110	mA
		LFXP20E/C	130	mA
I_{CCJ}	V_{CCJ} Power Supply	All	2	mA

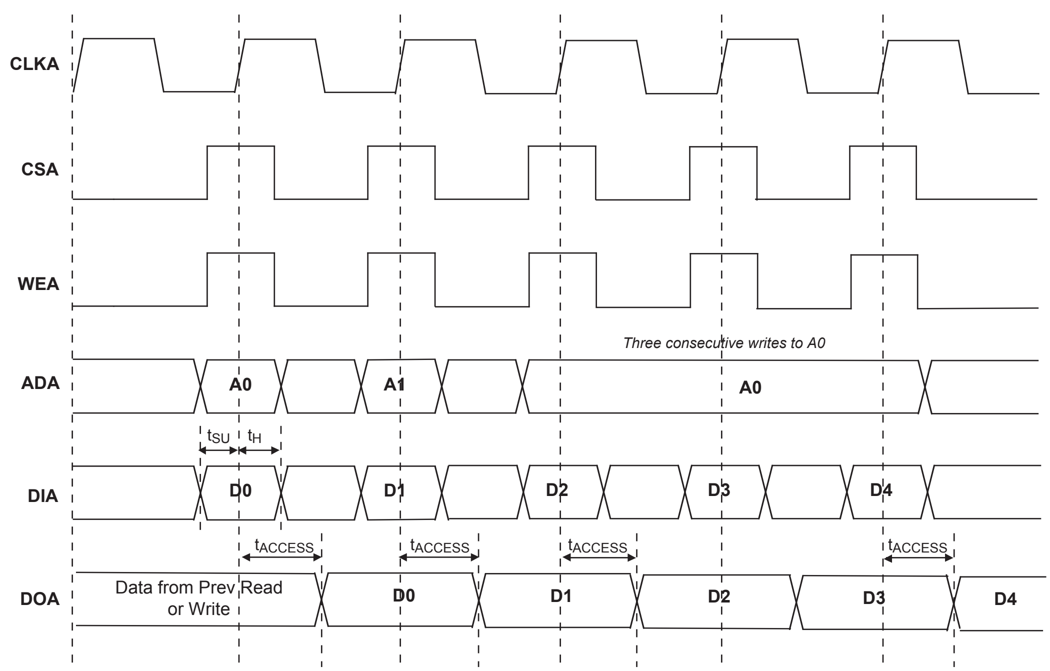
1. Until DONE signal is active.
2. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
4. Frequency 0MHz.
5. Typical user pattern.
6. Assume normal bypass capacitor/decoupling capacitor across the supply.
7. T_A=25°C, power supplies at nominal voltage.

Figure 3-10. Read Before Write (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

Figure 3-11. Write Through (SP Read/Write On Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

Flash Download Time

Symbol	Parameter		Min.	Typ.	Max.	Units
$t_{REFRESH}$	PROGRAMN Low-to-High. Transition to Done High.	LFXP3	—	1.1	1.7	ms
		LFXP6	—	1.4	2.0	ms
		LFXP10	—	0.9	1.5	ms
		LFXP15	—	1.1	1.7	ms
		LFXP20	—	1.3	1.9	ms

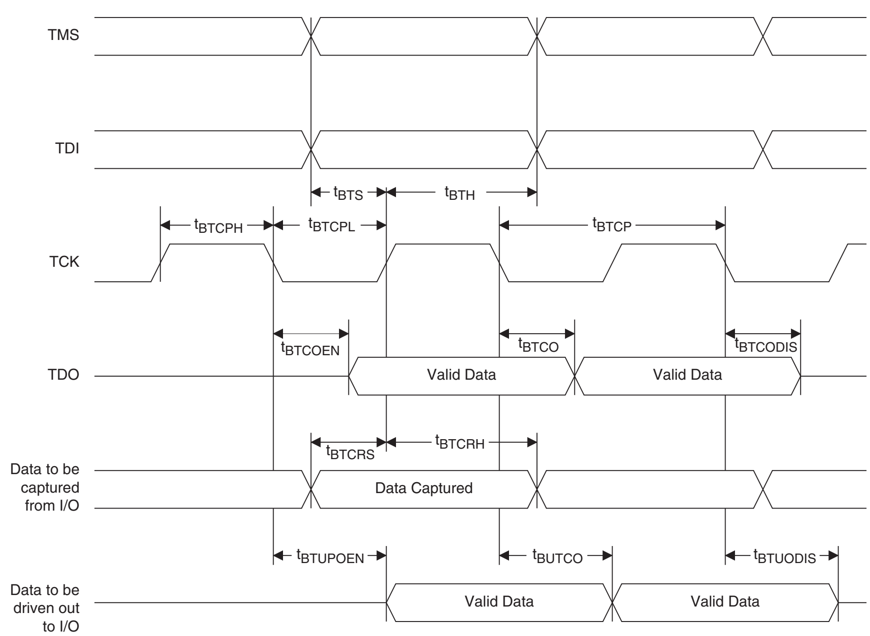
JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f_{MAX}		—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Timing v.F0.11

Figure 3-12. JTAG Port Timing Waveforms



Switching Test Conditions

Figure 3-13 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Figure 3-5.

Figure 3-13. Output Test Load, LVTTL and LVCMOS Standards

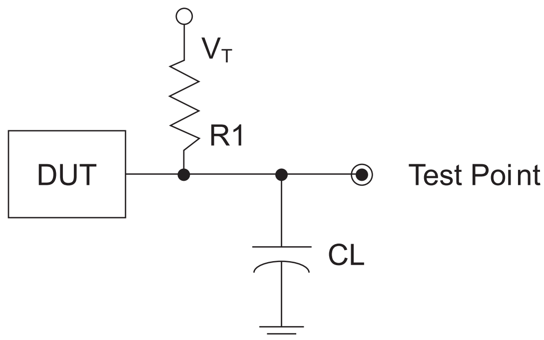


Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	0pF	LVCMOS 3.3 = 1.5V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	188	0pF	$V_{CCIO}/2$	V_{OL}
LVCMOS 2.5 I/O (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVCMOS 2.5 I/O (H -> Z)			V_{OH} - 0.15	V_{OL}
LVCMOS 2.5 I/O (L -> Z)			V_{OL} + 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

LFXP3 Logic Signal Connections: 100 TQFP

Pin Number	Pin Function	Bank	Differential	Dual Function
1	CFG1	0	-	-
2	DONE	0	-	-
3	PROGRAMN	7	-	-
4	CCLK	7	-	-
5	PL3A	7	T	LUM0_PLLT_FB_A
6	PL3B	7	C	LUM0_PLLC_FB_A
7	VCCIO7	7	-	-
8	PL5A	7	-	VREF1_7
9	PL6B	7	-	VREF2_7
10	GNDIO7	7	-	-
11	PL7A	7	T[3]	DQS
12	PL7B	7	C[3]	-
13	PL8A	7	T	LUM0_PLLT_IN_A
14	PL8B	7	C	LUM0_PLLC_IN_A
15	PL9A	7	T[3]	-
16	PL9B	7	C[3]	-
17	VCCP0	-	-	-
18	GNDP0	-	-	-
19	PL12A	6	T	PCLKT6_0
20	PL12B	6	C	PCLKC6_0
21	GNDIO6	6	-	-
22	VCCIO6	6	-	-
23	PL18A	6	T[3]	-
24	PL18B	6	C[3]	-
25	VCCAUX	-	-	-
26	SLEEPN[1]/TOE[2]	-	-	-
27	INITN	5	-	-
28	VCC	-	-	-
29	PB2B	5	-	VREF1_5
30	PB5B	5	-	VREF2_5
31	PB8A	5	T	-
32	PB8B	5	C	-
33	GNDIO5	5	-	-
34	PB9A	5	-	-
35	PB10B	5	-	-
36	PB11A	5	T	DQS
37	PB11B	5	C	-
38	VCCIO5	5	-	-
39	PB12A	5	T	-
40	PB12B	5	C	-
41	PB13A	5	T	-
42	PB13B	5	C	-
43	GND	-	-	-

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
47	GNDIO6	6	-	-	GNDIO6	6	-	-
48	PL18B	6	C[3]	-	PL26B	6	C[3]	-
49	GND	-	-	-	GND	-	-	-
50	VCCAUX	-	-	-	VCCAUX	-	-	-
51	SLEEPN[1]/TOE[2]	-	-	-	SLEEPN[1]/TOE[2]	-	-	-
52	INITN	5	-	-	INITN	5	-	-
53	VCC	-	-	-	VCC	-	-	-
54	PB2B	5	-	VREF1_5	PB5B	5	-	VREF1_5
55	PB3A	5	T	-	PB6A	5	T	DQS
56	PB3B	5	C	-	PB6B	5	C	-
57	PB4A	5	T	-	PB7A	5	T	-
58	PB4B	5	C	-	PB7B	5	C	-
59	GNDIO5	5	-	-	GNDIO5	5	-	-
60	PB5A	5	T	-	PB8A	5	T	-
61	PB5B	5	C	VREF2_5	PB8B	5	C	VREF2_5
62	PB6A	5	T	-	PB9A	5	T	-
63	PB6B	5	C	-	PB9B	5	C	-
64	VCCIO5	5	-	-	VCCIO5	5	-	-
65	PB7A	5	T	-	PB10A	5	T	-
66	PB7B	5	C	-	PB10B	5	C	-
67	PB8A	5	T	-	PB11A	5	T	-
68	PB8B	5	C	-	PB11B	5	C	-
69	GNDIO5	5	-	-	GNDIO5	5	-	-
70	PB9A	5	-	-	PB12A	5	-	-
71	PB10B	5	-	-	PB13B	5	-	-
72	PB11A	5	T	DQS	PB14A	5	T	DQS
73	PB11B	5	C	-	PB14B	5	C	-
74	VCCIO5	5	-	-	VCCIO5	5	-	-
75	PB12A	5	T	-	PB15A	5	T	-
76	PB12B	5	C	-	PB15B	5	C	-
77	PB13A	5	T	-	PB16A	5	T	-
78	PB13B	5	C	-	PB16B	5	C	-
79	GND	-	-	-	GND	-	-	-
80	VCC	-	-	-	VCC	-	-	-
81	PB14A	4	T	-	PB17A	4	T	-
82	GNDIO4	4	-	-	GNDIO4	4	-	-
83	PB14B	4	C	-	PB17B	4	C	-
84	PB15A	4	T	PCLKT4_0	PB18A	4	T	PCLKT4_0
85	PB15B	4	C	PCLKC4_0	PB18B	4	C	PCLKC4_0
86	PB16A	4	T	-	PB19A	4	T	-
87	VCCIO4	4	-	-	VCCIO4	4	-	-
88	PB16B	4	C	-	PB19B	4	C	-
89	PB17A	4	-	-	PB20A	4	-	-
90	PB18B	4	-	-	PB21B	4	-	-
91	PB19A	4	T	DQS	PB22A	4	T	DQS
92	GNDIO4	4	-	-	GNDIO4	4	-	-

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

	LFXP6				LFXP10			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
E8	PT13B	0	-	-	PT17B	0	-	-
D8	PT12A	0	-	DOUT	PT16A	0	-	DOUT
A6	PT11B	0	C	-	PT15B	0	C	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
C6	PT11A	0	T	WRITEN	PT15A	0	T	WRITEN
E7	PT10B	0	C	-	PT14B	0	C	-
D7	PT10A	0	T	VREF1_0	PT14A	0	T	VREF1_0
A5	PT9B	0	C	-	PT13B	0	C	-
B5	PT9A	0	T	DI	PT13A	0	T	DI
A4	PT8B	0	C	-	PT12B	0	C	-
B6	PT8A	0	T	CSN	PT12A	0	T	CSN
E6	PT7B	0	C	-	PT11B	0	C	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
D6	PT7A	0	T	-	PT11A	0	T	-
D5	PT6B	0	C	VREF2_0	PT10B	0	C	VREF2_0
A3	PT6A	0	T	DQS	PT10A	0	T	DQS
B3	PT5B	0	-	-	PT9B	0	-	-
B2	PT4A	0	-	-	PT8A	0	-	-
A2	PT3B	0	C	-	PT7B	0	C	-
B1	PT3A	0	T	-	PT7A	0	T	-
F5	PT2B	0	C	-	PT6B	0	C	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
C5	PT2A	0	T	-	PT6A	0	T	-
C4	CFG0	0	-	-	CFG0	0	-	-
B4	CFG1	0	-	-	CFG1	0	-	-
C3	DONE	0	-	-	DONE	0	-	-
A1	GND	-	-	-	GND	-	-	-
A16	GND	-	-	-	GND	-	-	-
F11	GND	-	-	-	GND	-	-	-
F6	GND	-	-	-	GND	-	-	-
G10	GND	-	-	-	GND	-	-	-
G7	GND	-	-	-	GND	-	-	-
G8	GND	-	-	-	GND	-	-	-
G9	GND	-	-	-	GND	-	-	-
H10	GND	-	-	-	GND	-	-	-
H7	GND	-	-	-	GND	-	-	-
H8	GND	-	-	-	GND	-	-	-
H9	GND	-	-	-	GND	-	-	-
J10	GND	-	-	-	GND	-	-	-
J7	GND	-	-	-	GND	-	-	-
J8	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15 Ball Function	LFXP15 Bank	LFXP15 Differential	LFXP15 Dual Function	LFXP20 Ball Function	LFXP20 Bank	LFXP20 Differential	LFXP20 Dual Function
P16	PR37B	3	C[3]	-	PR41B	3	C[3]	-
R16	PR37A	3	T[3]	DQS	PR41A	3	T[3]	DQS
M15	PR36B	3	-	-	PR40B	3	-	-
N14	PR35A	3	-	VREF1_3	PR39A	3	-	VREF1_3
-	GNDIO3	3	-	-	GNDIO3	3	-	-
M14	PR33B	3	C	-	PR37B	3	C	-
L13	PR33A	3	T	-	PR37A	3	T	-
L15	PR32B	3	C[3]	-	PR36B	3	C[3]	-
L14	PR32A	3	T[3]	-	PR36A	3	T[3]	-
L12	PR30A	3	-	-	PR34A	3	-	-
M16	PR29B	3	C	RLM0_PLLC_IN_A	PR33B	3	C	RLM0_PLLC_IN_A
N16	PR29A	3	T	RLM0_PLLT_IN_A	PR33A	3	T	RLM0_PLLT_IN_A
-	GNDIO3	3	-	-	GNDIO3	3	-	-
K14	PR28B	3	C[3]	-	PR32B	3	C[3]	-
K15	PR28A	3	T[3]	DQS	PR32A	3	T[3]	DQS
K12	PR27B	3	-	-	PR31B	3	-	-
K13	PR26A	3	-	VREF2_3	PR30A	3	-	VREF2_3
L16	PR25B	3	C[3]	-	PR29B	3	C[3]	-
K16	PR25A	3	T[3]	-	PR29A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
J15	PR23B	3	C[3]	-	PR27B	3	C[3]	-
J14	PR23A	3	T[3]	-	PR27A	3	T[3]	-
J13	GNDP1	-	-	-	GNDP1	-	-	-
J12	VCCP1	-	-	-	VCCP1	-	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
J16	PR21B	2	C	PCLKC2_0	PR21B	2	C	PCLKC2_0
H16	PR21A	2	T	PCLKT2_0	PR21A	2	T	PCLKT2_0
H13	PR20B	2	C[3]	-	PR20B	2	C[3]	-
H12	PR20A	2	T[3]	DQS	PR20A	2	T[3]	DQS
H15	PR19B	2	-	-	PR19B	2	-	-
H14	PR18A	2	-	VREF1_2	PR18A	2	-	VREF1_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G15	PR17B	2	C[3]	-	PR17B	2	C[3]	-
G14	PR17A	2	T[3]	-	PR17A	2	T[3]	-
G16	PR16B	2	C	RUM0_PLLC_IN_A	PR16B	2	C	RUM0_PLLC_IN_A
F16	PR16A	2	T	RUM0_PLLT_IN_A	PR16A	2	T	RUM0_PLLT_IN_A
G13	PR15B	2	-	-	PR15B	2	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G12	PR12B	2	C	-	PR12B	2	C	-
F13	PR12A	2	T	-	PR12A	2	T	-
B16	PR11B	2	C[3]	-	PR11B	2	C[3]	-
C16	PR11A	2	T[3]	DQS	PR11A	2	T[3]	DQS

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15 Ball Function	LFXP15 Bank	LFXP15 Differential	LFXP15 Dual Function	LFXP20 Ball Function	LFXP20 Bank	LFXP20 Differential	LFXP20 Dual Function
A9	PT27A	1	T	-	PT31A	1	T	-
C9	PT26B	1	C	D7	PT30B	1	C	D7
C8	PT26A	1	T	-	PT30A	1	T	-
E9	PT25B	0	C	BUSY	PT29B	0	C	BUSY
-	GNDIO0	0	-	-	GNDIO0	0	-	-
B8	PT25A	0	T	CS1N	PT29A	0	T	CS1N
A8	PT24B	0	C	PCLKC0_0	PT28B	0	C	PCLKC0_0
A7	PT24A	0	T	PCLKT0_0	PT28A	0	T	PCLKT0_0
B7	PT23B	0	C	-	PT27B	0	C	-
C7	PT23A	0	T	DQS	PT27A	0	T	DQS
E8	PT22B	0	-	-	PT26B	0	-	-
D8	PT21A	0	-	DOUT	PT25A	0	-	DOUT
A6	PT20B	0	C	-	PT24B	0	C	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
C6	PT20A	0	T	WRITEN	PT24A	0	T	WRITEN
E7	PT19B	0	C	-	PT23B	0	C	-
D7	PT19A	0	T	VREF1_0	PT23A	0	T	VREF1_0
A5	PT18B	0	C	-	PT22B	0	C	-
B5	PT18A	0	T	DI	PT22A	0	T	DI
A4	PT17B	0	C	-	PT21B	0	C	-
B6	PT17A	0	T	CSN	PT21A	0	T	CSN
E6	PT16B	0	C	-	PT20B	0	C	-
D6	PT16A	0	T	-	PT20A	0	T	-
D5	PT15B	0	C	VREF2_0	PT19B	0	C	VREF2_0
A3	PT15A	0	T	DQS	PT19A	0	T	DQS
B3	PT14B	0	-	-	PT18B	0	-	-
B2	PT13A	0	-	-	PT17A	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
A2	PT12B	0	C	-	PT16B	0	C	-
B1	PT12A	0	T	-	PT16A	0	T	-
F5	PT11B	0	C	-	PT15B	0	C	-
C5	PT11A	0	T	-	PT15A	0	T	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
C4	CFG0	0	-	-	CFG0	0	-	-
B4	CFG1	0	-	-	CFG1	0	-	-
C3	DONE	0	-	-	DONE	0	-	-
A1	GND	-	-	-	GND	-	-	-
A16	GND	-	-	-	GND	-	-	-
F11	GND	-	-	-	GND	-	-	-
F6	GND	-	-	-	GND	-	-	-

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L7	VCCIO5	5	-	-	VCCIO5	5	-	-
L8	VCCIO5	5	-	-	VCCIO5	5	-	-
J6	VCCIO6	6	-	-	VCCIO6	6	-	-
K6	VCCIO6	6	-	-	VCCIO6	6	-	-
G6	VCCIO7	7	-	-	VCCIO7	7	-	-
H6	VCCIO7	7	-	-	VCCIO7	7	-	-

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

	LFXP10				LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
A7	PT13A	0	T	DI	PT18A	0	T	DI	PT22A	0	T	DI
B7	PT12B	0	C	-	PT17B	0	C	-	PT21B	0	C	-
C6	PT12A	0	T	CSN	PT17A	0	T	CSN	PT21A	0	T	CSN
C10	PT11B	0	C	-	PT16B	0	C	-	PT20B	0	C	-
C9	PT11A	0	T	-	PT16A	0	T	-	PT20A	0	T	-
A6	PT10B	0	C	VREF2_0	PT15B	0	C	VREF2_0	PT19B	0	C	VREF2_0
B6	PT10A	0	T	DQS	PT15A	0	T	DQS	PT19A	0	T	DQS
A5	PT9B	0	-	-	PT14B	0	-	-	PT18B	0	-	-
B5	PT8A	0	-	-	PT13A	0	-	-	PT17A	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C5	PT7B	0	C	-	PT12B	0	C	-	PT16B	0	C	-
A4	PT7A	0	T	-	PT12A	0	T	-	PT16A	0	T	-
D9	PT6B	0	C	-	PT11B	0	C	-	PT15B	0	C	-
D8	PT6A	0	T	-	PT11A	0	T	-	PT15A	0	T	-
B4	PT5B	0	C	-	PT10B	0	C	-	PT14B	0	C	-
A2	PT5A	0	T	-	PT10A	0	T	-	PT14A	0	T	-
A3	PT4B	0	C	-	PT9B	0	C	-	PT13B	0	C	-
B3	PT4A	0	T	-	PT9A	0	T	-	PT13A	0	T	-
C4	PT3B	0	C	-	PT8B	0	C	-	PT12B	0	C	-
C3	PT3A	0	T	-	PT8A	0	T	-	PT12A	0	T	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C2	-	-	-	-	PT7B	0	C	-	PT11B	0	C	-
D3	PT2A	0	-	-	PT7A	0	T	DQS	PT11A	0	T	DQS
D7	-	-	-	-	PT6B	0	-	-	PT10B	0	-	-
D6	-	-	-	-	PT5A	0	-	-	PT9A	0	-	-
E4	-	-	-	-	PT4B	0	C	-	PT8B	0	C	-
D4	-	-	-	-	PT4A	0	T	-	PT8A	0	T	-
D5	-	-	-	-	PT3B	0	-	-	PT7B	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C1	CFG0	0	-	-	CFG0	0	-	-	CFG0	0	-	-
B2	CFG1	0	-	-	CFG1	0	-	-	CFG1	0	-	-
B1	DONE	0	-	-	DONE	0	-	-	DONE	0	-	-
A1	GND	-	-	-	GND	-	-	-	GND	-	-	-
A22	GND	-	-	-	GND	-	-	-	GND	-	-	-
AB1	GND	-	-	-	GND	-	-	-	GND	-	-	-
AB22	GND	-	-	-	GND	-	-	-	GND	-	-	-
H10	GND	-	-	-	GND	-	-	-	GND	-	-	-
H11	GND	-	-	-	GND	-	-	-	GND	-	-	-
H12	GND	-	-	-	GND	-	-	-	GND	-	-	-
H13	GND	-	-	-	GND	-	-	-	GND	-	-	-
H14	GND	-	-	-	GND	-	-	-	GND	-	-	-
J10	GND	-	-	-	GND	-	-	-	GND	-	-	-
J11	GND	-	-	-	GND	-	-	-	GND	-	-	-
J12	GND	-	-	-	GND	-	-	-	GND	-	-	-
J13	GND	-	-	-	GND	-	-	-	GND	-	-	-
J14	GND	-	-	-	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-	GND	-	-	-
K10	GND	-	-	-	GND	-	-	-	GND	-	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

	LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
R18	PR38B	3	C	RLM0_PLLC_FB_A	PR42B	3	C	RLM0_PLLC_FB_A
R17	PR38A	3	T	RLM0_PLLT_FB_A	PR42A	3	T	RLM0_PLLT_FB_A
Y22	PR37B	3	C[3]	-	PR41B	3	C[3]	-
Y21	PR37A	3	T[3]	DQS	PR41A	3	T[3]	DQS
W22	PR36B	3	-	-	PR40B	3	-	-
W21	PR35A	3	-	VREF1_3	PR39A	3	-	VREF1_3
P17	PR34B	3	C[3]	-	PR38B	3	C[3]	-
P18	PR34A	3	T[3]	-	PR38A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
R19	PR33B	3	C	-	PR37B	3	C	-
R20	PR33A	3	T	-	PR37A	3	T	-
V22	PR32B	3	C[3]	-	PR36B	3	C[3]	-
V21	PR32A	3	T[3]	-	PR36A	3	T[3]	-
U22	PR30B	3	C[3]	-	PR34B	3	C[3]	-
U21	PR30A	3	T[3]	-	PR34A	3	T[3]	-
P19	PR29B	3	C	RLM0_PLLC_IN_A	PR33B	3	C	RLM0_PLLC_IN_A
P20	PR29A	3	T	RLM0_PLLT_IN_A	PR33A	3	T	RLM0_PLLT_IN_A
-	GNDIO3	3	-	-	GNDIO3	3	-	-
T22	PR28B	3	C[3]	-	PR32B	3	C[3]	-
T21	PR28A	3	T[3]	DQS	PR32A	3	T[3]	DQS
R22	PR27B	3	-	-	PR31B	3	-	-
R21	PR26A	3	-	VREF2_3	PR30A	3	-	VREF2_3
N19	PR25B	3	C[3]	-	PR29B	3	C[3]	-
N20	PR25A	3	T[3]	-	PR29A	3	T[3]	-
N18	PR24B	3	C	-	PR28B	3	C	-
M18	PR24A	3	T	-	PR28A	3	T	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
P22	PR23B	3	C[3]	-	PR27B	3	C[3]	-
P21	PR23A	3	T[3]	-	PR27A	3	T[3]	-
N22	-	-	-	-	PR26B	3	C[3]	-
N21	-	-	-	-	PR26A	3	T[3]	-
M19	-	-	-	-	PR25B	3	-	-
M20	GNDP1	-	-	-	GNDP1	-	-	-
L18	VCCP1	-	-	-	VCCP1	-	-	-
M21	-	-	-	-	PR24A	2	-	-
M22	PR22B	2	C[3]	-	PR23B	2	C[3]	-
L22	PR22A	2	T[3]	-	PR23A	2	T[3]	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
L19	-	-	-	-	PR22B	2	C[3]	-
L20	-	-	-	-	PR22A	2	T[3]	-
L21	PR21B	2	C	PCLKC2_0	PR21B	2	C	PCLKC2_0
K22	PR21A	2	T	PCLKT2_0	PR21A	2	T	PCLKT2_0

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

	LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
J15	GND	-	-	-	GND	-	-	-
J8	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-
K10	GND	-	-	-	GND	-	-	-
K11	GND	-	-	-	GND	-	-	-
K12	GND	-	-	-	GND	-	-	-
K13	GND	-	-	-	GND	-	-	-
K14	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-
L10	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-
L12	GND	-	-	-	GND	-	-	-
L13	GND	-	-	-	GND	-	-	-
L14	GND	-	-	-	GND	-	-	-
L9	GND	-	-	-	GND	-	-	-
M10	GND	-	-	-	GND	-	-	-
M11	GND	-	-	-	GND	-	-	-
M12	GND	-	-	-	GND	-	-	-
M13	GND	-	-	-	GND	-	-	-
M14	GND	-	-	-	GND	-	-	-
M9	GND	-	-	-	GND	-	-	-
N10	GND	-	-	-	GND	-	-	-
N11	GND	-	-	-	GND	-	-	-
N12	GND	-	-	-	GND	-	-	-
N13	GND	-	-	-	GND	-	-	-
N14	GND	-	-	-	GND	-	-	-
N9	GND	-	-	-	GND	-	-	-
P10	GND	-	-	-	GND	-	-	-
P11	GND	-	-	-	GND	-	-	-
P12	GND	-	-	-	GND	-	-	-
P13	GND	-	-	-	GND	-	-	-
P14	GND	-	-	-	GND	-	-	-
P15	GND	-	-	-	GND	-	-	-
P8	GND	-	-	-	GND	-	-	-
P9	GND	-	-	-	GND	-	-	-
R14	GND	-	-	-	GND	-	-	-
R9	GND	-	-	-	GND	-	-	-
F10	VCC	-	-	-	VCC	-	-	-
F13	VCC	-	-	-	VCC	-	-	-
G10	VCC	-	-	-	VCC	-	-	-
G13	VCC	-	-	-	VCC	-	-	-
G14	VCC	-	-	-	VCC	-	-	-

Commercial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6E-3F256C	188	1.2V	-3	fpBGA	256	COM	5.8K
LFXP6E-4F256C	188	1.2V	-4	fpBGA	256	COM	5.8K
LFXP6E-5F256C	188	1.2V	-5	fpBGA	256	COM	5.8K
LFXP6E-3Q208C	142	1.2V	-3	PQFP	208	COM	5.8K
LFXP6E-4Q208C	142	1.2V	-4	PQFP	208	COM	5.8K
LFXP6E-5Q208C	142	1.2V	-5	PQFP	208	COM	5.8K
LFXP6E-3T144C	100	1.2V	-3	TQFP	144	COM	5.8K
LFXP6E-4T144C	100	1.2V	-4	TQFP	144	COM	5.8K
LFXP6E-5T144C	100	1.2V	-5	TQFP	144	COM	5.8K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10E-3F388C	244	1.2V	-3	fpBGA	388	COM	9.7K
LFXP10E-4F388C	244	1.2V	-4	fpBGA	388	COM	9.7K
LFXP10E-5F388C	244	1.2V	-5	fpBGA	388	COM	9.7K
LFXP10E-3F256C	188	1.2V	-3	fpBGA	256	COM	9.7K
LFXP10E-4F256C	188	1.2V	-4	fpBGA	256	COM	9.7K
LFXP10E-5F256C	188	1.2V	-5	fpBGA	256	COM	9.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15E-3F484C	300	1.2V	-3	fpBGA	484	COM	15.5K
LFXP15E-4F484C	300	1.2V	-4	fpBGA	484	COM	15.5K
LFXP15E-5F484C	300	1.2V	-5	fpBGA	484	COM	15.5K
LFXP15E-3F388C	268	1.2V	-3	fpBGA	388	COM	15.5K
LFXP15E-4F388C	268	1.2V	-4	fpBGA	388	COM	15.5K
LFXP15E-5F388C	268	1.2V	-5	fpBGA	388	COM	15.5K
LFXP15E-3F256C	188	1.2V	-3	fpBGA	256	COM	15.5K
LFXP15E-4F256C	188	1.2V	-4	fpBGA	256	COM	15.5K
LFXP15E-5F256C	188	1.2V	-5	fpBGA	256	COM	15.5K

LatticeXP Family Data Sheet Supplemental Information

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For Further Information

A variety of technical notes for the LatticeXP family are available on the Lattice website at www.latticesemi.com.

- LatticeECP/EC and LatticeXP sysIO Usage Guide (TN1056)
- Lattice ispTRACY Usage Guide (TN1054)
- LatticeECP/EC and LatticeXP sysCLOCK PLL Design and Usage Guide (TN1049)
- Memory Usage Guide for LatticeECP/EC and LatticeXP Devices (TN1051)
- LatticeECP/EC and XP DDR Usage Guide (TN1050)
- Power Estimation and Management for LatticeECP/EC and LatticeXP Devices (TN1052)
- LatticeXP sysCONFIG Usage Guide (TN1082)

For further information on interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com