



Welcome to [E-XFL.COM](#)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15000
Total RAM Bits	331776
Number of I/O	268
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	388-BBGA
Supplier Device Package	388-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp15e-5f388c

Introduction

The LatticeXP family of FPGA devices combine logic gates, embedded memory and high performance I/Os in a single architecture that is both non-volatile and infinitely reconfigurable to support cost-effective system designs.

The re-programmable non-volatile technology used in the LatticeXP family is the next generation ispXP™ technology. With this technology, expensive external configuration memories are not required and designs are secured from unauthorized read-back. In addition, instant-on capability allows for easy interfacing in many applications.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeXP family of FPGA devices. Synthesis library support for LatticeXP is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeXP device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeXP family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In ¹
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output ¹

1. See Figure 2-2 for connection details.

2. Requires two PFUs.

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SP 16x2	ROM 16x1 x 2
PFF Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	N/A	ROM 16x1 x 2

Logic Mode: In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other Slices.

Ripple Mode: Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Two additional signals: Carry Generate and Carry Propagate are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode: In this mode, distributed RAM can be constructed using each LUT block as a 16x1-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

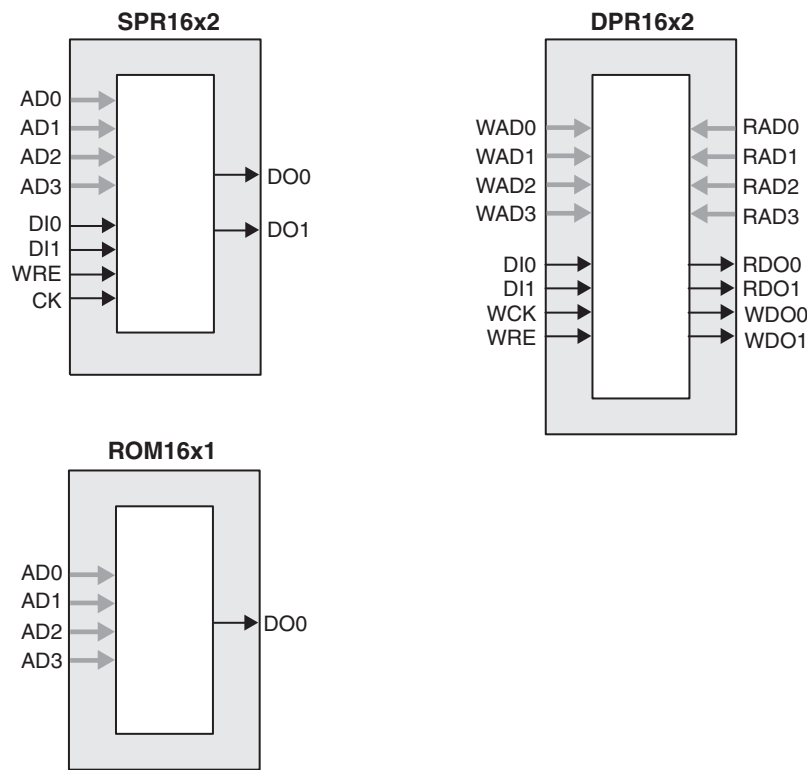
The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-4 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices, one Slice functions as the read-write port. The other companion Slice supports the read-only port. For more information on RAM mode in LatticeXP devices, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required for Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of Slices	1	2

Note: SPR = Single Port RAM, DPR = Dual Port RAM

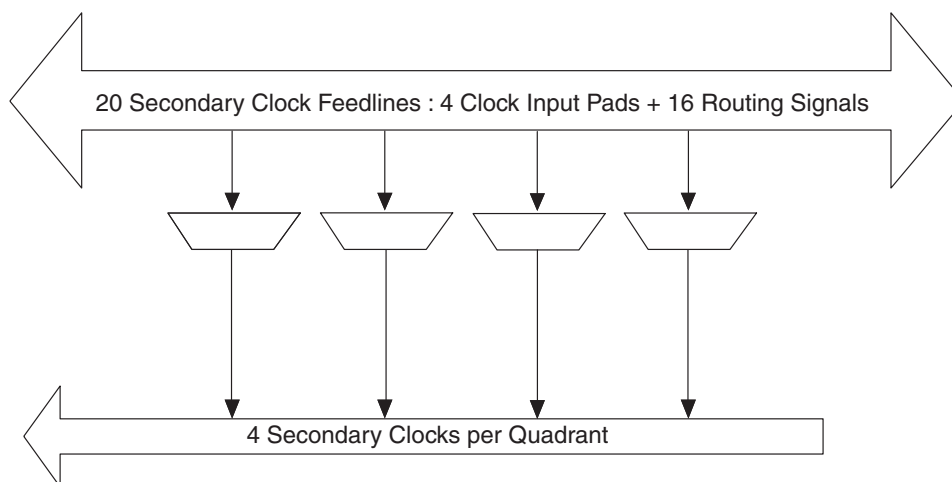
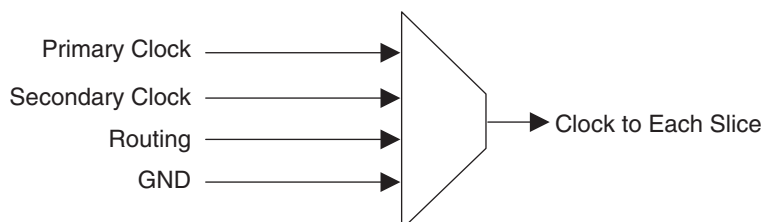
Figure 2-4. Distributed Memory Primitives



ROM Mode: The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

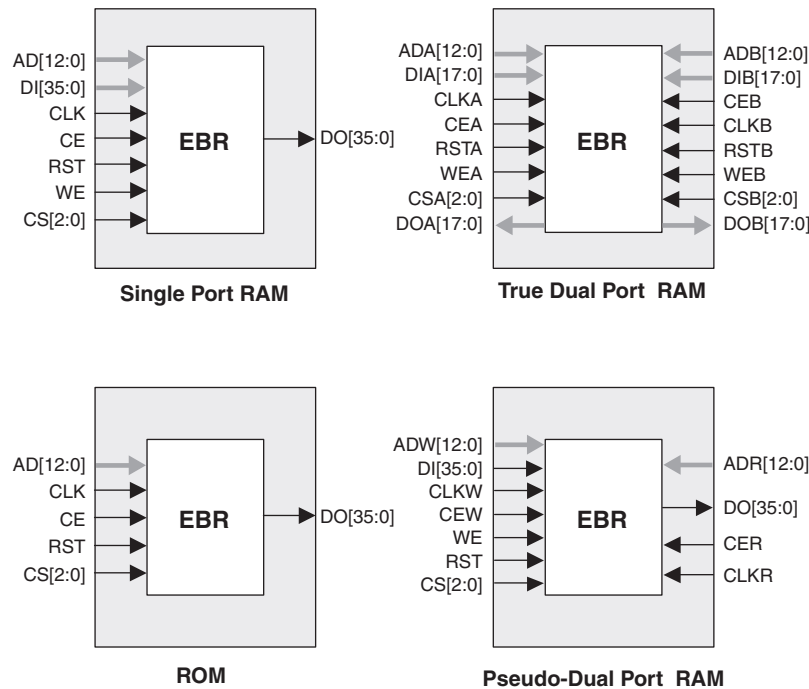
Figure 2-8. Per Quadrant Secondary Clock Selection**Figure 2-9. Slice Clock Selection**

sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signals to the feedback divider: from CLKOP (PLL internal), from clock net (CLKOP or CLKOS) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the t_{LOCK} parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

Figure 2-14. sysMEM Memory Primitives

The EBR memory supports three forms of write behavior for single port or dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – a copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-15.

Figure 2-26. DQS Local Bus

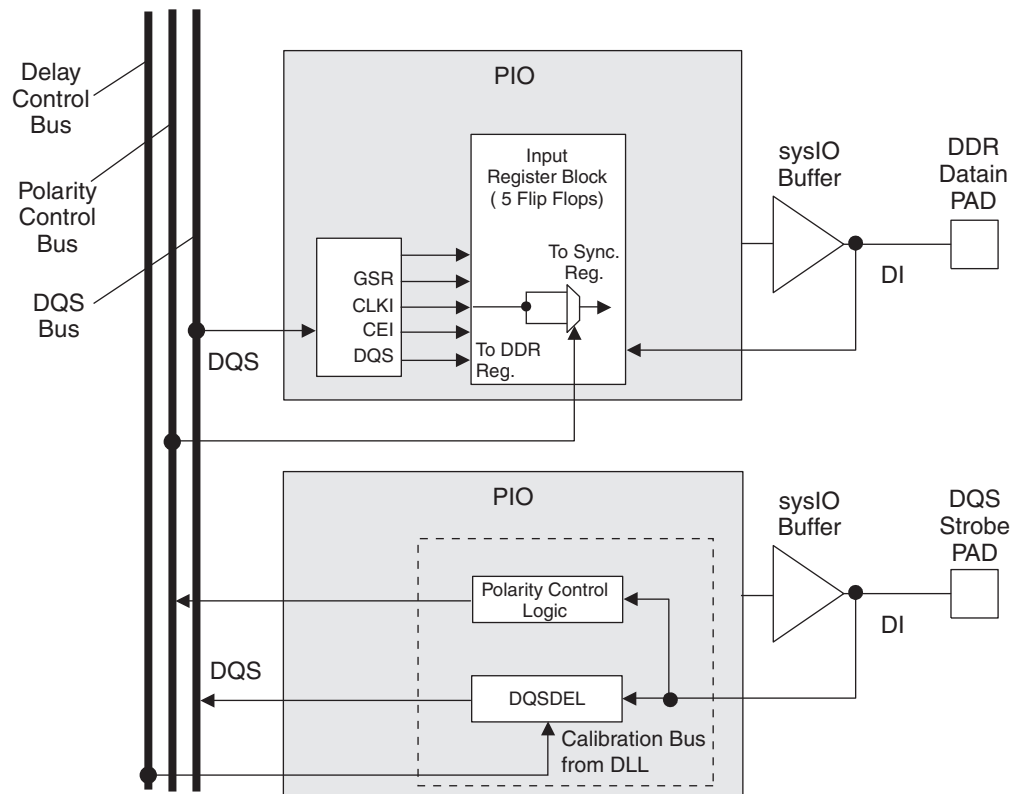


Figure 2-27. DLL Calibration Bus and DQS/DQS Transition Distribution

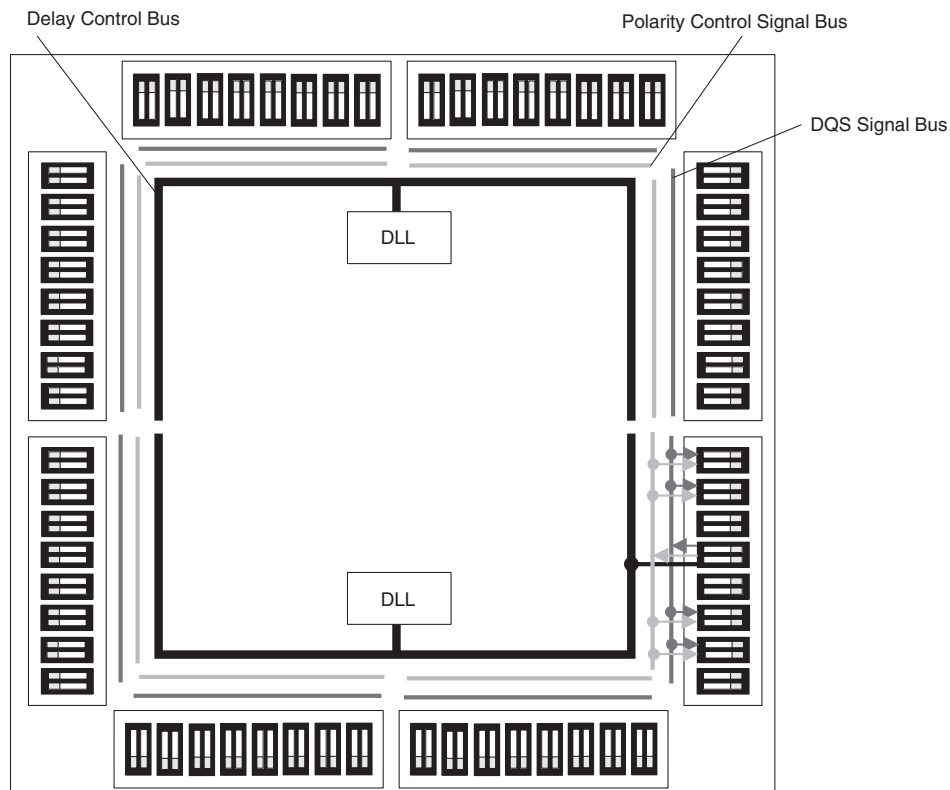


Table 2-8. Supported Output Standards

Output Standard	Drive	V _{CCIO} (Nom.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVC MOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVC MOS25	4mA, 8mA, 12mA 16mA, 20mA	2.5
LVC MOS18	4mA, 8mA, 12mA 16mA	1.8
LVC MOS15	4mA, 8mA	1.5
LVC MOS12	2mA, 6mA	1.2
LVC MOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVC MOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVC MOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVC MOS15, Open Drain	4mA, 8mA	—
LVC MOS12, Open Drain	2mA, 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II, III	N/A	1.8
HSTL15 Class I, III	N/A	1.5
SSTL3 Class I, II	N/A	3.3
SSTL2 Class I, II	N/A	2.5
SSTL18 Class I	N/A	1.8
Differential Interfaces		
Differential SSTL3, Class I, II	N/A	3.3
Differential SSTL2, Class I, II	N/A	2.5
Differential SSTL18, Class I	N/A	1.8
Differential HSTL18, Class I, II, III	N/A	1.8
Differential HSTL15, Class I, III	N/A	1.5
LVDS	N/A	2.5
BLVDS ¹	N/A	2.5
LVPECL ¹	N/A	3.3

1. Emulated with external resistors.

Hot Socketing

The LatticeXP devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits, which allows easy integration with the rest of the system. These capabilities make the LatticeXP ideal for many multiple power supply and hot-swap applications.

Sleep Mode

The LatticeXP “C” devices (V_{CC} = 1.8/2.5/3.3V) have a sleep mode that allows standby current to be reduced by up to three orders of magnitude during periods of system inactivity. Entry and exit to Sleep Mode is controlled by the SLEEPN pin.

During Sleep Mode, the FPGA logic is non-operational, registers and EBR contents are not maintained and I/Os are tri-stated. Do not enter Sleep Mode during device programming or configuration operation. In Sleep Mode, power supplies can be maintained in their normal operating range, eliminating the need for external switching of power supplies. Table 2-9 compares the characteristics of Normal, Off and Sleep Modes.

Figure 2-29 provides a pictorial representation of the different programming ports and modes available in the LatticeXP devices.

On power-up, the FPGA SRAM is ready to be configured with the sysCONFIG port active. The IEEE 1149.1 serial mode can be activated any time after power-up by sending the appropriate command through the TAP port.

Leave Alone I/O

When using 1532 mode for non-volatile memory programming, users may specify I/Os as high, low, tristated or held at current value. This provides excellent flexibility for implementing systems where reprogramming occurs on-the-fly.

TransFR (Transparent Field Reconfiguration)

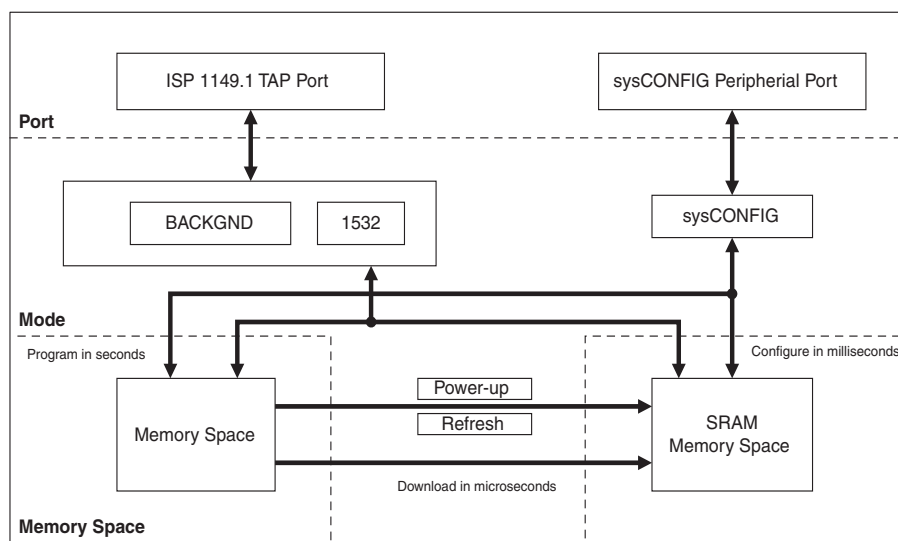
TransFR (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. See Lattice technical note #TN1087, *Minimizing System Interruption During Configuration Using TransFR Technology*, for details.

Security

The LatticeXP devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile memory spaces. Once set, the only way to clear security bits is to erase the memory space.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

Figure 2-29. ispXP Block Diagram



Internal Logic Analyzer Capability (ispTRACY)

All LatticeXP devices support an internal logic analyzer diagnostic feature. The diagnostic features provide capabilities similar to an external logic analyzer, such as programmable event and trigger condition and deep trace memory. This feature is enabled by Lattice's ispTRACY. The ispTRACY utility is added into the user design at compile time.

For more information on ispTRACY, please see information regarding additional technical documentation at the end of this data sheet.

Oscillator

Every LatticeXP device has an internal CMOS oscillator which is used to derive a master serial clock for configuration. The oscillator and the master serial clock run continuously in the configuration mode. The default value of the

master serial clock is 2.5MHz. Table 2-10 lists all the available Master Serial Clock frequencies. When a different Master Serial Clock is selected during the design process, the following sequence takes place:

1. User selects a different Master Serial Clock frequency for configuration.
2. During configuration the device starts with the default (2.5MHz) Master Serial Clock frequency.
3. The clock configuration settings are contained in the early configuration bit stream.
4. The Master Serial Clock frequency changes to the selected frequency once the clock configuration bits are received.

For further information on the use of this oscillator for configuration, please see details of additional technical documentation at the end of this data sheet.

Table 2-10. Selectable Master Serial Clock (CCLK) Frequencies During Configuration

CCLK (MHz)	CCLK (MHz)	CCLK (MHz)
2.5 ¹	13	45
4.3	15	51
5.4	20	55
6.9	26	60
8.1	30	130
9.2	34	—
10.0	41	—

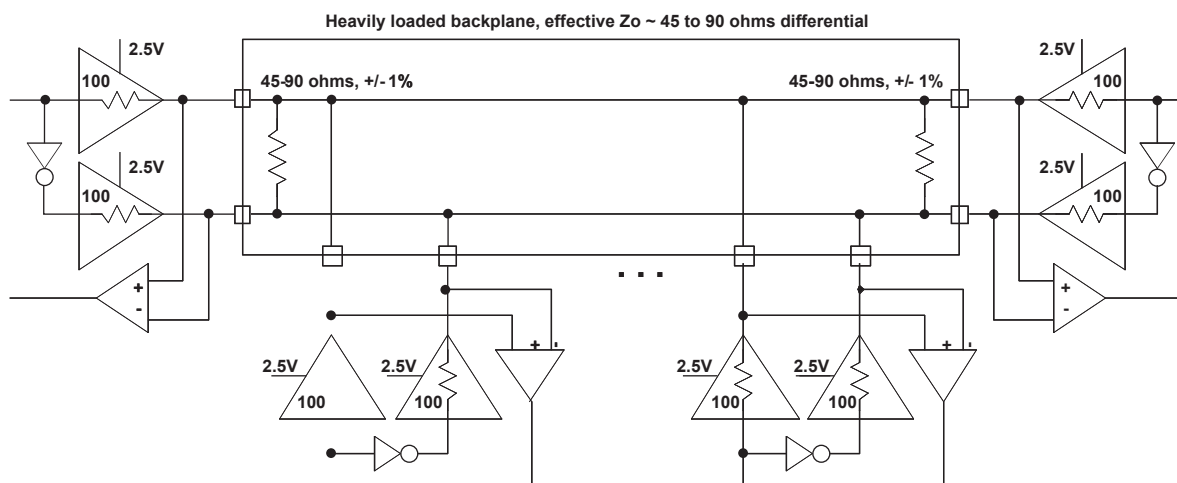
1. Default

Density Shifting

The LatticeXP family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

sysIO Differential Electrical Characteristics**LVDS****Over Recommended Operating Conditions**

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage		0	—	2.4	V
V_{THD}	Differential Input Threshold		+/-100	—	—	mV
V_{CM}	Input Common Mode Voltage	$100\text{mV} \leq V_{THD}$	$V_{THD}/2$	1.2	1.8	V
		$200\text{mV} \leq V_{THD}$	$V_{THD}/2$	1.2	1.9	V
		$350\text{mV} \leq V_{THD}$	$V_{THD}/2$	1.2	2.0	V
I_{IN}	Input current	Power on or power off	—	—	+/-10	μA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	$R_T = 100\text{ ohms}$	—	1.38	1.60	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	$R_T = 100\text{ ohms}$	0.9V	1.03	—	V
V_{OD}	Output voltage differential	$(V_{OP} - V_{OM}), R_T = 100\text{ ohms}$	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	$(V_{OP} - V_{OM})/2, R_T = 100\text{ ohms}$	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	$V_{OD} = 0\text{V}$ Driver outputs shorted	—	—	6	mA

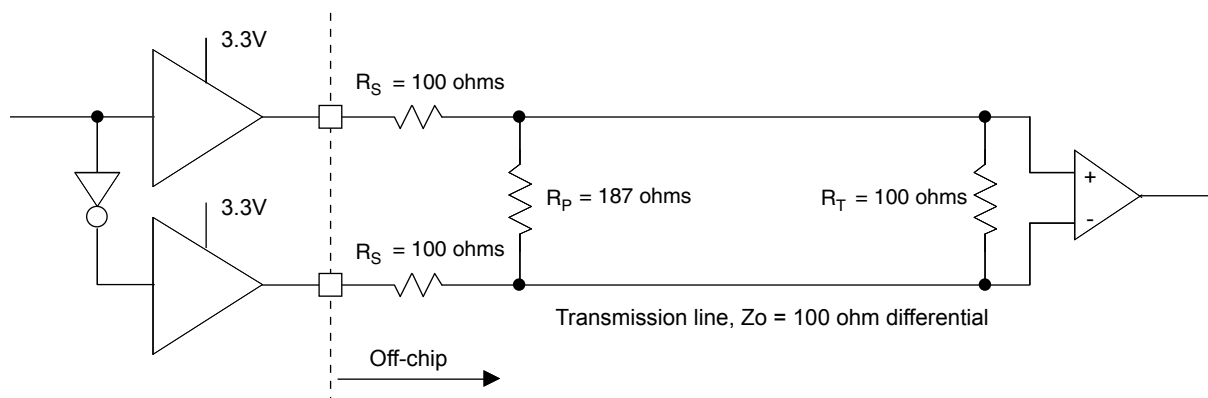
Figure 3-2. BLVDS Multi-point Output Example**Table 3-2. BLVDS DC Conditions¹****Over Recommended Operating Conditions**

Symbol	Description	Typical		Units
		Zo = 45	Zo = 90	
Z _{OUT}	Output impedance	100	100	ohms
R _{TLEFT}	Left end termination	45	90	ohms
R _{TRIGHT}	Right end termination	45	90	ohms
V _{OH}	Output high voltage	1.375	1.48	V
V _{OL}	Output low voltage	1.125	1.02	V
V _{OD}	Output differential voltage	0.25	0.46	V
V _{CM}	Output common mode voltage	1.25	1.25	V
I _{DC}	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

LVPECL

The LatticeXP devices support differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL**Table 3-3. LVPECL DC Conditions¹****Over Recommended Operating Conditions**

Symbol	Description	Typical	Units
Z_{OUT}	Output impedance	100	ohms
R_P	Driver parallel resistor	187	ohms
R_S	Driver series resistor	100	ohms
R_T	Receiver termination	100	ohms
V_{OH}	Output high voltage	2.03	V
V_{OL}	Output low voltage	1.27	V
V_{OD}	Output differential voltage	0.76	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	85.7	ohms
I_{DC}	DC output current	12.7	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

RSDS

The LatticeXP devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

LatticeXP Family Timing Adders¹ (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	-5	-4	-3	Units
HSTL15_I	HSTL_15 class I	0.2	0.2	0.2	ns
HSTL15_III	HSTL_15 class III	0.2	0.2	0.2	ns
HSTL15D_I	Differential HSTL 15 class I	0.2	0.2	0.2	ns
HSTL15D_III	Differential HSTL 15 class III	0.2	0.2	0.2	ns
SSTL33_I	SSTL_3 class I	0.1	0.1	0.1	ns
SSTL33_II	SSTL_3 class II	0.3	0.3	0.3	ns
SSTL33D_I	Differential SSTL_3 class I	0.1	0.1	0.1	ns
SSTL33D_II	Differential SSTL_3 class II	0.3	0.3	0.3	ns
SSTL25_I	SSTL_2 class I	-0.1	-0.1	-0.1	ns
SSTL25_II	SSTL_2 class II	0.3	0.3	0.3	ns
SSTL25D_I	Differential SSTL_2 class I	-0.1	-0.1	-0.1	ns
SSTL25D_II	Differential SSTL_2 class II	0.3	0.3	0.3	ns
SSTL18_I	SSTL_1.8 class I	0.1	0.1	0.1	ns
SSTL18D_I	Differential SSTL_1.8 class I	0.1	0.1	0.1	ns
LVTTTL33_4mA	LVTTTL 4mA drive	0.8	0.8	0.8	ns
LVTTTL33_8mA	LVTTTL 8mA drive	0.5	0.5	0.5	ns
LVTTTL33_12mA	LVTTTL 12mA drive	0.3	0.3	0.3	ns
LVTTTL33_16mA	LVTTTL 16mA drive	0.4	0.4	0.4	ns
LVTTTL33_20mA	LVTTTL 20mA drive	0.3	0.3	0.3	ns
LVC MOS33_2mA	LVC MOS 3.3 2mA drive	0.8	0.8	0.8	ns
LVC MOS33_4mA	LVC MOS 3.3 4mA drive	0.8	0.8	0.8	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive	0.5	0.5	0.5	ns
LVC MOS33_12mA	LVC MOS 3.3 12mA drive	0.3	0.3	0.3	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive	0.4	0.4	0.4	ns
LVC MOS33_20mA	LVC MOS 3.3 20mA drive	0.3	0.3	0.3	ns
LVC MOS25_2mA	LVC MOS 2.5 2mA drive	0.7	0.7	0.7	ns
LVC MOS25_4mA	LVC MOS 2.5 4mA drive	0.7	0.7	0.7	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive	0.4	0.4	0.4	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive	0.0	0.0	0.0	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive	0.2	0.2	0.2	ns
LVC MOS25_20mA	LVC MOS 2.5 20mA drive	0.4	0.4	0.4	ns
LVC MOS18_2mA	LVC MOS 1.8 2mA drive	0.6	0.6	0.6	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive	0.6	0.6	0.6	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive	0.4	0.4	0.4	ns
LVC MOS18_12mA	LVC MOS 1.8 12mA drive	0.2	0.2	0.2	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive	0.2	0.2	0.2	ns
LVC MOS15_2mA	LVC MOS 1.5 2mA drive	0.6	0.6	0.6	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive	0.6	0.6	0.6	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive	0.2	0.2	0.2	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive	0.4	0.4	0.4	ns
LVC MOS12_6mA	LVC MOS 1.2 6mA drive	0.4	0.4	0.4	ns
PCI33	PCI33	0.3	0.3	0.3	ns

1. General timing numbers based on LVC MOS 2.5, 12mA.
Timing v.F0.11

Pin Information Summary¹ (Cont.)

Pin Type		XP10		XP15			XP20		
		256 fpBGA	388 fpBGA	256 fpBGA	388 fpBGA	484 fpBGA	256 fpBGA	388 fpBGA	484 fpBGA
Single Ended User I/O		188	244	188	268	300	188	268	340
Differential Pair User I/O ²		76	104	76	112	128	76	112	144
Configuration	Dedicated	11	11	11	11	11	11	11	11
	Muxed	14	14	14	14	14	14	14	14
TAP		5	5	5	5	5	5	5	5
Dedicated (total without supplies)		6	6	6	6	6	6	6	6
V _{CC}		8	14	8	14	28	8	14	28
V _{CCAUX}		4	4	4	4	12	4	4	12
V _{CCPLL}		2	2	2	2	2	2	2	2
V _{CCIO}	Bank0	2	5	2	5	4	2	5	4
	Bank1	2	5	2	5	4	2	5	4
	Bank2	2	4	2	4	4	2	4	4
	Bank3	2	4	2	4	4	2	4	4
	Bank4	2	5	2	5	4	2	5	4
	Bank5	2	5	2	5	4	2	5	4
	Bank6	2	4	2	4	4	2	4	4
	Bank7	2	4	2	4	4	2	4	4
GND		24	50	24	50	56	24	50	56
GND _{PLL}		2	2	2	2	2	2	2	2
NC		0	24	0	0	40	0	0	0
Single Ended/ Differential I/O per Bank ²	Bank0	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank1	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank2	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank3	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank4	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank5	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank6	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank7	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
V _{CCJ}		1	1	1	1	1	1	1	1

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
2. The differential I/O per bank includes both dedicated LVDS and emulated LVDS pin pairs. Please see the Logic Signal Connections table for more information.

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
T7	PB23B	5	C	-	PB27B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
P8	PB24A	5	T	-	PB28A	5	T	-
T8	PB24B	5	C	-	PB28B	5	C	-
R8	PB25A	5	T	-	PB29A	5	T	-
T9	PB25B	5	C	-	PB29B	5	C	-
R9	PB26A	4	T	-	PB30A	4	T	-
P9	PB26B	4	C	-	PB30B	4	C	-
T10	PB27A	4	T	PCLKT4_0	PB31A	4	T	PCLKT4_0
T11	PB27B	4	C	PCLKC4_0	PB31B	4	C	PCLKC4_0
-	GNDIO4	4	-	-	GNDIO4	4	-	-
R10	PB28A	4	T	-	PB32A	4	T	-
P10	PB28B	4	C	-	PB32B	4	C	-
N9	PB29A	4	-	-	PB33A	4	-	-
M9	PB30B	4	-	-	PB34B	4	-	-
R12	PB31A	4	T	DQS	PB35A	4	T	DQS
T12	PB31B	4	C	VREF1_4	PB35B	4	C	VREF1_4
P13	PB32A	4	T	-	PB36A	4	T	-
R13	PB32B	4	C	-	PB36B	4	C	-
M11	PB33A	4	T	-	PB37A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
N11	PB33B	4	C	-	PB37B	4	C	-
N10	PB34A	4	T	-	PB38A	4	T	-
M10	PB34B	4	C	-	PB38B	4	C	-
T13	PB35A	4	T	-	PB39A	4	T	-
P14	PB35B	4	C	-	PB39B	4	C	-
R11	PB36A	4	T	VREF2_4	PB40A	4	T	VREF2_4
P12	PB36B	4	C	-	PB40B	4	C	-
T14	PB37A	4	-	-	PB41A	4	-	-
R14	PB38B	4	-	-	PB42B	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
P11	PB39A	4	T	DQS	PB43A	4	T	DQS
N12	PB39B	4	C	-	PB43B	4	C	-
T15	PB40A	4	T	-	PB44A	4	T	-
R15	PB40B	4	C	-	PB44B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
P15	PR38B	3	C	RLM0_PLLC_FB_A	PR42B	3	C	RLM0_PLLC_FB_A
N15	PR38A	3	T	RLM0_PLLT_FB_A	PR42A	3	T	RLM0_PLLT_FB_A

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
C20	PT38A	1	T	-	PT43A	1	T	-	PT47A	1	T	-
C21	PT37B	1	C	-	PT42B	1	C	-	PT46B	1	C	-
C22	PT37A	1	T	-	PT42A	1	T	-	PT46A	1	T	-
B22	PT36B	1	C	-	PT41B	1	C	-	PT45B	1	C	-
A21	PT36A	1	T	-	PT41A	1	T	-	PT45A	1	T	-
D15	PT35B	1	C	-	PT40B	1	C	-	PT44B	1	C	-
D14	PT35A	1	T	-	PT40A	1	T	-	PT44A	1	T	-
B21	PT34B	1	C	VREF1_1	PT39B	1	C	VREF1_1	PT43B	1	C	VREF1_1
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
A20	PT34A	1	T	DQS	PT39A	1	T	DQS	PT43A	1	T	DQS
B20	PT33B	1	-	-	PT38B	1	-	-	PT42B	1	-	-
A19	PT32A	1	-	-	PT37A	1	-	-	PT41A	1	-	-
B19	PT31B	1	C	-	PT36B	1	C	-	PT40B	1	C	-
A18	PT31A	1	T	-	PT36A	1	T	-	PT40A	1	T	-
C14	PT30B	1	C	-	PT35B	1	C	-	PT39B	1	C	-
C13	PT30A	1	T	D0	PT35A	1	T	D0	PT39A	1	T	D0
B18	PT29B	1	C	D1	PT34B	1	C	D1	PT38B	1	C	D1
A17	PT29A	1	T	VREF2_1	PT34A	1	T	VREF2_1	PT38A	1	T	VREF2_1
B17	PT28B	1	C	-	PT33B	1	C	-	PT37B	1	C	-
A16	PT28A	1	T	D2	PT33A	1	T	D2	PT37A	1	T	D2
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
B16	PT27B	1	C	D3	PT32B	1	C	D3	PT36B	1	C	D3
A15	PT27A	1	T	-	PT32A	1	T	-	PT36A	1	T	-
B15	PT26B	1	C	-	PT31B	1	C	-	PT35B	1	C	-
A14	PT26A	1	T	DQS	PT31A	1	T	DQS	PT35A	1	T	DQS
D13	PT25B	1	-	-	PT30B	1	-	-	PT34B	1	-	-
D12	PT24A	1	-	D4	PT29A	1	-	D4	PT33A	1	-	D4
B14	PT23B	1	C	-	PT28B	1	C	-	PT32B	1	C	-
A13	PT23A	1	T	D5	PT28A	1	T	D5	PT32A	1	T	D5
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
B13	PT22B	1	C	D6	PT27B	1	C	D6	PT31B	1	C	D6
A12	PT22A	1	T	-	PT27A	1	T	-	PT31A	1	T	-
B12	PT21B	1	C	D7	PT26B	1	C	D7	PT30B	1	C	D7
C12	PT21A	1	T	-	PT26A	1	T	-	PT30A	1	T	-
C11	PT20B	0	C	BUSY	PT25B	0	C	BUSY	PT29B	0	C	BUSY
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
B11	PT20A	0	T	CS1N	PT25A	0	T	CS1N	PT29A	0	T	CS1N
A11	PT19B	0	C	PCLKC0_0	PT24B	0	C	PCLKC0_0	PT28B	0	C	PCLKC0_0
A10	PT19A	0	T	PCLKT0_0	PT24A	0	T	PCLKT0_0	PT28A	0	T	PCLKT0_0
B10	PT18B	0	C	-	PT23B	0	C	-	PT27B	0	C	-
B9	PT18A	0	T	DQS	PT23A	0	T	DQS	PT27A	0	T	DQS
D11	PT17B	0	-	-	PT22B	0	-	-	PT26B	0	-	-
D10	PT16A	0	-	DOUT	PT21A	0	-	DOUT	PT25A	0	-	DOUT
A9	PT15B	0	C	-	PT20B	0	C	-	PT24B	0	C	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C8	PT15A	0	T	WRITEN	PT20A	0	T	WRITEN	PT24A	0	T	WRITEN
B8	PT14B	0	C	-	PT19B	0	C	-	PT23B	0	C	-
A8	PT14A	0	T	VREF1_0	PT19A	0	T	VREF1_0	PT23A	0	T	VREF1_0
C7	PT13B	0	C	-	PT18B	0	C	-	PT22B	0	C	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
A7	PT13A	0	T	DI	PT18A	0	T	DI	PT22A	0	T	DI
B7	PT12B	0	C	-	PT17B	0	C	-	PT21B	0	C	-
C6	PT12A	0	T	CSN	PT17A	0	T	CSN	PT21A	0	T	CSN
C10	PT11B	0	C	-	PT16B	0	C	-	PT20B	0	C	-
C9	PT11A	0	T	-	PT16A	0	T	-	PT20A	0	T	-
A6	PT10B	0	C	VREF2_0	PT15B	0	C	VREF2_0	PT19B	0	C	VREF2_0
B6	PT10A	0	T	DQS	PT15A	0	T	DQS	PT19A	0	T	DQS
A5	PT9B	0	-	-	PT14B	0	-	-	PT18B	0	-	-
B5	PT8A	0	-	-	PT13A	0	-	-	PT17A	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C5	PT7B	0	C	-	PT12B	0	C	-	PT16B	0	C	-
A4	PT7A	0	T	-	PT12A	0	T	-	PT16A	0	T	-
D9	PT6B	0	C	-	PT11B	0	C	-	PT15B	0	C	-
D8	PT6A	0	T	-	PT11A	0	T	-	PT15A	0	T	-
B4	PT5B	0	C	-	PT10B	0	C	-	PT14B	0	C	-
A2	PT5A	0	T	-	PT10A	0	T	-	PT14A	0	T	-
A3	PT4B	0	C	-	PT9B	0	C	-	PT13B	0	C	-
B3	PT4A	0	T	-	PT9A	0	T	-	PT13A	0	T	-
C4	PT3B	0	C	-	PT8B	0	C	-	PT12B	0	C	-
C3	PT3A	0	T	-	PT8A	0	T	-	PT12A	0	T	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C2	-	-	-	-	PT7B	0	C	-	PT11B	0	C	-
D3	PT2A	0	-	-	PT7A	0	T	DQS	PT11A	0	T	DQS
D7	-	-	-	-	PT6B	0	-	-	PT10B	0	-	-
D6	-	-	-	-	PT5A	0	-	-	PT9A	0	-	-
E4	-	-	-	-	PT4B	0	C	-	PT8B	0	C	-
D4	-	-	-	-	PT4A	0	T	-	PT8A	0	T	-
D5	-	-	-	-	PT3B	0	-	-	PT7B	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C1	CFG0	0	-	-	CFG0	0	-	-	CFG0	0	-	-
B2	CFG1	0	-	-	CFG1	0	-	-	CFG1	0	-	-
B1	DONE	0	-	-	DONE	0	-	-	DONE	0	-	-
A1	GND	-	-	-	GND	-	-	-	GND	-	-	-
A22	GND	-	-	-	GND	-	-	-	GND	-	-	-
AB1	GND	-	-	-	GND	-	-	-	GND	-	-	-
AB22	GND	-	-	-	GND	-	-	-	GND	-	-	-
H10	GND	-	-	-	GND	-	-	-	GND	-	-	-
H11	GND	-	-	-	GND	-	-	-	GND	-	-	-
H12	GND	-	-	-	GND	-	-	-	GND	-	-	-
H13	GND	-	-	-	GND	-	-	-	GND	-	-	-
H14	GND	-	-	-	GND	-	-	-	GND	-	-	-
J10	GND	-	-	-	GND	-	-	-	GND	-	-	-
J11	GND	-	-	-	GND	-	-	-	GND	-	-	-
J12	GND	-	-	-	GND	-	-	-	GND	-	-	-
J13	GND	-	-	-	GND	-	-	-	GND	-	-	-
J14	GND	-	-	-	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-	GND	-	-	-
K10	GND	-	-	-	GND	-	-	-	GND	-	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
F5	PROGRAMN	7	-	-	PROGRAMN	7	-	-
E3	CCLK	7	-	-	CCLK	7	-	-
C1	PL2B	7	-	-	PL2B	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
G5	PL3A	7	T ³	-	PL3A	7	T ³	-
G6	PL3B	7	C ³	-	PL3B	7	C ³	-
F4	PL4A	7	T	-	PL4A	7	T	-
F3	PL4B	7	C	-	PL4B	7	C	-
G4	PL5A	7	T ³	-	PL5A	7	T ³	-
G3	PL5B	7	C ³	-	PL5B	7	C ³	-
D1	PL6A	7	T ³	-	PL6A	7	T ³	-
D2	PL6B	7	C ³	-	PL6B	7	C ³	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
E1	PL7A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A
E2	PL7B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A
H5	PL8A	7	T ³	-	PL8A	7	T ³	-
H6	PL8B	7	C ³	-	PL8B	7	C ³	-
H4	PL9A	7	-	-	PL9A	7	-	-
H3	PL10B	7	-	VREF1_7	PL10B	7	-	VREF1_7
F1	PL11A	7	T ³	DQS	PL11A	7	T ³	DQS
F2	PL11B	7	C ³	-	PL11B	7	C ³	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
J5	PL12A	7	T	-	PL12A	7	T	-
J6	PL12B	7	C	-	PL12B	7	C	-
G1	PL13A	7	T ³	-	PL13A	7	T ³	-
G2	PL13B	7	C ³	-	PL13B	7	C ³	-
J4	PL15A	7	T ³	-	PL15A	7	T ³	-
J3	PL15B	7	C ³	-	PL15B	7	C ³	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
H1	PL16A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A
H2	PL16B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A
J1	PL17A	7	T ³	-	PL17A	7	T ³	-
J2	PL17B	7	C ³	-	PL17B	7	C ³	-
K3	PL18A	7	-	VREF2_7	PL18A	7	-	VREF2_7
K2	PL19B	7	-	-	PL19B	7	-	-
K4	PL20A	7	T ³	DQS	PL20A	7	T ³	DQS
-	GNDIO7	7	-	-	GNDIO7	7	-	-
K5	PL20B	7	C ³	-	PL20B	7	C ³	-
K1	PL21A	7	T	-	PL21A	7	T	-
L2	PL21B	7	C	-	PL21B	7	C	-
L4	PL22A	7	T ³	-	PL22A	7	T ³	-
L3	PL22B	7	C ³	-	PL22B	7	C ³	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
D18	-	-	-	-	PT55B	1	C	-
E18	-	-	-	-	PT55A	1	T	-
C19	-	-	-	-	PT54B	1	C	-
C18	-	-	-	-	PT54A	1	T	-
C21	-	-	-	-	PT53B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B21	-	-	-	-	PT53A	1	T	-
E17	PT48B	1	C	-	PT52B	1	C	-
E16	PT48A	1	T	-	PT52A	1	T	-
C17	PT47B	1	C	-	PT51B	1	C	-
D17	PT47A	1	T	DQS	PT51A	1	T	DQS
F17	PT46B	1	-	-	PT50B	1	-	-
F16	PT45A	1	-	-	PT49A	1	-	-
C16	PT44B	1	C	-	PT48B	1	C	-
D16	PT44A	1	T	-	PT48A	1	T	-
A20	PT43B	1	C	-	PT47B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B20	PT43A	1	T	-	PT47A	1	T	-
A19	PT42B	1	C	-	PT46B	1	C	-
B19	PT42A	1	T	-	PT46A	1	T	-
C15	PT41B	1	C	-	PT45B	1	C	-
D15	PT41A	1	T	-	PT45A	1	T	-
A18	PT40B	1	C	-	PT44B	1	C	-
B18	PT40A	1	T	-	PT44A	1	T	-
F15	PT39B	1	C	VREF1_1	PT43B	1	C	VREF1_1
-	GNDIO1	1	-	-	GNDIO1	1	-	-
E15	PT39A	1	T	DQS	PT43A	1	T	DQS
A17	PT38B	1	-	-	PT42B	1	-	-
B17	PT37A	1	-	-	PT41A	1	-	-
E14	PT36B	1	C	-	PT40B	1	C	-
F14	PT36A	1	T	-	PT40A	1	T	-
D14	PT35B	1	C	-	PT39B	1	C	-
C14	PT35A	1	T	D0	PT39A	1	T	D0
A16	PT34B	1	C	D1	PT38B	1	C	D1
B16	PT34A	1	T	VREF2_1	PT38A	1	T	VREF2_1
A15	PT33B	1	C	-	PT37B	1	C	-
B15	PT33A	1	T	D2	PT37A	1	T	D2
-	GNDIO1	1	-	-	GNDIO1	1	-	-
E13	PT32B	1	C	D3	PT36B	1	C	D3
D13	PT32A	1	T	-	PT36A	1	T	-
C13	PT31B	1	C	-	PT35B	1	C	-
B13	PT31A	1	T	DQS	PT35A	1	T	DQS

Industrial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10E-3FN388I	244	1.2V	-3	fpBGA	388	IND	9.7K
LFXP10E-4FN388I	244	1.2V	-4	fpBGA	388	IND	9.7K
LFXP10E-3FN256I	188	1.2V	-3	fpBGA	256	IND	9.7K
LFXP10E-4FN256I	188	1.2V	-4	fpBGA	256	IND	9.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15E-3FN484I	300	1.2V	-3	fpBGA	484	IND	15.5K
LFXP15E-4FN484I	300	1.2V	-4	fpBGA	484	IND	15.5K
LFXP15E-3FN388I	268	1.2V	-3	fpBGA	388	IND	15.5K
LFXP15E-4FN388I	268	1.2V	-4	fpBGA	388	IND	15.5K
LFXP15E-3FN256I	188	1.2V	-3	fpBGA	256	IND	15.5K
LFXP15E-4FN256I	188	1.2V	-4	fpBGA	256	IND	15.5K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20E-3FN484I	340	1.2V	-3	fpBGA	484	IND	19.7K
LFXP20E-4FN484I	340	1.2V	-4	fpBGA	484	IND	19.7K
LFXP20E-3FN388I	268	1.2V	-3	fpBGA	388	IND	19.7K
LFXP20E-4FN388I	268	1.2V	-4	fpBGA	388	IND	19.7K
LFXP20E-3FN256I	188	1.2V	-3	fpBGA	256	IND	19.7K
LFXP20E-4FN256I	188	1.2V	-4	fpBGA	256	IND	19.7K