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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	20000
Total RAM Bits	405504
Number of I/O	188
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp20c-3f256c

Slice

Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from adjacent slice or PFU). There are 7 outputs: 6 to routing and one to carry-chain (to adjacent PFU). Table 2-1 lists the signals associated with each slice.

Figure 2-3. Slice Diagram

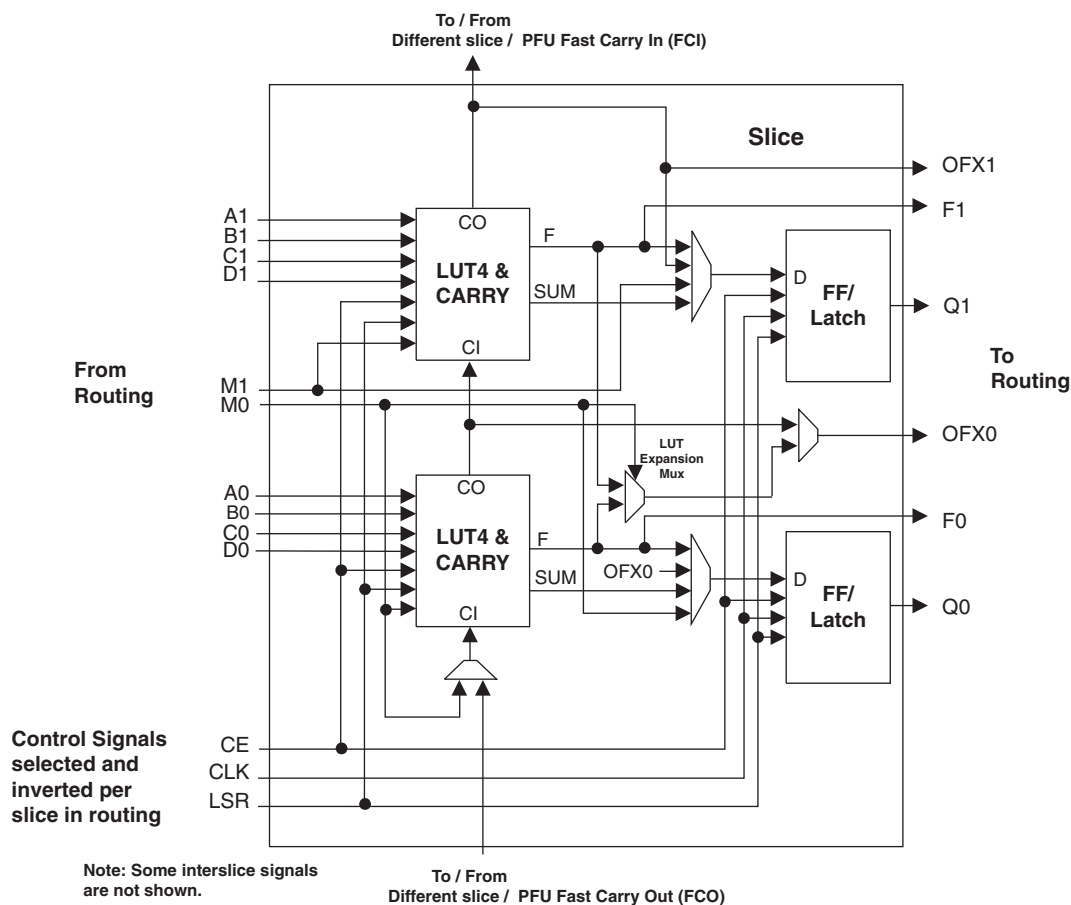
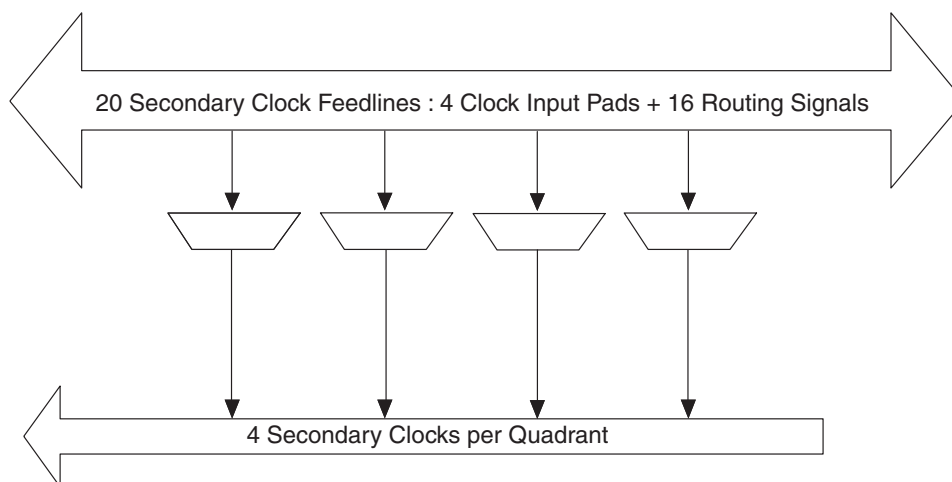
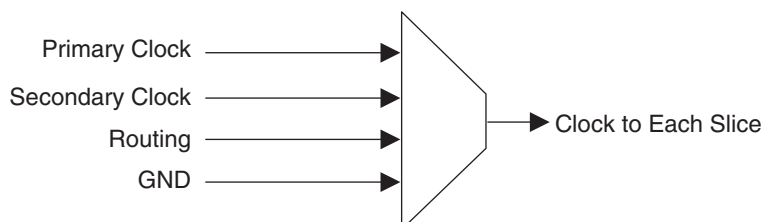


Figure 2-8. Per Quadrant Secondary Clock Selection**Figure 2-9. Slice Clock Selection**

sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signals to the feedback divider: from CLKOP (PLL internal), from clock net (CLKOP or CLKOS) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the t_{LOCK} parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

Figure 2-21. Input Register DDR Waveforms

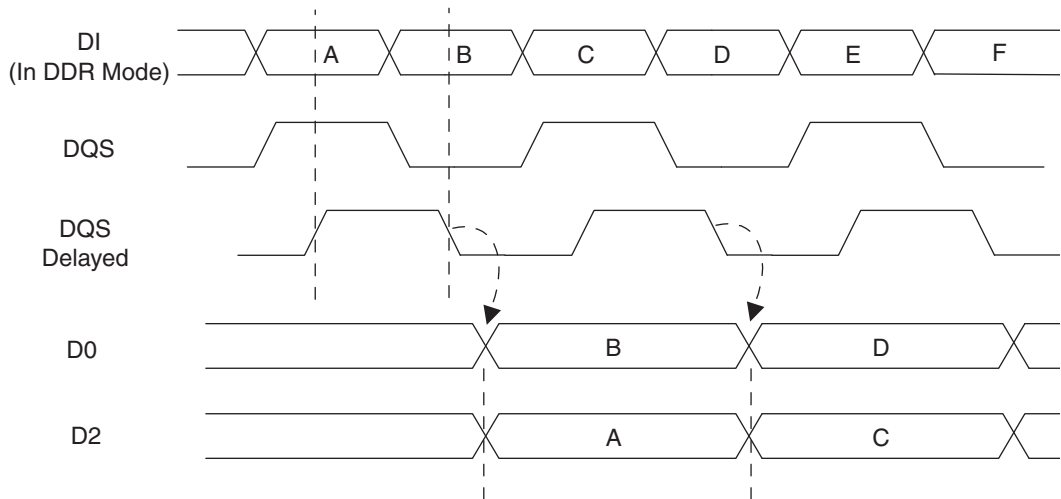
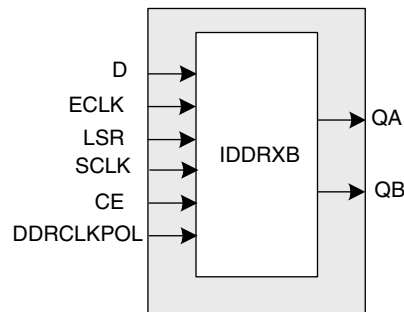


Figure 2-22. INDDRxB Primitive



Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-23 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or as a latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-24 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

Polarity Control Logic

In a typical DDR Memory interface design, the phase relation between the incoming delayed DQS strobe and the internal system Clock (during the READ cycle) is unknown.

The LatticeXP family contains dedicated circuits to transfer data between these domains. To prevent setup and hold violations at the domain transfer between DQS (delayed) and the system Clock a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of the each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in eight groups referred to as Banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

sysIO Buffer Banks

LatticeXP devices have eight sysIO buffer banks; each is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCIO}), and two voltage references V_{REF1} and V_{REF2} resources allowing each bank to be completely independent from each other. Figure 2-28 shows the eight banks and their associated supplies.

In the LatticeXP devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS, PCI and PCI-X) are powered using V_{CCIO} . LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as a fixed threshold input independent of V_{CCIO} . In addition to the bank V_{CCIO} supplies, the LatticeXP devices have a V_{CC} core logic power supply, and a V_{CCAUX} supply that power all differential and referenced buffers.

Each bank can support up to two separate VREF voltages, VREF1 and VREF2 that set the threshold for the referenced input buffers. In the LatticeXP devices, a dedicated pin in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Supply Current (Standby)^{1, 2, 3, 4}**Over Recommended Operating Conditions**

Symbol	Parameter	Device	Typ. ⁵	Units
I_{CC}	Core Power Supply	LFXP3E	15	mA
		LFXP6E	20	mA
		LFXP10E	35	mA
		LFXP15E	45	mA
		LFXP20E	55	mA
		LFXP3C	35	mA
		LFXP6C	40	mA
		LFXP10C	70	mA
		LFXP15C	80	mA
		LFXP20C	90	mA
I_{CCP}	PLL Power Supply (per PLL)	All	8	mA
I_{CCAUX}	Auxiliary Power Supply $V_{CCAUX} = 3.3V$	LFXP3E/C	22	mA
		LFXP6E/C	22	mA
		LFXP10E/C	30	mA
		LFXP15E/C	30	mA
		LFXP20E/C	30	mA
I_{CCIO}	Bank Power Supply ⁶	All	2	mA
I_{CCJ}	V_{CCJ} Power Supply	All	1	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the VCCIO or GND.

3. Frequency 0MHz.

4. User pattern: blank.

5. $T_A=25^{\circ}C$, power supplies at nominal voltage.

6. Per bank.

Programming and Erase Flash Supply Current^{1, 2, 3, 4, 5}

Symbol	Parameter	Device	Typ ⁶	Units
I_{CC}	Core Power Supply	LFXP3E	30	mA
		LFXP6E	40	mA
		LFXP10E	50	mA
		LFXP15E	60	mA
		LFXP20E	70	mA
		LFXP3C	50	mA
		LFXP6C	60	mA
		LFXP10C	90	mA
		LFXP15C	100	mA
		LFXP20C	110	mA
I_{CCAUX}	Auxiliary Power Supply $V_{CCAUX} = 3.3V$	LFXP3E/C	50	mA
		LFXP6E/C	60	mA
		LFXP10E/C	90	mA
		LFXP15E/C	110	mA
		LFXP20E/C	130	mA
I_{CCJ}	V_{CCJ} Power Supply ⁷	All	2	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

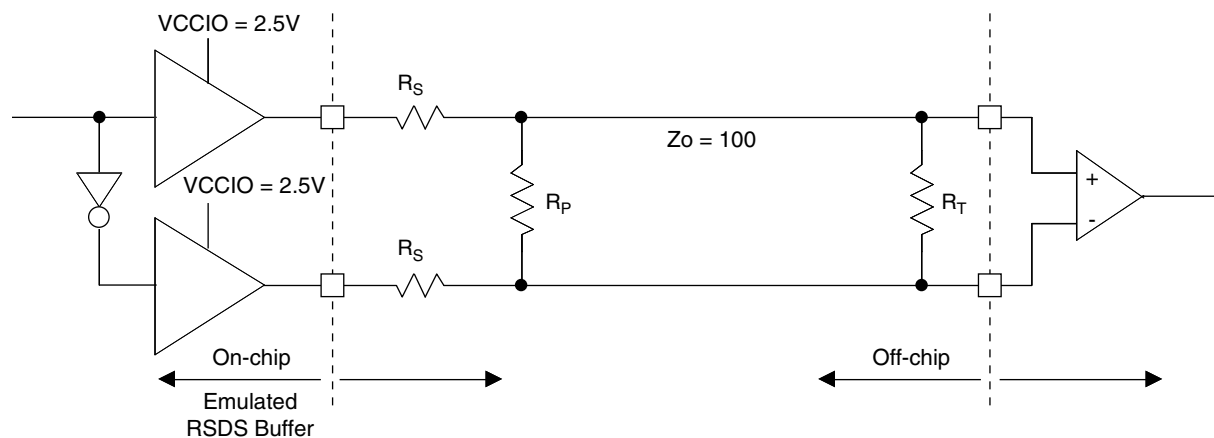
3. Blank user pattern; typical Flash pattern.

4. Bypass or decoupling capacitor across the supply.

5. JTAG programming is at 1MHz.

6. $T_A=25^{\circ}C$, power supplies at nominal voltage.

7. When programming via JTAG.

Figure 3-4. RSDS (Reduced Swing Differential Standard)**Table 3-4. RSDS DC Conditions**

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	ohms
R_S	Driver series resistor	300	ohms
R_P	Driver parallel resistor	121	ohms
R_T	Receiver termination	100	ohms
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	ohms
I_{DC}	DC output current	3.66	mA

LatticeXP Internal Timing Parameters¹

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t _{LUT4_PFU}	LUT4 Delay (A to D Inputs to F Output)	—	0.28	—	0.34	—	0.40	ns
t _{LUT6_PFU}	LUT6 Delay (A to D Inputs to OFX Output)	—	0.44	—	0.53	—	0.63	ns
t _{LSR_PFU}	Set/Reset to Output of PFU	—	0.90	—	1.08	—	1.29	ns
t _{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.13	—	0.15	—	0.19	—	ns
t _{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.04	—	-0.03	—	-0.03	—	ns
t _{SUD_PFU}	Clock to D Input Setup Time	0.13	—	0.16	—	0.19	—	ns
t _{HD_PFU}	Clock to D Input Hold Time	-0.03	—	-0.02	—	-0.02	—	ns
t _{CK2Q_PFU}	Clock to Q Delay, D-type Register Configuration	—	0.40	—	0.48	—	0.58	ns
t _{LE2Q_PFU}	Clock to Q Delay Latch Configuration	—	0.53	—	0.64	—	0.76	ns
t _{LD2Q_PFU}	D to Q Throughput Delay when Latch is Enabled	—	0.55	—	0.66	—	0.79	ns
PFU Dual Port Memory Mode Timing								
t _{CORAM_PFU}	Clock to Output	—	0.40	—	0.48	—	0.58	ns
t _{SUDATA_PFU}	Data Setup Time	-0.18	—	-0.14	—	-0.11	—	ns
t _{HDATA_PFU}	Data Hold Time	0.28	—	0.34	—	0.40	—	ns
t _{SUADDR_PFU}	Address Setup Time	-0.46	—	-0.37	—	-0.30	—	ns
t _{HADDR_PFU}	Address Hold Time	0.71	—	0.85	—	1.02	—	ns
t _{SUWREN_PFU}	Write/Read Enable Setup Time	-0.22	—	-0.17	—	-0.14	—	ns
t _{HWREN_PFU}	Write/Read Enable Hold Time	0.33	—	0.40	—	0.48	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t _{IN_PIO}	Input Buffer Delay	—	0.62	—	0.72	—	0.85	ns
t _{OUT_PIO}	Output Buffer Delay	—	2.12	—	2.54	—	3.05	ns
IOLOGIC Input/Output Timing								
t _{SUI_PIO}	Input Register Setup Time (Data Before Clock)	1.35	—	1.83	—	2.37	—	ns
t _{HI_PIO}	Input Register Hold Time (Data After Clock)	0.05	—	0.05	—	0.05	—	ns
t _{COO_PIO}	Output Register Clock to Output Delay	—	0.36	—	0.44	—	0.52	ns
t _{SUCE_PIO}	Input Register Clock Enable Setup Time	-0.09	—	-0.07	—	-0.06	—	ns
t _{HCE_PIO}	Input Register Clock Enable Hold Time	0.13	—	0.16	—	0.19	—	ns
t _{SULSR_PIO}	Set/Reset Setup Time	0.19	—	0.23	—	0.28	—	ns
t _{HLSR_PIO}	Set/Reset Hold Time	-0.14	—	-0.11	—	-0.09	—	ns
EBR Timing								
t _{CO_EBR}	Clock to Output from Address or Data	—	4.01	—	4.81	—	5.78	ns
t _{COO_EBR}	Clock to Output from EBR Output Register	—	0.81	—	0.97	—	1.17	ns
t _{SUDATA_EBR}	Setup Data to EBR Memory	-0.26	—	-0.21	—	-0.17	—	ns
t _{HDATA_EBR}	Hold Data to EBR Memory	0.41	—	0.49	—	0.59	—	ns
t _{SUADDR_EBR}	Setup Address to EBR Memory	-0.26	—	-0.21	—	-0.17	—	ns
t _{HADDR_EBR}	Hold Address to EBR Memory	0.41	—	0.49	—	0.59	—	ns
t _{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory	-0.17	—	-0.13	—	-0.11	—	ns
t _{HWREN_EBR}	Hold Write/Read Enable to EBR Memory	0.26	—	0.31	—	0.37	—	ns
t _{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.19	—	0.23	—	0.28	—	ns
t _{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.13	—	-0.10	—	-0.08	—	ns

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
P[Edge] [Row/Column Number*]_[A/B]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic. During configuration, the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
GSRN	I	Global RESET signal. (Active low). Any I/O pin can be configured to be GSRN.
NC	—	No connect.
GND	—	GND - Ground. Dedicated Pins.
V _{CC}	—	VCC - The power supply pins for core logic. Dedicated Pins.
V _{CCAUX}	—	V _{CCAUX} - The Auxiliary power supply pin. It powers all the differential and referenced input buffers. Dedicated Pins.
V _{CCP0}	—	Voltage supply pins for ULM0PLL (and LLM1PLL ¹).
V _{CCP1}	—	Voltage supply pins for URM0PLL (and LRM1PLL ¹).
GNDP0	—	Ground pins for ULM0PLL (and LLM1PLL ¹).
GNDP1	—	Ground pins for URM0PLL (and LRM1PLL ¹).
V _{CCIOx}	—	V _{CCIO} - The power supply pins for I/O bank x. Dedicated Pins.
V _{REF1(x)} , V _{REF2(x)}	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V _{REF} inputs. When not used, they may be used as I/O pins.
PLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_PLL[T, C]_IN_A	—	Reference clock (PLL) input Pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A, B, C...at each side.
[LOC][num]_PLL[T, C]_FB_A	—	Optional feedback (PLL) input Pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A, B, C...at each side.
PCLK[T, C]_[n:0]_[3:0]	—	Primary Clock Pads, T = true and C = complement, n per side, indexed by bank and 0, 1, 2, 3 within bank.
[LOC]DQS[num]	—	DQS input Pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = Ball function number. Any pad can be configured to be DQS output.

LFXP3 Logic Signal Connections: 100 TQFP

Pin Number	Pin Function	Bank	Differential	Dual Function
1	CFG1	0	-	-
2	DONE	0	-	-
3	PROGRAMN	7	-	-
4	CCLK	7	-	-
5	PL3A	7	T	LUM0_PLLT_FB_A
6	PL3B	7	C	LUM0_PLLC_FB_A
7	VCCIO7	7	-	-
8	PL5A	7	-	VREF1_7
9	PL6B	7	-	VREF2_7
10	GNDIO7	7	-	-
11	PL7A	7	T ³	DQS
12	PL7B	7	C ³	-
13	PL8A	7	T	LUM0_PLLT_IN_A
14	PL8B	7	C	LUM0_PLLC_IN_A
15	PL9A	7	T ³	-
16	PL9B	7	C ³	-
17	VCCP0	-	-	-
18	GNDP0	-	-	-
19	PL12A	6	T	PCLKT6_0
20	PL12B	6	C	PCLKC6_0
21	GNDIO6	6	-	-
22	VCCIO6	6	-	-
23	PL18A	6	T ³	-
24	PL18B	6	C ³	-
25	VCCAUX	-	-	-
26	SLEEPN ¹ /TOE ²	-	-	-
27	INITN	5	-	-
28	VCC	-	-	-
29	PB2B	5	-	VREF1_5
30	PB5B	5	-	VREF2_5
31	PB8A	5	T	-
32	PB8B	5	C	-
33	GNDIO5	5	-	-
34	PB9A	5	-	-
35	PB10B	5	-	-
36	PB11A	5	T	DQS
37	PB11B	5	C	-
38	VCCIO5	5	-	-
39	PB12A	5	T	-
40	PB12B	5	C	-
41	PB13A	5	T	-
42	PB13B	5	C	-
43	GND	-	-	-

LFXP3 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	Pin Function	Bank	Differential	Dual Function
44	GNDIO4	4	-	-
45	PB15A	4	T	PCLKT4_0
46	PB15B	4	C	PCLKC4_0
47	VCCIO4	4	-	-
48	PB19A	4	T	DQS
49	PB19B	4	C	VREF1_4
50	PB24A	4	-	VREF2_4
51	PR18B	3	C ³	-
52	GNDIO3	3	-	-
53	PR18A	3	T ³	-
54	PR15B	3	-	VREF1_3
55	PR14A	3	-	VREF2_3
56	PR13B	3	C	-
57	PR13A	3	T	-
58	VCCIO3	3	-	-
59	GNDP1	-	-	-
60	VCCP1	-	-	-
61	PR9B	2	C	PCLKC2_0
62	PR9A	2	T	PCLKT2_0
63	PR8B	2	C	RUM0_PLLC_IN_A
64	PR8A	2	T	RUM0_PLLT_IN_A
65	VCCIO2	2	-	-
66	PR6B	2	-	VREF1_2
67	PR5A	2	-	VREF2_2
68	GNDIO2	2	-	-
69	PR3B	2	C	RUM0_PLLC_FB_A
70	PR3A	2	T	RUM0_PLLT_FB_A
71	VCCAUX	-	-	-
72	TDO	-	-	-
73	VCCJ	-	-	-
74	TDI	-	-	-
75	TMS	-	-	-
76	TCK	-	-	-
77	VCC	-	-	-
78	PT24A	1	-	-
79	PT23A	1	-	D0
80	PT22B	1	-	D1
81	PT21A	1	-	D2
82	VCCIO1	1	-	-
83	PT20B	1	-	D3
84	GNDIO1	1	-	-
85	PT17A	1	-	D4
86	PT16A	1	-	D5
87	PT15B	1	-	D6

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
1	CFG1	0	-	-	CFG1	0	-	-
2	DONE	0	-	-	DONE	0	-	-
3	PROGRAMN	7	-	-	PROGRAMN	7	-	-
4	CCLK	7	-	-	CCLK	7	-	-
5	GND	-	-	-	GND	-	-	-
6	PL2A	7	T ³	-	PL2A	7	T ³	-
7	GNDIO7	7	-	-	GNDIO7	7	-	-
8	PL2B	7	C ³	-	PL2B	7	C ³	-
9	PL3A	7	T	LUM0_PLLT_FB_A	PL3A	7	T	LUM0_PLLT_FB_A
10	PL3B	7	C	LUM0_PLLC_FB_A	PL3B	7	C	LUM0_PLLC_FB_A
11	PL4A	7	T ³	-	PL4A	7	T ³	-
12	PL4B	7	C ³	-	PL4B	7	C ³	-
13	VCCIO7	7	-	-	VCCIO7	7	-	-
14	PL5A	7	-	VREF1_7	PL5A	7	-	VREF1_7
15	PL6B	7	-	VREF2_7	PL6B	7	-	VREF2_7
16	GNDIO7	7	-	-	GNDIO7	7	-	-
17	PL7A	7	T ³	DQS	PL7A	7	T ³	DQS
18	PL7B	7	C ³	-	PL7B	7	C ³	-
19	VCC	-	-	-	VCC	-	-	-
20	PL8A	7	T	LUM0_PLLT_IN_A	PL8A	7	T	LUM0_PLLT_IN_A
21	PL8B	7	C	LUM0_PLLC_IN_A	PL8B	7	C	LUM0_PLLC_IN_A
22	PL9A	7	T ³	-	PL9A	7	T ³	-
23	VCCIO7	7	-	-	VCCIO7	7	-	-
24	PL9B	7	C ³	-	PL9B	7	C ³	-
25	VCCP0	-	-	-	VCCP0	-	-	-
26	GNDP0	-	-	-	GNDP0	-	-	-
27	NC	-	-	-	PL15B	6	-	-
28	VCCIO6	6	-	-	VCCIO6	6	-	-
29	PL11A	6	T ³	-	PL16A	6	T ³	-
30	PL11B	6	C ³	-	PL16B	6	C ³	-
31	PL12A	6	T	PCLKT6_0	PL17A	6	T	PCLKT6_0
32	PL12B	6	C	PCLKC6_0	PL17B	6	C	PCLKC6_0
33	NC	-	-	-	PL18A	6	T ³	-
34	NC	-	-	-	PL18B	6	C ³	-
35	VCC	-	-	-	VCC	-	-	-
36	PL13A	6	T ³	-	PL21A	6	T ³	-
37	PL13B	6	C ³	-	PL21B	6	C ³	-
38	GNDIO6	6	-	-	GNDIO6	6	-	-
39	PL14A	6	-	VREF1_6	PL22A	6	-	VREF1_6
40	PL15B	6	-	VREF2_6	PL23B	6	-	VREF2_6
41	VCCIO6	6	-	-	VCCIO6	6	-	-
42	PL16A	6	T ³	DQS	PL24A	6	T ³	DQS
43	PL16B	6	C ³	-	PL24B	6	C ³	-
44	PL17A	6	T	-	PL25A	6	T	-
45	PL17B	6	C	-	PL25B	6	C	-
46	PL18A	6	T ³	-	PL26A	6	T ³	-

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP6				LFXP10			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
K4	PL20A	6	T	-	PL29A	6	T	-
K5	PL20B	6	C	-	PL29B	6	C	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
N1	PL23B	6	-	VREF2_6	PL31A	6	-	VREF2_6
N2	PL21B	6	C ³	-	PL32B	6	-	-
P1	PL24A	6	T ³	DQS	PL33A	6	T ³	DQS
P2	PL24B	6	C ³	-	PL33B	6	C ³	-
L5	PL25A	6	T	-	PL34A	6	T	LLM0_PLLT_FB_A
M6	PL25B	6	C	-	PL34B	6	C	LLM0_PLLC_FB_A
M3	PL26A	6	T ³	-	PL35A	6	T ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
N3	PL26B	6	C ³	-	PL35B	6	C ³	-
P4	SLEEPN ¹ /TOE ²	-	-	-	SLEEPN ¹ /TOE ²	-	-	-
P3	INITN	5	-	-	INITN	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
R4	PB2A	5	T	-	PB6A	5	T	-
N5	PB2B	5	C	-	PB6B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
P5	PB5B	5	-	VREF1_5	PB7A	5	T	VREF1_5
R1	PB3B	5	C	-	PB7B	5	C	-
N6	PB4A	5	-	-	PB8A	5	-	-
M7	PB3A	5	T	-	PB9B	5	-	-
R2	PB6A	5	T	DQS	PB10A	5	T	DQS
T2	PB6B	5	C	-	PB10B	5	C	-
R3	PB7A	5	T	-	PB11A	5	T	-
T3	PB7B	5	C	-	PB11B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
T4	PB8A	5	T	-	PB12A	5	T	-
R5	PB8B	5	C	VREF2_5	PB12B	5	C	VREF2_5
N7	PB9A	5	T	-	PB13A	5	T	-
M8	PB9B	5	C	-	PB13B	5	C	-
T5	PB10A	5	T	-	PB14A	5	T	-
P6	PB10B	5	C	-	PB14B	5	C	-
T6	PB11A	5	T	-	PB15A	5	T	-
R6	PB11B	5	C	-	PB15B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
P7	PB12A	5	-	-	PB16A	5	-	-
N8	PB13B	5	-	-	PB17B	5	-	-
R7	PB14A	5	T	DQS	PB18A	5	T	DQS
T7	PB14B	5	C	-	PB18B	5	C	-
P8	PB15A	5	T	-	PB19A	5	T	-
T8	PB15B	5	C	-	PB19B	5	C	-

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP6				LFXP10			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
K10	GND	-	-	-	GND	-	-	-
K7	GND	-	-	-	GND	-	-	-
K8	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-
L6	GND	-	-	-	GND	-	-	-
T1	GND	-	-	-	GND	-	-	-
T16	GND	-	-	-	GND	-	-	-
D13	VCC	-	-	-	VCC	-	-	-
D4	VCC	-	-	-	VCC	-	-	-
E12	VCC	-	-	-	VCC	-	-	-
E5	VCC	-	-	-	VCC	-	-	-
M12	VCC	-	-	-	VCC	-	-	-
M5	VCC	-	-	-	VCC	-	-	-
N13	VCC	-	-	-	VCC	-	-	-
N4	VCC	-	-	-	VCC	-	-	-
E13	VCCAUX	-	-	-	VCCAUX	-	-	-
E4	VCCAUX	-	-	-	VCCAUX	-	-	-
M13	VCCAUX	-	-	-	VCCAUX	-	-	-
M4	VCCAUX	-	-	-	VCCAUX	-	-	-
F7	VCCIO0	0	-	-	VCCIO0	0	-	-
F8	VCCIO0	0	-	-	VCCIO0	0	-	-
F10	VCCIO1	1	-	-	VCCIO1	1	-	-
F9	VCCIO1	1	-	-	VCCIO1	1	-	-
G11	VCCIO2	2	-	-	VCCIO2	2	-	-
H11	VCCIO2	2	-	-	VCCIO2	2	-	-
J11	VCCIO3	3	-	-	VCCIO3	3	-	-
K11	VCCIO3	3	-	-	VCCIO3	3	-	-
L10	VCCIO4	4	-	-	VCCIO4	4	-	-
L9	VCCIO4	4	-	-	VCCIO4	4	-	-
L7	VCCIO5	5	-	-	VCCIO5	5	-	-
L8	VCCIO5	5	-	-	VCCIO5	5	-	-
J6	VCCIO6	6	-	-	VCCIO6	6	-	-
K6	VCCIO6	6	-	-	VCCIO6	6	-	-
G6	VCCIO7	7	-	-	VCCIO7	7	-	-
H6	VCCIO7	7	-	-	VCCIO7	7	-	-

1. Applies to LFXP "C" only.

2. Applies to LFXP "E" only.

3. Supports dedicated LVDS outputs.

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
G7	VCCAUX	-	-	-	VCCAUX	-	-	-	VCCAUX	-	-	-
T16	VCCAUX	-	-	-	VCCAUX	-	-	-	VCCAUX	-	-	-
T7	VCCAUX	-	-	-	VCCAUX	-	-	-	VCCAUX	-	-	-
G10	VCCIO0	0	-	-	VCCIO0	0	-	-	VCCIO0	0	-	-
G11	VCCIO0	0	-	-	VCCIO0	0	-	-	VCCIO0	0	-	-
G8	VCCIO0	0	-	-	VCCIO0	0	-	-	VCCIO0	0	-	-
G9	VCCIO0	0	-	-	VCCIO0	0	-	-	VCCIO0	0	-	-
H8	VCCIO0	0	-	-	VCCIO0	0	-	-	VCCIO0	0	-	-
G12	VCCIO1	1	-	-	VCCIO1	1	-	-	VCCIO1	1	-	-
G13	VCCIO1	1	-	-	VCCIO1	1	-	-	VCCIO1	1	-	-
G14	VCCIO1	1	-	-	VCCIO1	1	-	-	VCCIO1	1	-	-
G15	VCCIO1	1	-	-	VCCIO1	1	-	-	VCCIO1	1	-	-
H15	VCCIO1	1	-	-	VCCIO1	1	-	-	VCCIO1	1	-	-
H16	VCCIO2	2	-	-	VCCIO2	2	-	-	VCCIO2	2	-	-
J16	VCCIO2	2	-	-	VCCIO2	2	-	-	VCCIO2	2	-	-
K16	VCCIO2	2	-	-	VCCIO2	2	-	-	VCCIO2	2	-	-
L16	VCCIO2	2	-	-	VCCIO2	2	-	-	VCCIO2	2	-	-
M16	VCCIO3	3	-	-	VCCIO3	3	-	-	VCCIO3	3	-	-
N16	VCCIO3	3	-	-	VCCIO3	3	-	-	VCCIO3	3	-	-
P16	VCCIO3	3	-	-	VCCIO3	3	-	-	VCCIO3	3	-	-
R16	VCCIO3	3	-	-	VCCIO3	3	-	-	VCCIO3	3	-	-
R15	VCCIO4	4	-	-	VCCIO4	4	-	-	VCCIO4	4	-	-
T12	VCCIO4	4	-	-	VCCIO4	4	-	-	VCCIO4	4	-	-
T13	VCCIO4	4	-	-	VCCIO4	4	-	-	VCCIO4	4	-	-
T14	VCCIO4	4	-	-	VCCIO4	4	-	-	VCCIO4	4	-	-
T15	VCCIO4	4	-	-	VCCIO4	4	-	-	VCCIO4	4	-	-
R8	VCCIO5	5	-	-	VCCIO5	5	-	-	VCCIO5	5	-	-
T10	VCCIO5	5	-	-	VCCIO5	5	-	-	VCCIO5	5	-	-
T11	VCCIO5	5	-	-	VCCIO5	5	-	-	VCCIO5	5	-	-
T8	VCCIO5	5	-	-	VCCIO5	5	-	-	VCCIO5	5	-	-
T9	VCCIO5	5	-	-	VCCIO5	5	-	-	VCCIO5	5	-	-
M7	VCCIO6	6	-	-	VCCIO6	6	-	-	VCCIO6	6	-	-
N7	VCCIO6	6	-	-	VCCIO6	6	-	-	VCCIO6	6	-	-
P7	VCCIO6	6	-	-	VCCIO6	6	-	-	VCCIO6	6	-	-
R7	VCCIO6	6	-	-	VCCIO6	6	-	-	VCCIO6	6	-	-
H7	VCCIO7	7	-	-	VCCIO7	7	-	-	VCCIO7	7	-	-
J7	VCCIO7	7	-	-	VCCIO7	7	-	-	VCCIO7	7	-	-
K7	VCCIO7	7	-	-	VCCIO7	7	-	-	VCCIO7	7	-	-
L7	VCCIO7	7	-	-	VCCIO7	7	-	-	VCCIO7	7	-	-

1. Applies to LFXP "C" only.
2. Applies to LFXP "E" only.
3. Supports dedicated LVDS outputs.

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
AB5	PB16A	5	T	-	PB20A	5	T	-
AB6	PB16B	5	C	-	PB20B	5	C	-
AA8	PB17A	5	T	-	PB21A	5	T	-
AA9	PB17B	5	C	VREF2_5	PB21B	5	C	VREF2_5
W10	PB18A	5	T	-	PB22A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
V10	PB18B	5	C	-	PB22B	5	C	-
AB7	PB19A	5	T	-	PB23A	5	T	-
AB8	PB19B	5	C	-	PB23B	5	C	-
AB9	PB20A	5	T	-	PB24A	5	T	-
AB10	PB20B	5	C	-	PB24B	5	C	-
Y10	PB21A	5	-	-	PB25A	5	-	-
AA10	PB22B	5	-	-	PB26B	5	-	-
W11	PB23A	5	T	DQS	PB27A	5	T	DQS
V11	PB23B	5	C	-	PB27B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y11	PB24A	5	T	-	PB28A	5	T	-
AA11	PB24B	5	C	-	PB28B	5	C	-
AB11	PB25A	5	T	-	PB29A	5	T	-
AB12	PB25B	5	C	-	PB29B	5	C	-
Y12	PB26A	4	T	-	PB30A	4	T	-
AA12	PB26B	4	C	-	PB30B	4	C	-
W12	PB27A	4	T	PCLKT4_0	PB31A	4	T	PCLKT4_0
V12	PB27B	4	C	PCLKC4_0	PB31B	4	C	PCLKC4_0
-	GNDIO4	4	-	-	GNDIO4	4	-	-
AB13	PB28A	4	T	-	PB32A	4	T	-
AB14	PB28B	4	C	-	PB32B	4	C	-
AA13	PB29A	4	-	-	PB33A	4	-	-
Y13	PB30B	4	-	-	PB34B	4	-	-
AB15	PB31A	4	T	DQS	PB35A	4	T	DQS
AB16	PB31B	4	C	VREF1_4	PB35B	4	C	VREF1_4
V13	PB32A	4	T	-	PB36A	4	T	-
W13	PB32B	4	C	-	PB36B	4	C	-
AA14	PB33A	4	T	-	PB37A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA15	PB33B	4	C	-	PB37B	4	C	-
AB17	PB34A	4	T	-	PB38A	4	T	-
AB18	PB34B	4	C	-	PB38B	4	C	-
W14	PB35A	4	T	-	PB39A	4	T	-
Y14	PB35B	4	C	-	PB39B	4	C	-
U14	PB36A	4	T	VREF2_4	PB40A	4	T	VREF2_4
V14	PB36B	4	C	-	PB40B	4	C	-

Industrial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15E-3F484I	300	1.2V	-3	fpBGA	484	IND	15.5K
LFXP15E-4F484I	300	1.2V	-4	fpBGA	484	IND	15.5K
LFXP15E-3F388I	268	1.2V	-3	fpBGA	388	IND	15.5K
LFXP15E-4F388I	268	1.2V	-4	fpBGA	388	IND	15.5K
LFXP15E-3F256I	188	1.2V	-3	fpBGA	256	IND	15.5K
LFXP15E-4F256I	188	1.2V	-4	fpBGA	256	IND	15.5K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20E-3F484I	340	1.2V	-3	fpBGA	484	IND	19.7K
LFXP20E-4F484I	340	1.2V	-4	fpBGA	484	IND	19.7K
LFXP20E-3F388I	268	1.2V	-3	fpBGA	388	IND	19.7K
LFXP20E-4F388I	268	1.2V	-4	fpBGA	388	IND	19.7K
LFXP20E-3F256I	188	1.2V	-3	fpBGA	256	IND	19.7K
LFXP20E-4F256I	188	1.2V	-4	fpBGA	256	IND	19.7K

Commercial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15E-3FN484C	300	1.2V	-3	fpBGA	484	COM	15.5K
LFXP15E-4FN484C	300	1.2V	-4	fpBGA	484	COM	15.5K
LFXP15E-5FN484C	300	1.2V	-5	fpBGA	484	COM	15.5K
LFXP15E-3FN388C	268	1.2V	-3	fpBGA	388	COM	15.5K
LFXP15E-4FN388C	268	1.2V	-4	fpBGA	388	COM	15.5K
LFXP15E-5FN388C	268	1.2V	-5	fpBGA	388	COM	15.5K
LFXP15E-3FN256C	188	1.2V	-3	fpBGA	256	COM	15.5K
LFXP15E-4FN256C	188	1.2V	-4	fpBGA	256	COM	15.5K
LFXP15E-5FN256C	188	1.2V	-5	fpBGA	256	COM	15.5K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20E-3FN484C	340	1.2V	-3	fpBGA	484	COM	19.7K
LFXP20E-4FN484C	340	1.2V	-4	fpBGA	484	COM	19.7K
LFXP20E-5FN484C	340	1.2V	-5	fpBGA	484	COM	19.7K
LFXP20E-3FN388C	268	1.2V	-3	fpBGA	388	COM	19.7K
LFXP20E-4FN388C	268	1.2V	-4	fpBGA	388	COM	19.7K
LFXP20E-5FN388C	268	1.2V	-5	fpBGA	388	COM	19.7K
LFXP20E-3FN256C	188	1.2V	-3	fpBGA	256	COM	19.7K
LFXP20E-4FN256C	188	1.2V	-4	fpBGA	256	COM	19.7K
LFXP20E-5FN256C	188	1.2V	-5	fpBGA	256	COM	19.7K

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3C-3QN208I	136	1.8/2.5/3.3V	-3	PQFP	208	IND	3.1K
LFXP3C-4QN208I	136	1.8/2.5/3.3V	-4	PQFP	208	IND	3.1K
LFXP3C-3TN144I	100	1.8/2.5/3.3V	-3	TQFP	144	IND	3.1K
LFXP3C-4TN144I	100	1.8/2.5/3.3V	-4	TQFP	144	IND	3.1K
LFXP3C-3TN100I	62	1.8/2.5/3.3V	-3	TQFP	100	IND	3.1K
LFXP3C-4TN100I	62	1.8/2.5/3.3V	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6C-3FN256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	5.8K
LFXP6C-4FN256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	5.8K
LFXP6C-3QN208I	142	1.8/2.5/3.3V	-3	PQFP	208	IND	5.8K
LFXP6C-4QN208I	142	1.8/2.5/3.3V	-4	PQFP	208	IND	5.8K
LFXP6C-3TN144I	100	1.8/2.5/3.3V	-3	TQFP	144	IND	5.8K
LFXP6C-4TN144I	100	1.8/2.5/3.3V	-4	TQFP	144	IND	5.8K

Industrial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10C-3FN388I	244	1.8/2.5/3.3V	-3	fpBGA	388	IND	9.7K
LFXP10C-4FN388I	244	1.8/2.5/3.3V	-4	fpBGA	388	IND	9.7K
LFXP10C-3FN256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	9.7K
LFXP10C-4FN256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	9.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15C-3FN484I	300	1.8/2.5/3.3V	-3	fpBGA	484	IND	15.5K
LFXP15C-4FN484I	300	1.8/2.5/3.3V	-4	fpBGA	484	IND	15.5K
LFXP15C-3FN388I	268	1.8/2.5/3.3V	-3	fpBGA	388	IND	15.5K
LFXP15C-4FN388I	268	1.8/2.5/3.3V	-4	fpBGA	388	IND	15.5K
LFXP15C-3FN256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	15.5K
LFXP15C-4FN256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	15.5K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20C-3FN484I	340	1.8/2.5/3.3V	-3	fpBGA	484	IND	19.7K
LFXP20C-4FN484I	340	1.8/2.5/3.3V	-4	fpBGA	484	IND	19.7K
LFXP20C-3FN388I	268	1.8/2.5/3.3V	-3	fpBGA	388	IND	19.7K
LFXP20C-4FN388I	268	1.8/2.5/3.3V	-4	fpBGA	388	IND	19.7K
LFXP20C-3FN256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	19.7K
LFXP20C-4FN256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	19.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3E-3QN208I	136	1.2V	-3	PQFP	208	IND	3.1K
LFXP3E-4QN208I	136	1.2V	-4	PQFP	208	IND	3.1K
LFXP3E-3TN144I	100	1.2V	-3	TQFP	144	IND	3.1K
LFXP3E-4TN144I	100	1.2V	-4	TQFP	144	IND	3.1K
LFXP3E-3TN100I	62	1.2V	-3	TQFP	100	IND	3.1K
LFXP3E-4TN100I	62	1.2V	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6E-3FN256I	188	1.2V	-3	fpBGA	256	IND	5.8K
LFXP6E-4FN256I	188	1.2V	-4	fpBGA	256	IND	5.8K
LFXP6E-3QN208I	142	1.2V	-3	PQFP	208	IND	5.8K
LFXP6E-4QN208I	142	1.2V	-4	PQFP	208	IND	5.8K
LFXP6E-3TN144I	100	1.2V	-3	TQFP	144	IND	5.8K
LFXP6E-4TN144I	100	1.2V	-4	TQFP	144	IND	5.8K

For Further Information

A variety of technical notes for the LatticeXP family are available on the Lattice website at www.latticesemi.com.

- LatticeECP/EC and LatticeXP sysIO Usage Guide (TN1056)
- Lattice ispTRACY Usage Guide (TN1054)
- LatticeECP/EC and LatticeXP sysCLOCK PLL Design and Usage Guide (TN1049)
- Memory Usage Guide for LatticeECP/EC and LatticeXP Devices (TN1051)
- LatticeECP/EC and XP DDR Usage Guide (TN1050)
- Power Estimation and Management for LatticeECP/EC and LatticeXP Devices (TN1052)
- LatticeXP sysCONFIG Usage Guide (TN1082)

For further information on interface standards refer to the following web sites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com