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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

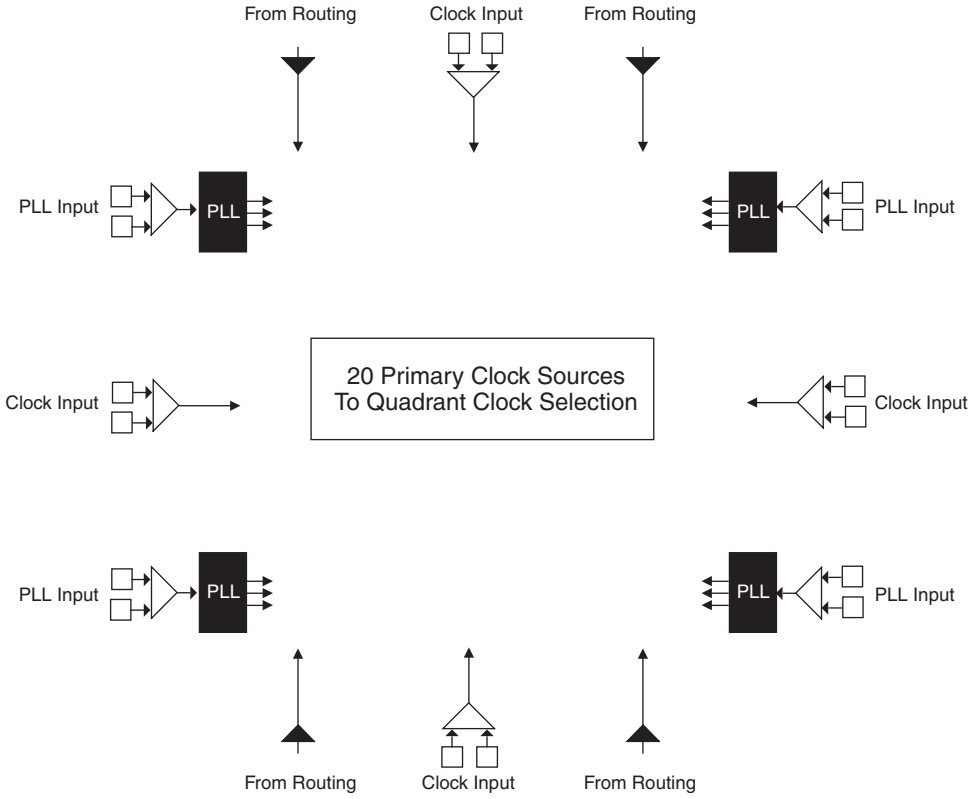
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 20000 |
| Total RAM Bits | 405504 |
| Number of I/O | 268 |
| Number of Gates | - |
| Voltage - Supply | 1.71V ~ 3.465V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 388-BBGA |
| Supplier Device Package | 388-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp20c-4f388i |

***Figure 2-5. Primary Clock Sources***




Note: Smaller devices have two PLLs.

## Secondary Clock Sources

LatticeXP devices have four secondary clock resources per quadrant. The secondary clock branches are tapped at every PFU. These secondary clock networks can also be used for controls and high fanout data. These secondary clocks are derived from four clock input pads and 16 routing signals as shown in Figure 2-6.

*Figure 2-8. Per Quadrant Secondary Clock Selection*

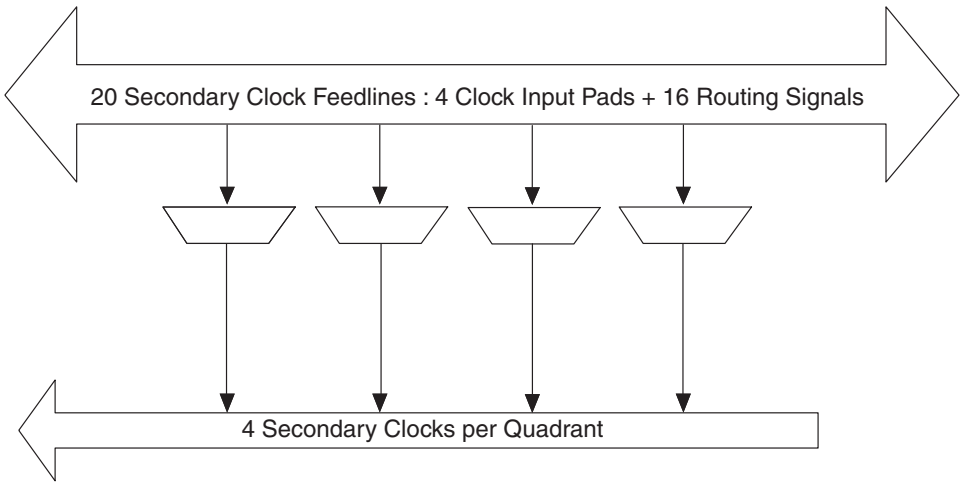
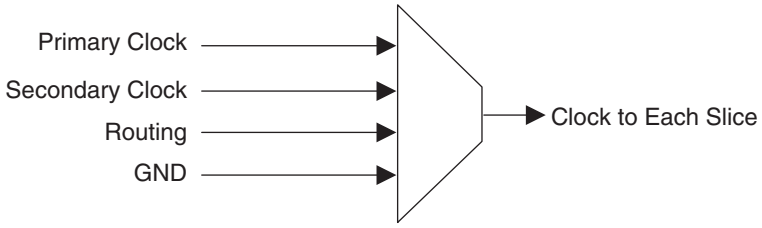



*Figure 2-9. Slice Clock Selection*




## sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signals to the feedback divider: from CLKOP (PLL internal), from clock net (CLKOP or CLKOS) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the $t_{LOCK}$ parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

## Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved irrespective of where the select signal is toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-12 illustrates the DCS Block Macro.

***Figure 2-12. DCS Block Primitive***

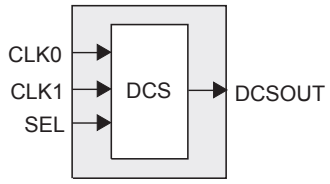
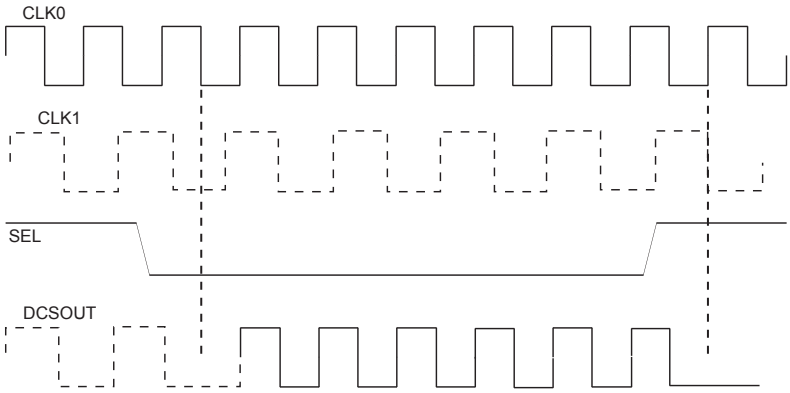



Figure 2-13 shows timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information on the DCS, please see details of additional technical documentation at the end of this data sheet.

***Figure 2-13. DCS Waveforms***




## sysMEM Memory

The LatticeXP family of devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers.

### sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-6.

***Figure 2-21. Input Register DDR Waveforms***

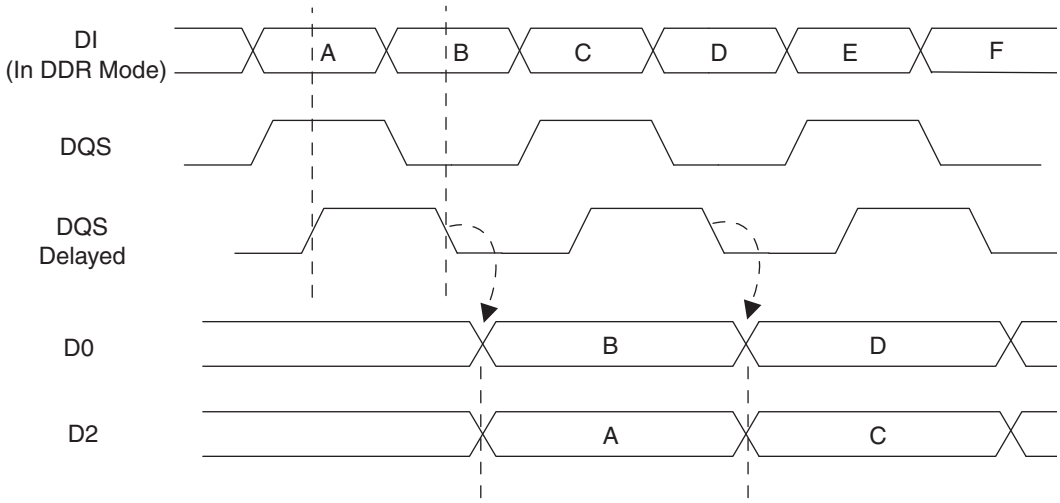
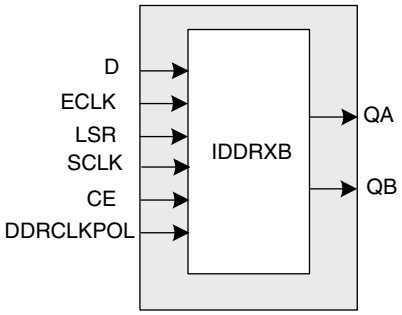



***Figure 2-22. INDDRXB Primitive***



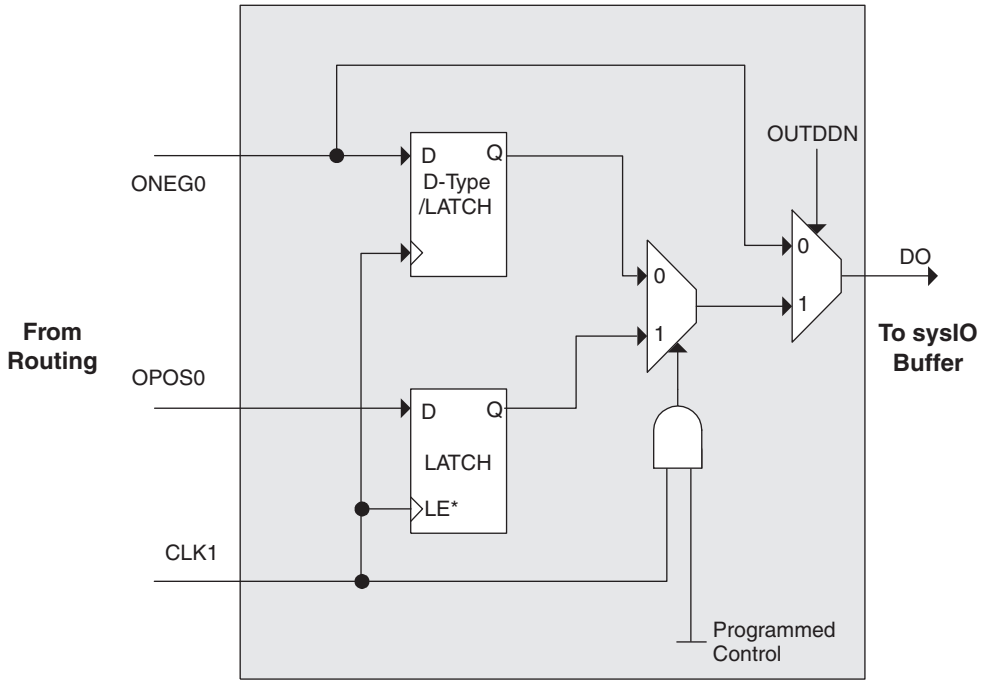

**Output Register Block**

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-23 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or as a latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

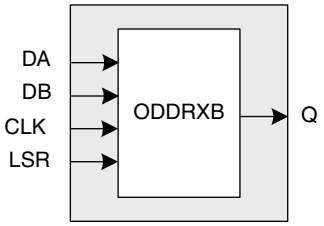
Figure 2-24 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

*Figure 2-23. Output Register Block*




*Latch is transparent when input is low.

*Figure 2-24. ODDRXB Primitive*

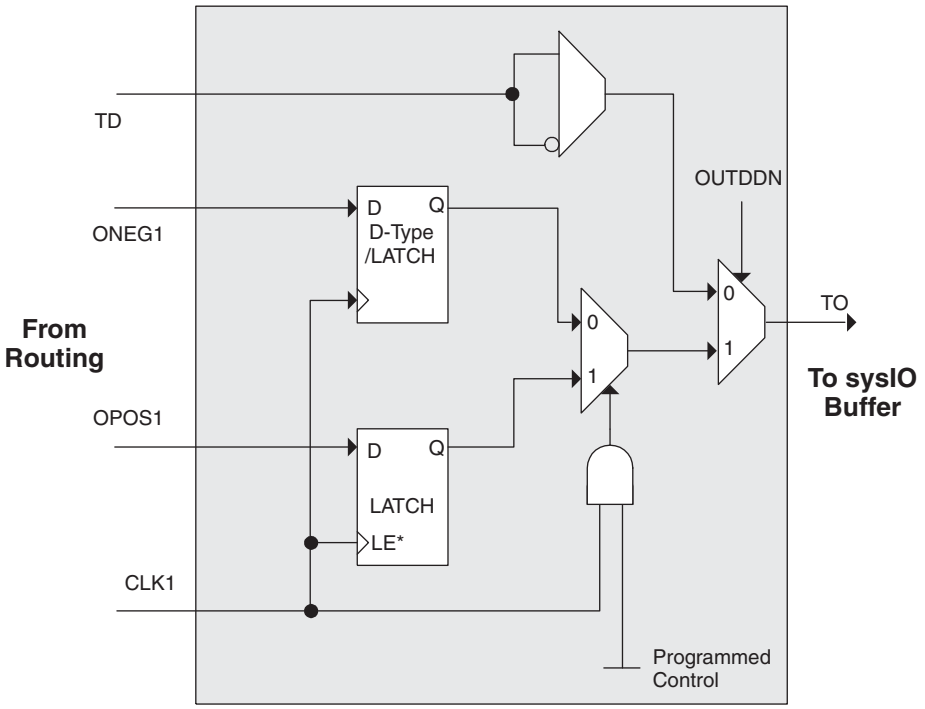



**Tristate Register Block**

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-25 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

*Figure 2-25. Tristate Register Block*




*Latch is transparent when input is low.

**Control Logic Block**

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing and a DQS signal provided from the programmable DQS pin. The clock can optionally be inverted.

The clock enable and local reset signals are selected from the routing and optionally inverted. The global tristate signal is passed through this block.

# DDR Memory Support

Implementing high performance DDR memory interfaces requires dedicated DDR register structures in the input (for read operations) and in the output (for write operations). As indicated in the PIO Logic section, the LatticeXP devices provide this capability. In addition to these registers, the LatticeXP devices contain two elements to simplify the design of input structures for read operations: the DQS delay block and polarity control logic.

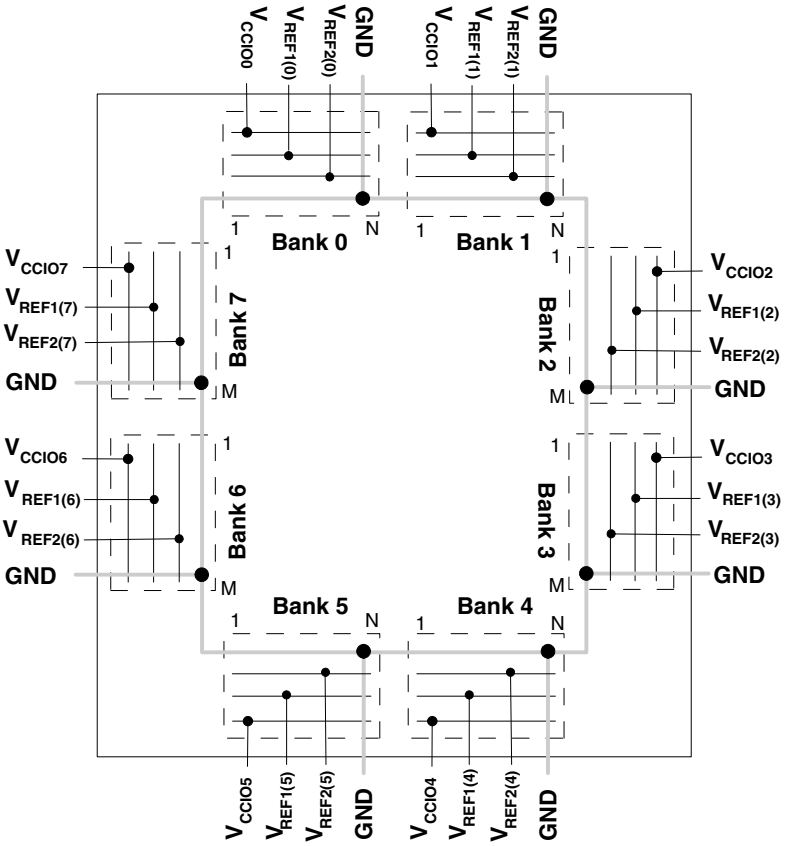
## DLL Calibrated DQS Delay Block

Source Synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment, however in DDR memories the clock (referred to as DQS) is not free running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds the polarity control logic which controls the polarity of the clock to the sync registers in the input register blocks. Figures 2-26 and 2-27 show how the polarity control logic are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two DLLs on opposite sides of the device. Each DLL compensates DQS Delays in its half of the device as shown in Figure 2-27. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

*Figure 2-28. LatticeXP Banks*




Note: N and M are the maximum number of I/Os per bank.

LatticeXP devices contain two types of sysIO buffer pairs.

1. **Top and Bottom sysIO Buffer Pair (Single-Ended Outputs Only)**
   The sysIO buffer pairs in the top and bottom banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

   Only the I/Os on the top and bottom banks have PCI clamps. Note that the PCI clamp is enabled after $V_{CC}$, $V_{CCAUX}$ and $V_{CCIO}$ are at valid operating levels and the device has been configured.

2. **Left and Right sysIO Buffer Pair (Differential and Single-Ended Outputs)**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. The referenced input buffer can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

   Select I/Os in the left and right banks have LVDS differential output drivers. Refer to the Logic Signal Connections tables for more information.

*Table 2-9. Characteristics of Normal, Off and Sleep Modes*

| Characteristic | Normal | Off | Sleep |
|---|---|---|---|
| SLEEPN Pin | High | — | Low |
| Static Icc | Typical <100mA | 0 | Typical <100uA |
| I/O Leakage | <10µA | <1mA | <10µA |
| Power Supplies VCC/VCCIO/VCCAUX | Normal Range | Off | Normal Range |
| Logic Operation | User Defined | Non Operational | Non operational |
| I/O Operation | User Defined | Tri-state | Tri-state |
| JTAG and Programming circuitry | Operational | Non-operational | Non-operational |
| EBR Contents and Registers | Maintained | Non-maintained | Non-maintained |

### SLEEPN Pin Characteristics

The SLEEPN pin behaves as an LVCMOS input with the voltage standard appropriate to the VCC supply for the device. This pin also has a weak pull-up typically in the order of 10µA along with a Schmidt trigger and glitch filter to prevent false triggering. An external pull-up to $V_{CC}$ is recommended when Sleep Mode is not used to ensure the device stays in normal operation mode. Typically the device enters Sleep Mode several hundred ns after SLEEPN is held at a valid low and restarts normal operation as specified in the Sleep Mode Timing table. The AC and DC specifications portion of this data sheet show a detailed timing diagram.

## Configuration and Testing

The following section describes the configuration and testing features of the LatticeXP family of devices.

### IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeXP devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage $V_{CCJ}$ and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

### Device Configuration

All LatticeXP devices contain two possible ports that can be used for device configuration and programming. The test access port (TAP), which supports serial configuration, and the sysCONFIG port that supports both byte-wide and serial configuration.

The non-volatile memory in the LatticeXP can be configured in three different modes:

- In sysCONFIG mode via the sysCONFIG port. Note this can also be done in background mode.
- In 1532 mode via the 1149.1 port.
- In background mode via the 1149.1 port. This allows the device to be operated while reprogramming takes place.

The SRAM configuration memory can be configured in three different ways:

- At power-up via the on-chip non-volatile memory.
- In 1532 mode via the 1149.1 port SRAM direct configuration.
- In sysCONFIG mode via the sysCONFIG port SRAM direct configuration.

# LatticeXP Family Data Sheet DC and Switching Characteristics

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## Absolute Maximum Ratings[1, 2, 3, 4]

| | XPE (1.2V) | XPC (1.8V/2.5V/3.3V) |
|---|---|---|
| Supply Voltage $V_{CC}$ | -0.5 to 1.32V | -0.5 to 3.75V |
| Supply Voltage $V_{CCP}$ | -0.5 to 1.32V | -0.5 to 3.75V |
| Supply Voltage $V_{CCAUX}$ | -0.5 to 3.75V | -0.5 to 3.75V |
| Supply Voltage $V_{CCJ}$ | -0.5 to 3.75V | -0.5 to 3.75V |
| Output Supply Voltage $V_{CCIO}$ | -0.5 to 3.75V | -0.5 to 3.75V |
| I/O Tristate Voltage Applied[5] | -0.5 to 3.75V | -0.5 to 3.75V |
| Dedicated Input Voltage Applied [5] | -0.5 to 3.75V | -0.5 to 4.25V |
| Storage Temperature (Ambient) | -65 to 150°C | -65 to 150°C |
| Junction Temp. (Tj) | +125°C | +125°C |

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions outside of those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. All chip grounds are connected together to a common package GND plane.
5. Overshoot and undershoot of -2V to ($V_{IHMAX}$ + 2) volts is permitted for a duration of <20ns.

## Recommended Operating Conditions[3]

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage for 1.2V Devices | 1.14 | 1.26 | V |
| | Core Supply Voltage for 1.8V/2.5V/3.3V Devices | 1.71 | 3.465 | V |
| $V_{CCP}$ | Supply Voltage for PLL for 1.2V Devices | 1.14 | 1.26 | V |
| | Supply Voltage for PLL for 1.8V/2.5V/3.3V Devices | 1.71 | 3.465 | V |
| $V_{CCAUX}$[4] | Auxiliary Supply Voltage | 3.135 | 3.465 | V |
| $V_{CCIO}$[1, 2] | I/O Driver Supply Voltage | 1.14 | 3.465 | V |
| $V_{CCJ}$[1] | Supply Voltage for IEEE 1149.1 Test Access Port | 1.14 | 3.465 | V |
| $t_{JCOM}$ | Junction Temperature, Commercial Operation | 0 | 85 | C |
| $t_{JIND}$ | Junction Temperature, Industrial Operation | -40 | 100 | C |
| $t_{JFLASHCOM}$ | Junction Temperature, Flash Programming, Commercial | 0 | 85 | C |
| $t_{JFLASHIND}$ | Junction Temperature, Flash Programming, Industrial | 0 | 85 | C |

1. If $V_{CCIO}$ or $V_{CCJ}$ is set to 3.3V, they must be connected to the same power supply as $V_{CCAUX}$. For the XPE devices (1.2V $V_{CC}$), if $V_{CCIO}$ or $V_{CCJ}$ is set to 1.2V, they must be connected to the same power supply as $V_{CC}$.
2. See recommended voltages by I/O standard in subsequent table.
3. The system designer must ensure that the FPGA design stays within the specified junction temperature and package thermal capabilities of the device based on the expected operating frequency, activity factor and environment conditions of the system.
4. $V_{CCAUX}$ ramp rate must not exceed 30mV/µs during power up when transitioning between 0V and 3.3V.

## Supply Current (Standby)[1, 2, 3, 4]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typ.[5] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LFXP3E | 15 | mA |
| | | LFXP6E | 20 | mA |
| | | LFXP10E | 35 | mA |
| | | LFXP15E | 45 | mA |
| | | LFXP20E | 55 | mA |
| | | LFXP3C | 35 | mA |
| | | LFXP6C | 40 | mA |
| | | LFXP10C | 70 | mA |
| | | LFXP15C | 80 | mA |
| | | LFXP20C | 90 | mA |
| $I_{CCP}$ | PLL Power Supply (per PLL) | All | 8 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply $V_{CCAUX}$ = 3.3V | LFXP3E/C | 22 | mA |
| | | LFXP6E/C | 22 | mA |
| | | LFXP10E/C | 30 | mA |
| | | LFXP15E/C | 30 | mA |
| | | LFXP20E/C | 30 | mA |
| $I_{CCIO}$ | Bank Power Supply[6] | All | 2 | mA |
| $I_{CCJ}$ | $V_{CCJ}$ Power Supply | All | 1 | mA |

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the VCCIO or GND.
3. Frequency 0MHz.
4. User pattern: blank.
5. $T_A$=25°C, power supplies at nominal voltage.
6. Per bank.

## LVPECL

The LatticeXP devices support differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

***Figure 3-3. Differential LVPECL***

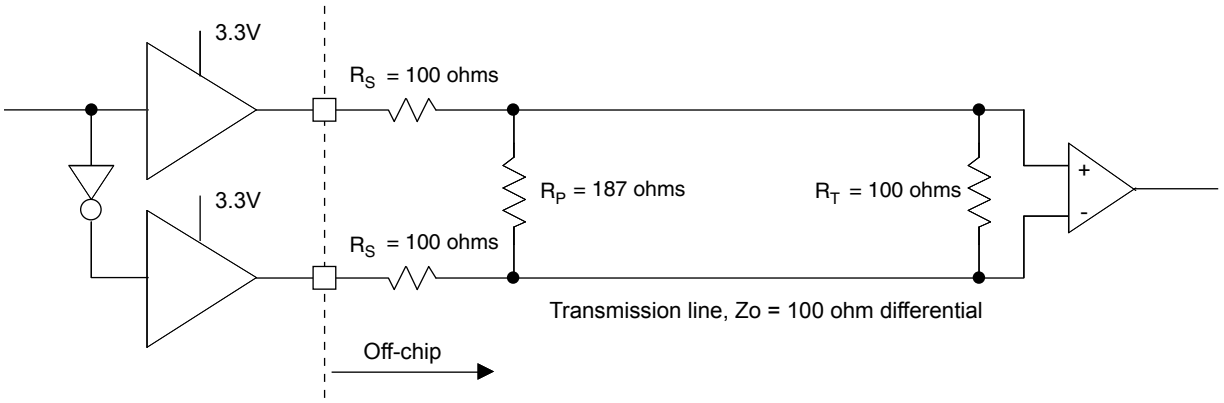



***Table 3-3. LVPECL DC Conditions[1]***

**Over Recommended Operating Conditions**

| Symbol | Description | Typical | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 100 | ohms |
| $R_P$ | Driver parallel resistor | 187 | ohms |
| $R_S$ | Driver series resistor | 100 | ohms |
| $R_T$ | Receiver termination | 100 | ohms |
| $V_{OH}$ | Output high voltage | 2.03 | V |
| $V_{OL}$ | Output low voltage | 1.27 | V |
| $V_{OD}$ | Output differential voltage | 0.76 | V |
| $V_{CM}$ | Output common mode voltage | 1.65 | V |
| $Z_{BACK}$ | Back impedance | 85.7 | ohms |
| $I_{DC}$ | DC output current | 12.7 | mA |

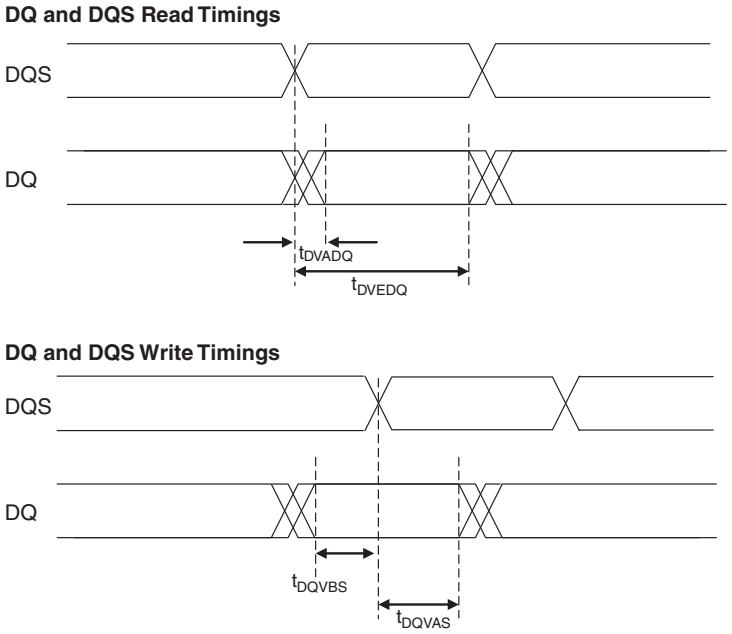
1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

## RSDS

The LatticeXP devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

*Figure 3-5. DDR Timings*



# LatticeXP sysCONFIG Port Timing Specifications

**Over Recommended Operating Conditions**

| Parameter | Description | Min. | Max. | Units |
|---|---|---|---|---|
| **sysCONFIG Byte Data Flow** | | | | |
| $t_{SUCBDI}$ | Byte D[0:7] Setup Time to CCLK | 7 | — | ns |
| $t_{HCBDI}$ | Byte D[0:7] Hold Time to CCLK | 3 | — | ns |
| $t_{CODO}$ | Clock to Dout in Flowthrough Mode | — | 12 | ns |
| $t_{SUCS}$ | CS[0:1] Setup Time to CCLK | 7 | — | ns |
| $t_{HCS}$ | CS[0:1] Hold Time to CCLK | 2 | — | ns |
| $t_{SUWD}$ | Write Signal Setup Time to CCLK | 7 | — | ns |
| $t_{HWD}$ | Write Signal Hold Time to CCLK | 2 | — | ns |
| $t_{DCB}$ | CCLK to BUSY Delay Time | — | 12 | ns |
| $t_{CORD}$ | Clock to Out for Read Data | — | 12 | ns |
| **sysCONFIG Byte Slave Clocking** | | | | |
| $t_{BSCH}$ | Byte Slave Clock Minimum High Pulse | 6 | — | ns |
| $t_{BSCL}$ | Byte Slave Clock Minimum Low Pulse | 8 | — | ns |
| $t_{BSCYC}$ | Byte Slave Clock Cycle Time | 15 | — | ns |
| **sysCONFIG Serial (Bit) Data Flow** | | | | |
| $t_{SUSCDI}$ | DI (Data In) Setup Time to CCLK | 7 | — | ns |
| $t_{HSCDI}$ | DI (Data In) Hold Time to CCLK | 2 | — | ns |
| $t_{CODO}$ | Clock to Dout in Flowthrough Mode | — | 12 | ns |
| **sysCONFIG Serial Slave Clocking** | | | | |
| $t_{SSCH}$ | Serial Slave Clock Minimum High Pulse | 6 | — | ns |
| $t_{SSCL}$ | Serial Slave Clock Minimum Low Pulse | 6 | — | ns |
| **sysCONFIG POR, Initialization and Wake Up** | | | | |
| $t_{ICFG}$ | Minimum Vcc to INIT High | — | 50 | ms |
| $t_{VMC}$ | Time from $t_{ICFG}$ to Valid Master Clock | — | 2 | us |
| $t_{PRGMRJ}$ | Program Pin Pulse Rejection | — | 7 | ns |
| $t_{PRGM}$[2] | PROGRAMN Low Time to Start Configuration | 25 | — | ns |
| $t_{DINIT}$ | INIT Low Time | — | 1 | ms |
| $t_{DPPINIT}$ | Delay Time from PROGRAMN Low to INIT Low | — | 37 | ns |
| $t_{DINITD}$ | Delay Time from PROGRAMN Low to DONE Low | — | 37 | ns |
| $t_{IODISS}$ | User I/O Disable from PROGRAMN Low | — | 25 | ns |
| $t_{IOENSS}$ | User I/O Enabled Time from CCLK Edge During Wake-up Sequence | — | 25 | ns |
| $t_{MWC}$ | Additional Wake Master Clock Signals after Done Pin High | 120 | — | cycles |
| **Configuration Master Clock (CCLK)** | | | | |
| Frequency[1] | | Selected Value - 30% | Selected Value + 30% | MHz |
| Duty Cycle | | 40 | 60 | % |

1. See Table 2-10 for available CCLK frequencies.
2. The threshold level for PROGRAMN, as well as for CFG[1] and CFG[0], is determined by $V_{CC}$, such that the threshold = $V_{CC}/2$.

Timing v.F0.11

## Signal Descriptions (Cont.)

| Signal Name | I/O | Descriptions |
|---|---|---|
| **Test and Programming** (Dedicated pins. Pull-up is enabled on input pins during configuration.) | | |
| TMS | I | Test Mode Select input, used to control the 1149.1 state machine. |
| TCK | I | Test Clock input pin, used to clock the 1149.1 state machine. |
| TDI | I | Test Data in pin, used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). |
| TDO | O | Output pin -Test Data out pin used to shift data out of device using 1149.1. |
| $V_{CCJ}$ | — | $V_{CCJ}$ - The power supply pin for JTAG Test Access Port. |
| **Configuration Pads** (used during sysCONFIG) | | |
| CFG[1:0] | I | Mode pins used to specify configuration modes values latched on rising edge of INITN. During configuration, a pull-up is enabled. |
| INITN | I/O | Open Drain pin - Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. If CFG1 and CFG0 are high (SDM) then this pin is pulled low. |
| PROGRAMN | I | Initiates configuration sequence when asserted low. This pin always has an active pull-up. |
| DONE | I/O | Open Drain pin - Indicates that the configuration sequence is complete, and the startup sequence is in progress. |
| CCLK | I/O | Configuration Clock for configuring an FPGA in sysCONFIG mode. |
| BUSY | I/O | Generally not used. After configuration it is a user-programmable I/O pin. |
| CSN | I | sysCONFIG chip select (Active low). During configuration, a pull-up is enabled. After configuration it is user a programmable I/O pin. |
| CS1N | I | sysCONFIG chip select (Active Low). During configuration, a pull-up is enabled. After configuration it is user programmable I/O pin |
| WRITEN | I | Write Data on Parallel port (Active low). After configuration it is a user programmable I/O pin |
| D[7:0] | I/O | sysCONFIG Port Data I/O. After configuration these are user programmable I/O pins. |
| DOUT, CSON | O | Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port. After configuration, it is a user-programmable I/O pin. |
| DI | I | Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. After configuration it is a user-programmable I/O pin. |
| SLEEPN[2] | I | Sleep Mode pin - Active low sleep pin.þ When this pin is held high, the device operates normally.þ When driven low, the device moves into Sleep Mode after a specified time.This pin has a weak internal pull-up, but when not used an external pull-up to $V_{CC}$ is recommended. |
| TOE[3] | I | Test Output Enable tri-states all I/O pins when driven low. This pin has a weak internal pull-up, but when not used an external pull-up to $V_{CC}$ is recommended. |

1. Applies toþ LFXP10, LFXP15 and LFXP20 only.
2. Applies to LFXP “C” devices only.
3. Applies to LFXP “E” devices only.

# LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP

| Pin Number | LFXP3 | | | | LFXP6 | | | |
|---|---|---|---|---|---|---|---|---|
| | Pin Function | Bank | Differential | Dual Function | Pin Function | Bank | Differential | Dual Function |
| 1 | PROGRAMN | 7 | - | - | PROGRAMN | 7 | - | - |
| 2 | CCLK | 7 | - | - | CCLK | 7 | - | - |
| 3 | GND | - | - | - | GND | - | - | - |
| 4 | PL2A | 7 | T[3] | - | PL2A | 7 | T[3] | - |
| 5 | PL2B | 7 | C[3] | - | PL2B | 7 | C[3] | - |
| 6 | PL3A | 7 | T | LUM0_PLLT_FB_A | PL3A | 7 | T | LUM0_PLLT_FB_A |
| 7 | PL3B | 7 | C | LUM0_PLLC_FB_A | PL3B | 7 | C | LUM0_PLLC_FB_A |
| 8 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| 9 | PL5A | 7 | - | VREF1_7 | PL5A | 7 | - | VREF1_7 |
| 10 | PL6B | 7 | - | VREF2_7 | PL6B | 7 | - | VREF2_7 |
| 11 | GNDIO7 | 7 | - | - | GNDIO7 | 7 | - | - |
| 12 | PL7A | 7 | T[3] | DQS | PL7A | 7 | T[3] | DQS |
| 13 | PL7B | 7 | C[3] | - | PL7B | 7 | C[3] | - |
| 14 | VCC | - | - | - | VCC | - | - | - |
| 15 | PL8A | 7 | T | LUM0_PLLT_IN_A | PL8A | 7 | T | LUM0_PLLT_IN_A |
| 16 | PL8B | 7 | C | LUM0_PLLC_IN_A | PL8B | 7 | C | LUM0_PLLC_IN_A |
| 17 | PL9A | 7 | T[3] | - | PL9A | 7 | T[3] | - |
| 18 | PL9B | 7 | C[3] | - | PL9B | 7 | C[3] | - |
| 19 | VCCP0 | - | - | - | VCCP0 | - | - | - |
| 20 | GNDP0 | - | - | - | GNDP0 | - | - | - |
| 21 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| 22 | PL11A | 6 | T[3] | - | PL16A | 6 | T[3] | - |
| 23 | PL11B | 6 | C[3] | - | PL16B | 6 | C[3] | - |
| 24 | PL12A | 6 | T | PCLKT6_0 | PL17A | 6 | T | PCLKT6_0 |
| 25 | PL12B | 6 | C | PCLKC6_0 | PL17B | 6 | C | PCLKC6_0 |
| 26 | PL13A | 6 | T[3] | - | PL18A | 6 | T[3] | - |
| 27 | PL13B | 6 | C[3] | - | PL18B | 6 | C[3] | - |
| 28 | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| 29 | PL14A | 6 | - | VREF1_6 | PL22A | 6 | - | VREF1_6 |
| 30 | PL15B | 6 | - | VREF2_6 | PL23B | 6 | - | VREF2_6 |
| 31 | PL16A | 6 | T[3] | DQS | PL24A | 6 | T[3] | DQS |
| 32 | PL16B | 6 | C[3] | - | PL24B | 6 | C[3] | - |
| 33 | PL17A | 6 | - | - | PL25A | 6 | - | - |
| 34 | PL18A | 6 | T[3] | - | PL26A | 6 | T[3] | - |
| 35 | PL18B | 6 | C[3] | - | PL26B | 6 | C[3] | - |
| 36 | VCCAUX | - | - | - | VCCAUX | - | - | - |
| 37 | SLEEPN[1]/TOE[2] | - | - | - | SLEEPN[1]/TOE[2] | - | - | - |
| 38 | INITN | 5 | - | - | INITN | 5 | - | - |
| 39 | VCC | - | - | - | VCC | - | - | - |
| 40 | PB2B | 5 | - | VREF1_5 | PB5B | 5 | - | VREF1_5 |
| 41 | PB5B | 5 | - | VREF2_5 | PB8B | 5 | - | VREF2_5 |
| 42 | PB7A | 5 | T | - | PB10A | 5 | T | - |
| 43 | PB7B | 5 | C | - | PB10B | 5 | C | - |
| 44 | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| 45 | PB9A | 5 | - | - | PB12A | 5 | - | - |
| 46 | PB10B | 5 | - | - | PB13B | 5 | - | - |

## LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| L4 | PL32A | 6 | - | - | PL36A | 6 | - | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| K4 | PL33A | 6 | T | - | PL37A | 6 | T | - |
| K5 | PL33B | 6 | C | - | PL37B | 6 | C | - |
| N1 | PL35A | 6 | - | VREF2_6 | PL39A | 6 | - | VREF2_6 |
| N2 | PL36B | 6 | - | - | PL40B | 6 | - | - |
| P1 | PL37A | 6 | T[3] | DQS | PL41A | 6 | T[3] | DQS |
| P2 | PL37B | 6 | C[3] | - | PL41B | 6 | C[3] | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| L5 | PL38A | 6 | T | LLM0_PLLT_FB_A | PL42A | 6 | T | LLM0_PLLT_FB_A |
| M6 | PL38B | 6 | C | LLM0_PLLC_FB_A | PL42B | 6 | C | LLM0_PLLC_FB_A |
| M3 | PL39A | 6 | T[3] | - | PL43A | 6 | T[3] | - |
| N3 | PL39B | 6 | C[3] | - | PL43B | 6 | C[3] | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| P4 | SLEEPN[1]/TOE[2] | - | - | - | SLEEPN[1]/TOE[2] | - | - | - |
| P3 | INITN | 5 | - | - | INITN | 5 | - | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| R4 | PB11A | 5 | T | - | PB15A | 5 | T | - |
| N5 | PB11B | 5 | C | - | PB15B | 5 | C | - |
| P5 | PB12A | 5 | T | VREF1_5 | PB16A | 5 | T | VREF1_5 |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| R1 | PB12B | 5 | C | - | PB16B | 5 | C | - |
| N6 | PB13A | 5 | - | - | PB17A | 5 | - | - |
| M7 | PB14B | 5 | - | - | PB18B | 5 | - | - |
| R2 | PB15A | 5 | T | DQS | PB19A | 5 | T | DQS |
| T2 | PB15B | 5 | C | - | PB19B | 5 | C | - |
| R3 | PB16A | 5 | T | - | PB20A | 5 | T | - |
| T3 | PB16B | 5 | C | - | PB20B | 5 | C | - |
| T4 | PB17A | 5 | T | - | PB21A | 5 | T | - |
| R5 | PB17B | 5 | C | VREF2_5 | PB21B | 5 | C | VREF2_5 |
| N7 | PB18A | 5 | T | - | PB22A | 5 | T | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| M8 | PB18B | 5 | C | - | PB22B | 5 | C | - |
| T5 | PB19A | 5 | T | - | PB23A | 5 | T | - |
| P6 | PB19B | 5 | C | - | PB23B | 5 | C | - |
| T6 | PB20A | 5 | T | - | PB24A | 5 | T | - |
| R6 | PB20B | 5 | C | - | PB24B | 5 | C | - |
| P7 | PB21A | 5 | - | - | PB25A | 5 | - | - |
| N8 | PB22B | 5 | - | - | PB26B | 5 | - | - |
| R7 | PB23A | 5 | T | DQS | PB27A | 5 | T | DQS |

# LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

| Ball Number | LFXP10 | | | | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function |
| G7 | VCCAUX | - | - | - | VCCAUX | - | - | - | VCCAUX | - | - | - |
| T16 | VCCAUX | - | - | - | VCCAUX | - | - | - | VCCAUX | - | - | - |
| T7 | VCCAUX | - | - | - | VCCAUX | - | - | - | VCCAUX | - | - | - |
| G10 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| G11 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| G8 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| G9 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| H8 | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - | VCCIO0 | 0 | - | - |
| G12 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| G13 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| G14 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| G15 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| H15 | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - | VCCIO1 | 1 | - | - |
| H16 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| J16 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| K16 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| L16 | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - | VCCIO2 | 2 | - | - |
| M16 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| N16 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| P16 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| R16 | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - | VCCIO3 | 3 | - | - |
| R15 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| T12 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| T13 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| T14 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| T15 | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - | VCCIO4 | 4 | - | - |
| R8 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| T10 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| T11 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| T8 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| T9 | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - | VCCIO5 | 5 | - | - |
| M7 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| N7 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| P7 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| R7 | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - | VCCIO6 | 6 | - | - |
| H7 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| J7 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| K7 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |
| L7 | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - | VCCIO7 | 7 | - | - |

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

# LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| T6 | PL41A | 6 | T | - | PL45A | 6 | T | - |
| T5 | PL41B | 6 | C | - | PL45B | 6 | C | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| U3 | PL42A | 6 | T[3] | - | PL46A | 6 | T[3] | - |
| U4 | PL42B | 6 | C[3] | - | PL46B | 6 | C[3] | - |
| V4 | PL43A | 6 | - | - | PL47A | 6 | - | - |
| W4 | SLEEPN[1]/ TOE[2] | - | - | - | SLEEPN[1]/ TOE[2] | - | - | - |
| W5 | INITN | 5 | - | - | INITN | 5 | - | - |
| Y3 | - | - | - | - | PB3B | 5 | - | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| U5 | - | - | - | - | PB4A | 5 | T | - |
| V5 | - | - | - | - | PB4B | 5 | C | - |
| Y4 | - | - | - | - | PB5A | 5 | T | - |
| Y5 | - | - | - | - | PB5B | 5 | C | - |
| V6 | - | - | - | - | PB6A | 5 | T | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| U6 | - | - | - | - | PB6B | 5 | C | - |
| W6 | PB3A | 5 | T | - | PB7A | 5 | T | - |
| Y6 | PB3B | 5 | C | - | PB7B | 5 | C | - |
| AA2 | PB4A | 5 | T | - | PB8A | 5 | T | - |
| AA3 | PB4B | 5 | C | - | PB8B | 5 | C | - |
| V7 | PB5A | 5 | - | - | PB9A | 5 | - | - |
| U7 | PB6B | 5 | - | - | PB10B | 5 | - | - |
| Y7 | PB7A | 5 | T | DQS | PB11A | 5 | T | DQS |
| W7 | PB7B | 5 | C | - | PB11B | 5 | C | - |
| AA4 | PB8A | 5 | T | - | PB12A | 5 | T | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| AA5 | PB8B | 5 | C | - | PB12B | 5 | C | - |
| AB3 | PB9A | 5 | T | - | PB13A | 5 | T | - |
| AB4 | PB9B | 5 | C | - | PB13B | 5 | C | - |
| AA6 | PB10A | 5 | T | - | PB14A | 5 | T | - |
| AA7 | PB10B | 5 | C | - | PB14B | 5 | C | - |
| U8 | PB11A | 5 | T | - | PB15A | 5 | T | - |
| V8 | PB11B | 5 | C | - | PB15B | 5 | C | - |
| Y8 | PB12A | 5 | T | VREF1_5 | PB16A | 5 | T | VREF1_5 |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| W8 | PB12B | 5 | C | - | PB16B | 5 | C | - |
| V9 | PB13A | 5 | - | - | PB17A | 5 | - | - |
| U9 | PB14B | 5 | - | - | PB18B | 5 | - | - |
| Y9 | PB15A | 5 | T | DQS | PB19A | 5 | T | DQS |
| W9 | PB15B | 5 | C | - | PB19B | 5 | C | - |

## LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| D18 | - | - | - | - | PT55B | 1 | C | - |
| E18 | - | - | - | - | PT55A | 1 | T | - |
| C19 | - | - | - | - | PT54B | 1 | C | - |
| C18 | - | - | - | - | PT54A | 1 | T | - |
| C21 | - | - | - | - | PT53B | 1 | C | - |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| B21 | - | - | - | - | PT53A | 1 | T | - |
| E17 | PT48B | 1 | C | - | PT52B | 1 | C | - |
| E16 | PT48A | 1 | T | - | PT52A | 1 | T | - |
| C17 | PT47B | 1 | C | - | PT51B | 1 | C | - |
| D17 | PT47A | 1 | T | DQS | PT51A | 1 | T | DQS |
| F17 | PT46B | 1 | - | - | PT50B | 1 | - | - |
| F16 | PT45A | 1 | - | - | PT49A | 1 | - | - |
| C16 | PT44B | 1 | C | - | PT48B | 1 | C | - |
| D16 | PT44A | 1 | T | - | PT48A | 1 | T | - |
| A20 | PT43B | 1 | C | - | PT47B | 1 | C | - |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| B20 | PT43A | 1 | T | - | PT47A | 1 | T | - |
| A19 | PT42B | 1 | C | - | PT46B | 1 | C | - |
| B19 | PT42A | 1 | T | - | PT46A | 1 | T | - |
| C15 | PT41B | 1 | C | - | PT45B | 1 | C | - |
| D15 | PT41A | 1 | T | - | PT45A | 1 | T | - |
| A18 | PT40B | 1 | C | - | PT44B | 1 | C | - |
| B18 | PT40A | 1 | T | - | PT44A | 1 | T | - |
| F15 | PT39B | 1 | C | VREF1_1 | PT43B | 1 | C | VREF1_1 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| E15 | PT39A | 1 | T | DQS | PT43A | 1 | T | DQS |
| A17 | PT38B | 1 | - | - | PT42B | 1 | - | - |
| B17 | PT37A | 1 | - | - | PT41A | 1 | - | - |
| E14 | PT36B | 1 | C | - | PT40B | 1 | C | - |
| F14 | PT36A | 1 | T | - | PT40A | 1 | T | - |
| D14 | PT35B | 1 | C | - | PT39B | 1 | C | - |
| C14 | PT35A | 1 | T | D0 | PT39A | 1 | T | D0 |
| A16 | PT34B | 1 | C | D1 | PT38B | 1 | C | D1 |
| B16 | PT34A | 1 | T | VREF2_1 | PT38A | 1 | T | VREF2_1 |
| A15 | PT33B | 1 | C | - | PT37B | 1 | C | - |
| B15 | PT33A | 1 | T | D2 | PT37A | 1 | T | D2 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| E13 | PT32B | 1 | C | D3 | PT36B | 1 | C | D3 |
| D13 | PT32A | 1 | T | - | PT36A | 1 | T | - |
| C13 | PT31B | 1 | C | - | PT35B | 1 | C | - |
| B13 | PT31A | 1 | T | DQS | PT35A | 1 | T | DQS |

# LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| A14 | PT30B | 1 | - | - | PT34B | 1 | - | - |
| B14 | PT29A | 1 | - | D4 | PT33A | 1 | - | D4 |
| C12 | PT28B | 1 | C | - | PT32B | 1 | C | - |
| B12 | PT28A | 1 | T | D5 | PT32A | 1 | T | D5 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| D12 | PT27B | 1 | C | D6 | PT31B | 1 | C | D6 |
| E12 | PT27A | 1 | T | - | PT31A | 1 | T | - |
| A13 | PT26B | 1 | C | D7 | PT30B | 1 | C | D7 |
| A12 | PT26A | 1 | T | - | PT30A | 1 | T | - |
| A11 | PT25B | 0 | C | BUSY | PT29B | 0 | C | BUSY |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| A10 | PT25A | 0 | T | CS1N | PT29A | 0 | T | CS1N |
| D11 | PT24B | 0 | C | PCLKC0_0 | PT28B | 0 | C | PCLKC0_0 |
| E11 | PT24A | 0 | T | PCLKT0_0 | PT28A | 0 | T | PCLKT0_0 |
| B11 | PT23B | 0 | C | - | PT27B | 0 | C | - |
| C11 | PT23A | 0 | T | DQS | PT27A | 0 | T | DQS |
| B9 | PT22B | 0 | - | - | PT26B | 0 | - | - |
| A9 | PT21A | 0 | - | DOUT | PT25A | 0 | - | DOUT |
| B8 | PT20B | 0 | C | - | PT24B | 0 | C | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| A8 | PT20A | 0 | T | WRITEN | PT24A | 0 | T | WRITEN |
| E10 | PT19B | 0 | C | - | PT23B | 0 | C | - |
| D10 | PT19A | 0 | T | VREF1_0 | PT23A | 0 | T | VREF1_0 |
| C10 | PT18B | 0 | C | - | PT22B | 0 | C | - |
| B10 | PT18A | 0 | T | DI | PT22A | 0 | T | DI |
| B7 | PT17B | 0 | C | - | PT21B | 0 | C | - |
| A7 | PT17A | 0 | T | CSN | PT21A | 0 | T | CSN |
| C9 | PT16B | 0 | C | - | PT20B | 0 | C | - |
| D9 | PT16A | 0 | T | - | PT20A | 0 | T | - |
| B6 | PT15B | 0 | C | VREF2_0 | PT19B | 0 | C | VREF2_0 |
| A6 | PT15A | 0 | T | DQS | PT19A | 0 | T | DQS |
| F9 | PT14B | 0 | - | - | PT18B | 0 | - | - |
| E9 | PT13A | 0 | - | - | PT17A | 0 | - | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| B5 | PT12B | 0 | C | - | PT16B | 0 | C | - |
| A5 | PT12A | 0 | T | - | PT16A | 0 | T | - |
| C8 | PT11B | 0 | C | - | PT15B | 0 | C | - |
| D8 | PT11A | 0 | T | - | PT15A | 0 | T | - |
| B4 | PT10B | 0 | C | - | PT14B | 0 | C | - |
| A4 | PT10A | 0 | T | - | PT14A | 0 | T | - |
| F8 | PT9B | 0 | C | - | PT13B | 0 | C | - |
| E8 | PT9A | 0 | T | - | PT13A | 0 | T | - |