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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	20000
Total RAM Bits	405504
Number of I/O	188
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp20c-5f256c

Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output[1]

1. See Figure 2-2 for connection details.
2. Requires two PFUs.

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SP 16x2	ROM 16x1 x 2
PFF Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	N/A	ROM 16x1 x 2

Logic Mode: In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other Slices.

Ripple Mode: Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two additional signals: Carry Generate and Carry Propagate are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode: In this mode, distributed RAM can be constructed using each LUT block as a 16x1-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

Table 2-4. PFU Modes of Operation

Logic	Ripple	RAM[1]	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR16x2 x 4 DPR16x2 x 2	ROM16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR16x4 x 2 DPR16x4 x 1	ROM16x2 x 4
LUT 6x 2 or MUX 8x1 x 2	2-bit Counter x 4	SPR16x8 x 1	ROM16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM16x8 x 1

1. These modes are not available in PFF blocks

Routing

There are many resources provided in the LatticeXP devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal, vertical and diagonal directions. The x2 and x6 resources are buffered allowing both short and long connections routing between PFUs.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

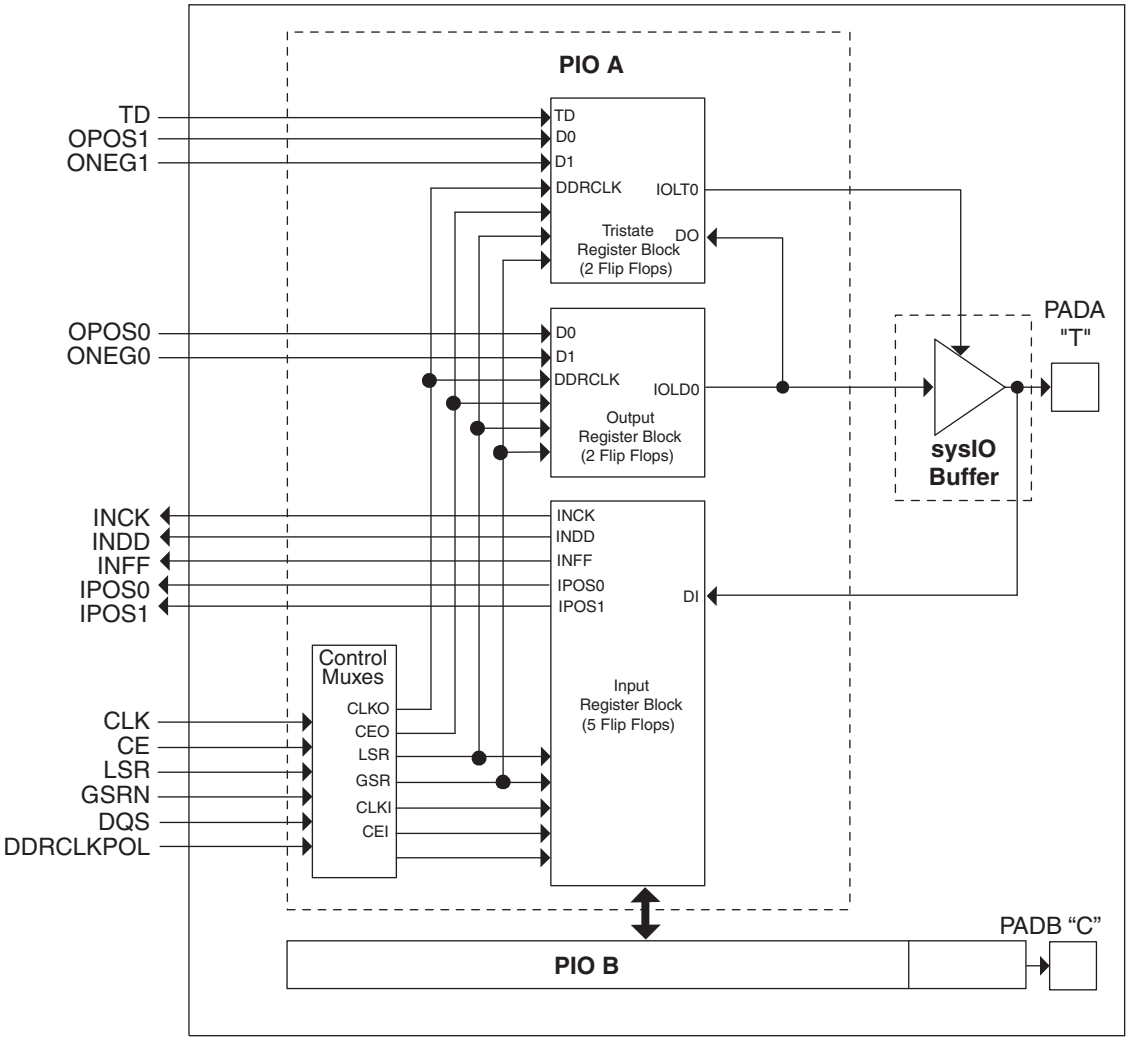
Clock Distribution Network

The clock inputs are selected from external I/O, the sysCLOCK™ PLLs or routing. These clock inputs are fed through the chip via a clock distribution system.

Primary Clock Sources

LatticeXP devices derive clocks from three primary sources: PLL outputs, dedicated clock inputs and routing. LatticeXP devices have two to four sysCLOCK PLLs, located on the left and right sides of the device. There are four dedicated clock inputs, one on each side of the device. Figure 2-5 shows the 20 primary clock sources.

Figure 2-17. PIC Diagram



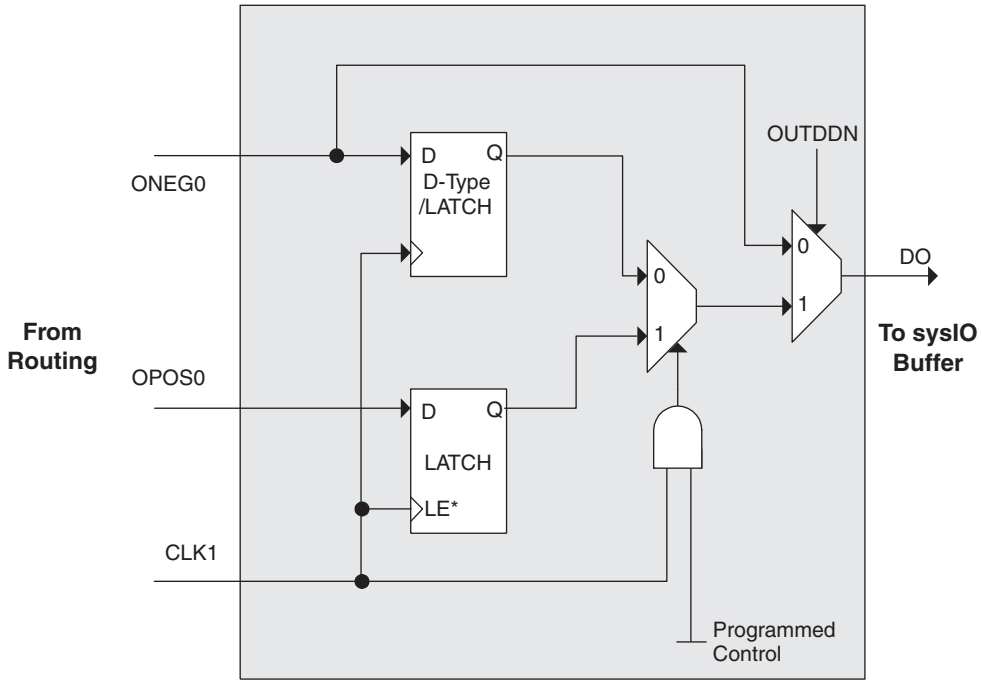
In the LatticeXP family, seven PIOs or four (3.5) PICs are grouped together to provide two LVDS differential pairs, one PIC pair and one single I/O, as shown in Figure 2-18.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”). The PAD Labels “T” and “C” distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 14 PIOs (a group of 8 PICs) contains a delay element to facilitate the generation of DQS signals as shown in Figure 2-19. The DQS signal feeds the DQS bus which spans the set of 13 PIOs (8 PICs). The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

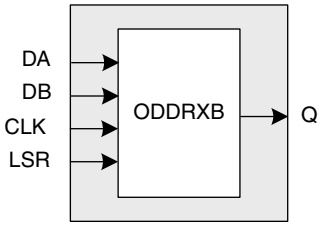
The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table in this data sheet.

Figure 2-23. Output Register Block



*Latch is transparent when input is low.

Figure 2-24. ODDRXB Primitive

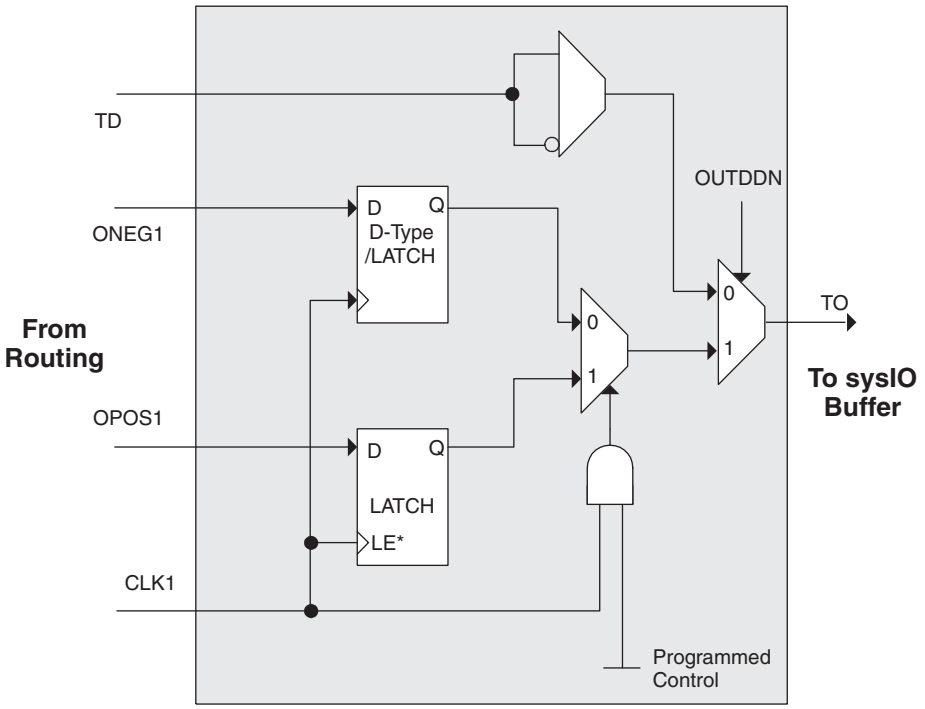


Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-25 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-25. Tristate Register Block



*Latch is transparent when input is low.

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing and a DQS signal provided from the programmable DQS pin. The clock can optionally be inverted.

The clock enable and local reset signals are selected from the routing and optionally inverted. The global tristate signal is passed through this block.

DDR Memory Support

Implementing high performance DDR memory interfaces requires dedicated DDR register structures in the input (for read operations) and in the output (for write operations). As indicated in the PIO Logic section, the LatticeXP devices provide this capability. In addition to these registers, the LatticeXP devices contain two elements to simplify the design of input structures for read operations: the DQS delay block and polarity control logic.

DLL Calibrated DQS Delay Block

Source Synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment, however in DDR memories the clock (referred to as DQS) is not free running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds the polarity control logic which controls the polarity of the clock to the sync registers in the input register blocks. Figures 2-26 and 2-27 show how the polarity control logic are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two DLLs on opposite sides of the device. Each DLL compensates DQS Delays in its half of the device as shown in Figure 2-27. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

Table 2-8. Supported Output Standards

Output Standard	Drive	V_{CCIO} (Nom.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVCMOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVCMOS25	4mA, 8mA, 12mA 16mA, 20mA	2.5
LVCMOS18	4mA, 8mA, 12mA 16mA	1.8
LVCMOS15	4mA, 8mA	1.5
LVCMOS12	2mA, 6mA	1.2
LVCMOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVCMOS15, Open Drain	4mA, 8mA	—
LVCMOS12, Open Drain	2mA. 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II, III	N/A	1.8
HSTL15 Class I, III	N/A	1.5
SSTL3 Class I, II	N/A	3.3
SSTL2 Class I, II	N/A	2.5
SSTL18 Class I	N/A	1.8
Differential Interfaces		
Differential SSTL3, Class I, II	N/A	3.3
Differential SSTL2, Class I, II	N/A	2.5
Differential SSTL18, Class I	N/A	1.8
Differential HSTL18, Class I, II, III	N/A	1.8
Differential HSTL15, Class I, III	N/A	1.5
LVDS	N/A	2.5
BLVDS[1]	N/A	2.5
LVPECL[1]	N/A	3.3

1. Emulated with external resistors.

Hot Socketing

The LatticeXP devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits, which allows easy integration with the rest of the system. These capabilities make the LatticeXP ideal for many multiple power supply and hot-swap applications.

Sleep Mode

The LatticeXP "C" devices (V_{CC} = 1.8/2.5/3.3V) have a sleep mode that allows standby current to be reduced by up to three orders of magnitude during periods of system inactivity. Entry and exit to Sleep Mode is controlled by the SLEEPN pin.

During Sleep Mode, the FPGA logic is non-operational, registers and EBR contents are not maintained and I/Os are tri-stated. Do not enter Sleep Mode during device programming or configuration operation. In Sleep Mode, power supplies can be maintained in their normal operating range, eliminating the need for external switching of power supplies. Table 2-9 compares the characteristics of Normal, Off and Sleep Modes.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 2, 4]	Input or I/O Leakage	$0 \le V_{IN} \le (V_{CCIO} - 0.2V)$	—	—	10	µA
		$(V_{CCIO} - 0.2V) < V_{IN} \le 3.6V$	—	—	40	µA
I_{PU}	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7\ V_{CCIO}$	-30	—	-150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	-150	µA
V_{BHT}	Bus Hold trip Points	$0 \le V_{IN} \le V_{IH}$ (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[3]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Dedicated Input Capacitance[3]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. Not applicable to SLEEPN/TOE pin.
3. T_A 25°C, f = 1.0MHz
4. When V_{IH} is higher than V_{CCIO}, a transient current typically of 30ns in duration or less with a peak current of 6mA can be expected on the high-to-low transition.

Supply Current (Sleep Mode)[1, 2, 3]

Symbol	Parameter	Device	Typ.[4]	Max	Units
I_{CC}	Core Power Supply	LFXP3C	12	65	µA
		LFXP6C	14	75	µA
		LFXP10C	16	85	µA
		LFXP15C	18	95	µA
		LFXP20C	20	105	µA
I_{CCP}	PLL Power Supply (per PLL)	All LFXP 'C' Devices	1	5	µA
I_{CCAUX}	Auxiliary Power Supply	LFXP3C	2	90	µA
		LFXP6C	2	100	µA
		LFXP10C	2	110	µA
		LFXP15C	3	120	µA
		LFXP20C	4	130	µA
I_{CCIO}	Bank Power Supply[5]	LFXP3C	2	20	µA
		LFXP6C	2	22	µA
		LFXP10C	2	24	µA
		LFXP15C	3	27	µA
		LFXP20C	4	30	µA
I_{CCJ}	VCCJ Power Supply	All LFXP 'C' Devices	1	5	µA

1. Assumes all inputs are configured as LVCMOS and held at the VCCIO or GND.
2. Frequency 0MHz.
3. User pattern: blank.
4. T_A=25°C, power supplies at nominal voltage.
5. Per bank.

Derating Logic Timing

Logic timing provided in the following sections of this data sheet and in the ispLEVER design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best-case process can be much better than the values given in the tables. The ispLEVER design tool from Lattice can provide logic timing numbers at a particular temperature and voltage.

Flash Download Time

Symbol	Parameter		Min.	Typ.	Max.	Units
$t_{REFRESH}$	PROGRAMN Low-to-High. Transition to Done High.	LFXP3	—	1.1	1.7	ms
		LFXP6	—	1.4	2.0	ms
		LFXP10	—	0.9	1.5	ms
		LFXP15	—	1.1	1.7	ms
		LFXP20	—	1.3	1.9	ms

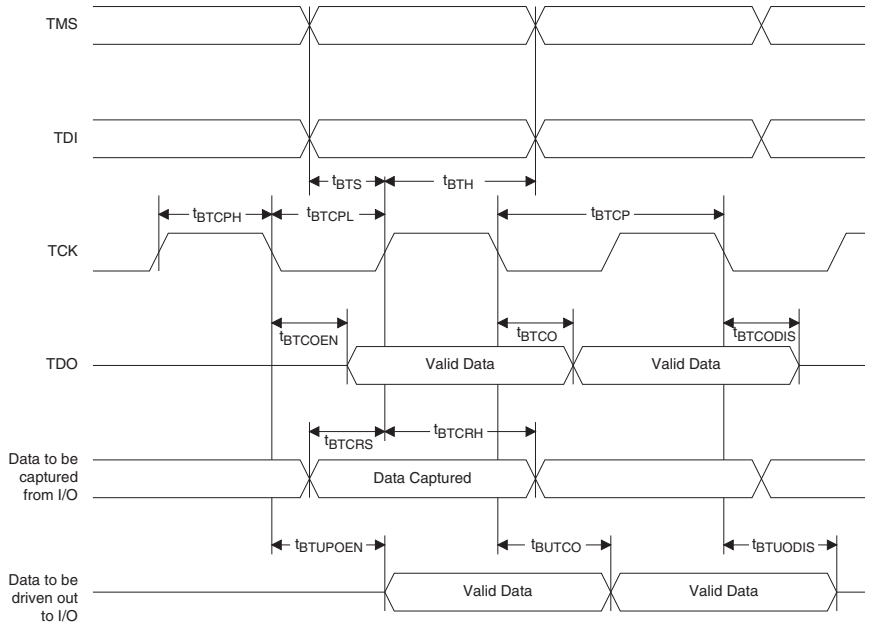
JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f_{MAX}		—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Timing v.F0.11

Figure 3-12. JTAG Port Timing Waveforms



PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO within PIC	Polarity	DDR Strobe (DQS) and Data (DQ) Pins
P[Edge] [n-4]	A	True	DQ
	B	Complement	DQ
P[Edge] [n-3]	A	True	DQ
	B	Complement	DQ
P[Edge] [n-2]	A	True	DQ
	B	Complement	DQ
P[Edge] [n-1]	A	True	DQ
P[Edge] [n]			
	B	Complement	DQ
P[Edge] [n+1]	A	True	[Edge]DQSn
	B	Complement	DQ
P[Edge] [n+2]	A	True	DQ
	B	Complement	DQ
P[Edge] [n+3]	A	True	DQ
	B	Complement	DQ

Notes:
1. “n” is a row/column PIC number.
2. The DDR interface is designed for memories that support one DQS strobe per eight bits of data. In some packages, all the potential DDR data (DQ) pins may not be available.
3. The definition of the PIC numbering is provided in the Signal Names column of the Signal Descriptions table in this data sheet.

LFXP3 Logic Signal Connections: 100 TQFP

Pin Number	Pin Function	Bank	Differential	Dual Function
1	CFG1	0	-	-
2	DONE	0	-	-
3	PROGRAMN	7	-	-
4	CCLK	7	-	-
5	PL3A	7	T	LUM0_PLLT_FB_A
6	PL3B	7	C	LUM0_PLLC_FB_A
7	VCCIO7	7	-	-
8	PL5A	7	-	VREF1_7
9	PL6B	7	-	VREF2_7
10	GNDIO7	7	-	-
11	PL7A	7	T[3]	DQS
12	PL7B	7	C[3]	-
13	PL8A	7	T	LUM0_PLLT_IN_A
14	PL8B	7	C	LUM0_PLLC_IN_A
15	PL9A	7	T[3]	-
16	PL9B	7	C[3]	-
17	VCCP0	-	-	-
18	GNDP0	-	-	-
19	PL12A	6	T	PCLKT6_0
20	PL12B	6	C	PCLKC6_0
21	GNDIO6	6	-	-
22	VCCIO6	6	-	-
23	PL18A	6	T[3]	-
24	PL18B	6	C[3]	-
25	VCCAUX	-	-	-
26	SLEEPN[1]/TOE[2]	-	-	-
27	INITN	5	-	-
28	VCC	-	-	-
29	PB2B	5	-	VREF1_5
30	PB5B	5	-	VREF2_5
31	PB8A	5	T	-
32	PB8B	5	C	-
33	GNDIO5	5	-	-
34	PB9A	5	-	-
35	PB10B	5	-	-
36	PB11A	5	T	DQS
37	PB11B	5	C	-
38	VCCIO5	5	-	-
39	PB12A	5	T	-
40	PB12B	5	C	-
41	PB13A	5	T	-
42	PB13B	5	C	-
43	GND	-	-	-

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
1	CFG1	0	-	-	CFG1	0	-	-
2	DONE	0	-	-	DONE	0	-	-
3	PROGRAMN	7	-	-	PROGRAMN	7	-	-
4	CCLK	7	-	-	CCLK	7	-	-
5	GND	-	-	-	GND	-	-	-
6	PL2A	7	T[3]	-	PL2A	7	T[3]	-
7	GNDIO7	7	-	-	GNDIO7	7	-	-
8	PL2B	7	C[3]	-	PL2B	7	C[3]	-
9	PL3A	7	T	LUM0_PLLT_FB_A	PL3A	7	T	LUM0_PLLT_FB_A
10	PL3B	7	C	LUM0_PLLC_FB_A	PL3B	7	C	LUM0_PLLC_FB_A
11	PL4A	7	T[3]	-	PL4A	7	T[3]	-
12	PL4B	7	C[3]	-	PL4B	7	C[3]	-
13	VCCIO7	7	-	-	VCCIO7	7	-	-
14	PL5A	7	-	VREF1_7	PL5A	7	-	VREF1_7
15	PL6B	7	-	VREF2_7	PL6B	7	-	VREF2_7
16	GNDIO7	7	-	-	GNDIO7	7	-	-
17	PL7A	7	T[3]	DQS	PL7A	7	T[3]	DQS
18	PL7B	7	C[3]	-	PL7B	7	C[3]	-
19	VCC	-	-	-	VCC	-	-	-
20	PL8A	7	T	LUM0_PLLT_IN_A	PL8A	7	T	LUM0_PLLT_IN_A
21	PL8B	7	C	LUM0_PLLC_IN_A	PL8B	7	C	LUM0_PLLC_IN_A
22	PL9A	7	T[3]	-	PL9A	7	T[3]	-
23	VCCIO7	7	-	-	VCCIO7	7	-	-
24	PL9B	7	C[3]	-	PL9B	7	C[3]	-
25	VCCP0	-	-	-	VCCP0	-	-	-
26	GNDP0	-	-	-	GNDP0	-	-	-
27	NC	-	-	-	PL15B	6	-	-
28	VCCIO6	6	-	-	VCCIO6	6	-	-
29	PL11A	6	T[3]	-	PL16A	6	T[3]	-
30	PL11B	6	C[3]	-	PL16B	6	C[3]	-
31	PL12A	6	T	PCLKT6_0	PL17A	6	T	PCLKT6_0
32	PL12B	6	C	PCLKC6_0	PL17B	6	C	PCLKC6_0
33	NC	-	-	-	PL18A	6	T[3]	-
34	NC	-	-	-	PL18B	6	C[3]	-
35	VCC	-	-	-	VCC	-	-	-
36	PL13A	6	T[3]	-	PL21A	6	T[3]	-
37	PL13B	6	C[3]	-	PL21B	6	C[3]	-
38	GNDIO6	6	-	-	GNDIO6	6	-	-
39	PL14A	6	-	VREF1_6	PL22A	6	-	VREF1_6
40	PL15B	6	-	VREF2_6	PL23B	6	-	VREF2_6
41	VCCIO6	6	-	-	VCCIO6	6	-	-
42	PL16A	6	T[3]	DQS	PL24A	6	T[3]	DQS
43	PL16B	6	C[3]	-	PL24B	6	C[3]	-
44	PL17A	6	T	-	PL25A	6	T	-
45	PL17B	6	C	-	PL25B	6	C	-
46	PL18A	6	T[3]	-	PL26A	6	T[3]	-

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP6				LFXP10			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
R8	PB16A	5	T	-	PB20A	5	T	-
T9	PB16B	5	C	-	PB20B	5	C	-
R9	PB17A	4	T	-	PB21A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
P9	PB17B	4	C	-	PB21B	4	C	-
T10	PB18A	4	T	PCLKT4_0	PB22A	4	T	PCLKT4_0
T11	PB18B	4	C	PCLKC4_0	PB22B	4	C	PCLKC4_0
R10	PB19A	4	T	-	PB23A	4	T	-
P10	PB19B	4	C	-	PB23B	4	C	-
N9	PB20A	4	-	-	PB24A	4	-	-
M9	PB21B	4	-	-	PB25B	4	-	-
R12	PB22A	4	T	DQS	PB26A	4	T	DQS
-	GNDIO4	4	-	-	GNDIO4	4	-	-
T12	PB22B	4	C	VREF1_4	PB26B	4	C	VREF1_4
P13	PB23A	4	T	-	PB27A	4	T	-
R13	PB23B	4	C	-	PB27B	4	C	-
M11	PB24A	4	T	-	PB28A	4	T	-
N11	PB24B	4	C	-	PB28B	4	C	-
N10	PB25A	4	T	-	PB29A	4	T	-
M10	PB25B	4	C	-	PB29B	4	C	-
T13	PB26A	4	T	-	PB30A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
P14	PB26B	4	C	-	PB30B	4	C	-
R11	PB27A	4	T	VREF2_4	PB31A	4	T	VREF2_4
P12	PB27B	4	C	-	PB31B	4	C	-
T14	PB28A	4	-	-	PB32A	4	-	-
R14	PB29B	4	-	-	PB33B	4	-	-
P11	PB30A	4	T	DQS	PB34A	4	T	DQS
N12	PB30B	4	C	-	PB34B	4	C	-
T15	PB31A	4	T	-	PB35A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
R15	PB31B	4	C	-	PB35B	4	C	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
P15	PR26B	3	C[3]	-	PR34B	3	C	RLM0_PLLC_FB_A
N15	PR26A	3	T[3]	-	PR34A	3	T	RLM0_PLLT_FB_A
P16	PR24B	3	C[3]	-	PR33B	3	C[3]	-
R16	PR24A	3	T[3]	DQS	PR33A	3	T[3]	DQS
M15	PR15B	3	-	-	PR32B	3	-	-
N14	PR23B	3	-	VREF1_3	PR31A	3	-	VREF1_3
-	GNDIO3	3	-	-	GNDIO3	3	-	-
M14	PR25B	3	C	-	PR29B	3	C	-
L13	PR25A	3	T	-	PR29A	3	T	-

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP6				LFXP10			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
K10	GND	-	-	-	GND	-	-	-
K7	GND	-	-	-	GND	-	-	-
K8	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-
L6	GND	-	-	-	GND	-	-	-
T1	GND	-	-	-	GND	-	-	-
T16	GND	-	-	-	GND	-	-	-
D13	VCC	-	-	-	VCC	-	-	-
D4	VCC	-	-	-	VCC	-	-	-
E12	VCC	-	-	-	VCC	-	-	-
E5	VCC	-	-	-	VCC	-	-	-
M12	VCC	-	-	-	VCC	-	-	-
M5	VCC	-	-	-	VCC	-	-	-
N13	VCC	-	-	-	VCC	-	-	-
N4	VCC	-	-	-	VCC	-	-	-
E13	VCCAUX	-	-	-	VCCAUX	-	-	-
E4	VCCAUX	-	-	-	VCCAUX	-	-	-
M13	VCCAUX	-	-	-	VCCAUX	-	-	-
M4	VCCAUX	-	-	-	VCCAUX	-	-	-
F7	VCCIO0	0	-	-	VCCIO0	0	-	-
F8	VCCIO0	0	-	-	VCCIO0	0	-	-
F10	VCCIO1	1	-	-	VCCIO1	1	-	-
F9	VCCIO1	1	-	-	VCCIO1	1	-	-
G11	VCCIO2	2	-	-	VCCIO2	2	-	-
H11	VCCIO2	2	-	-	VCCIO2	2	-	-
J11	VCCIO3	3	-	-	VCCIO3	3	-	-
K11	VCCIO3	3	-	-	VCCIO3	3	-	-
L10	VCCIO4	4	-	-	VCCIO4	4	-	-
L9	VCCIO4	4	-	-	VCCIO4	4	-	-
L7	VCCIO5	5	-	-	VCCIO5	5	-	-
L8	VCCIO5	5	-	-	VCCIO5	5	-	-
J6	VCCIO6	6	-	-	VCCIO6	6	-	-
K6	VCCIO6	6	-	-	VCCIO6	6	-	-
G6	VCCIO7	7	-	-	VCCIO7	7	-	-
H6	VCCIO7	7	-	-	VCCIO7	7	-	-

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L4	PL32A	6	-	-	PL36A	6	-	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
K4	PL33A	6	T	-	PL37A	6	T	-
K5	PL33B	6	C	-	PL37B	6	C	-
N1	PL35A	6	-	VREF2_6	PL39A	6	-	VREF2_6
N2	PL36B	6	-	-	PL40B	6	-	-
P1	PL37A	6	T[3]	DQS	PL41A	6	T[3]	DQS
P2	PL37B	6	C[3]	-	PL41B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
L5	PL38A	6	T	LLM0_PLLT_FB_A	PL42A	6	T	LLM0_PLLT_FB_A
M6	PL38B	6	C	LLM0_PLLC_FB_A	PL42B	6	C	LLM0_PLLC_FB_A
M3	PL39A	6	T[3]	-	PL43A	6	T[3]	-
N3	PL39B	6	C[3]	-	PL43B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
P4	SLEEPN[1]/TOE[2]	-	-	-	SLEEPN[1]/TOE[2]	-	-	-
P3	INITN	5	-	-	INITN	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
R4	PB11A	5	T	-	PB15A	5	T	-
N5	PB11B	5	C	-	PB15B	5	C	-
P5	PB12A	5	T	VREF1_5	PB16A	5	T	VREF1_5
-	GNDIO5	5	-	-	GNDIO5	5	-	-
R1	PB12B	5	C	-	PB16B	5	C	-
N6	PB13A	5	-	-	PB17A	5	-	-
M7	PB14B	5	-	-	PB18B	5	-	-
R2	PB15A	5	T	DQS	PB19A	5	T	DQS
T2	PB15B	5	C	-	PB19B	5	C	-
R3	PB16A	5	T	-	PB20A	5	T	-
T3	PB16B	5	C	-	PB20B	5	C	-
T4	PB17A	5	T	-	PB21A	5	T	-
R5	PB17B	5	C	VREF2_5	PB21B	5	C	VREF2_5
N7	PB18A	5	T	-	PB22A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
M8	PB18B	5	C	-	PB22B	5	C	-
T5	PB19A	5	T	-	PB23A	5	T	-
P6	PB19B	5	C	-	PB23B	5	C	-
T6	PB20A	5	T	-	PB24A	5	T	-
R6	PB20B	5	C	-	PB24B	5	C	-
P7	PB21A	5	-	-	PB25A	5	-	-
N8	PB22B	5	-	-	PB26B	5	-	-
R7	PB23A	5	T	DQS	PB27A	5	T	DQS

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
F4	PROGRAMN	7	-	-	PROGRAMN	7	-	-	PROGRAMN	7	-	-
G4	CCLK	7	-	-	CCLK	7	-	-	CCLK	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
D2	PL2A	7	T[3]	-	PL6A	7	T[3]	-	PL6A	7	T[3]	-
D1	PL2B	7	C[3]	-	PL6B	7	C[3]	-	PL6B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
E2	PL3A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A
E3	PL3B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A
F3	PL4A	7	T[3]	-	PL8A	7	T[3]	-	PL8A	7	T[3]	-
F2	PL4B	7	C[3]	-	PL8B	7	C[3]	-	PL8B	7	C[3]	-
H4	PL5A	7	-	-	PL9A	7	-	-	PL9A	7	-	-
H3	PL6B	7	-	VREF1_7	PL10B	7	-	VREF1_7	PL10B	7	-	VREF1_7
G3	PL7A	7	T[3]	DQS	PL11A	7	T[3]	DQS	PL11A	7	T[3]	DQS
G2	PL7B	7	C[3]	-	PL11B	7	C[3]	-	PL11B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
F1	PL8A	7	T	-	PL12A	7	T	-	PL12A	7	T	-
E1	PL8B	7	C	-	PL12B	7	C	-	PL12B	7	C	-
J4	PL9A	7	T[3]	-	PL13A	7	T[3]	-	PL13A	7	T[3]	-
K4	PL9B	7	C[3]	-	PL13B	7	C[3]	-	PL13B	7	C[3]	-
G1	PL11A	7	T[3]	-	PL15A	7	T[3]	-	PL15A	7	T[3]	-
H2	PL11B	7	C[3]	-	PL15B	7	C[3]	-	PL15B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
J2	PL12A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A
H1	PL12B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A
J1	PL13A	7	T[3]	-	PL17A	7	T[3]	-	PL17A	7	T[3]	-
K2	PL13B	7	C[3]	-	PL17B	7	C[3]	-	PL17B	7	C[3]	-
K3	PL14A	7	-	VREF2_7	PL18A	7	-	VREF2_7	PL18A	7	-	VREF2_7
J3	PL15B	7	-	-	PL19B	7	-	-	PL19B	7	-	-
K1	PL16A	7	T[3]	DQS	PL20A	7	T[3]	DQS	PL20A	7	T[3]	DQS
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
L2	PL16B	7	C[3]	-	PL20B	7	C[3]	-	PL20B	7	C[3]	-
L3	PL17A	7	T	-	PL21A	7	T	-	PL21A	7	T	-
L4	PL17B	7	C	-	PL21B	7	C	-	PL21B	7	C	-
L1	PL18A	7	T[3]	-	PL22A	7	T[3]	-	PL22A	7	T[3]	-
M1	PL18B	7	C[3]	-	PL22B	7	C[3]	-	PL22B	7	C[3]	-
M2	VCCP0	-	-	-	VCCP0	-	-	-	VCCP0	-	-	-
N1	GNDP0	-	-	-	GNDP0	-	-	-	GNDP0	-	-	-
M3	PL19A	6	T[3]	-	PL23A	6	T[3]	-	PL27A	6	T[3]	-
M4	PL19B	6	C[3]	-	PL23B	6	C[3]	-	PL27B	6	C[3]	-
P1	PL20A	6	T	PCLKT6_0	PL24A	6	T	PCLKT6_0	PL28A	6	T	PCLKT6_0
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
N2	PL20B	6	C	PCLKC6_0	PL24B	6	C	PCLKC6_0	PL28B	6	C	PCLKC6_0
R1	PL21A	6	T[3]	-	PL25A	6	T[3]	-	PL29A	6	T[3]	-
P2	PL21B	6	C[3]	-	PL25B	6	C[3]	-	PL29B	6	C[3]	-
N3	PL22A	6	-	-	PL26A	6	-	-	PL30A	6	-	-
N4	PL23B	6	-	VREF1_6	PL27B	6	-	VREF1_6	PL31B	6	-	VREF1_6
T1	PL24A	6	T[3]	DQS	PL28A	6	T[3]	DQS	PL32A	6	T[3]	DQS
R2	PL24B	6	C[3]	-	PL28B	6	C[3]	-	PL32B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
A7	PT13A	0	T	DI	PT18A	0	T	DI	PT22A	0	T	DI
B7	PT12B	0	C	-	PT17B	0	C	-	PT21B	0	C	-
C6	PT12A	0	T	CSN	PT17A	0	T	CSN	PT21A	0	T	CSN
C10	PT11B	0	C	-	PT16B	0	C	-	PT20B	0	C	-
C9	PT11A	0	T	-	PT16A	0	T	-	PT20A	0	T	-
A6	PT10B	0	C	VREF2_0	PT15B	0	C	VREF2_0	PT19B	0	C	VREF2_0
B6	PT10A	0	T	DQS	PT15A	0	T	DQS	PT19A	0	T	DQS
A5	PT9B	0	-	-	PT14B	0	-	-	PT18B	0	-	-
B5	PT8A	0	-	-	PT13A	0	-	-	PT17A	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C5	PT7B	0	C	-	PT12B	0	C	-	PT16B	0	C	-
A4	PT7A	0	T	-	PT12A	0	T	-	PT16A	0	T	-
D9	PT6B	0	C	-	PT11B	0	C	-	PT15B	0	C	-
D8	PT6A	0	T	-	PT11A	0	T	-	PT15A	0	T	-
B4	PT5B	0	C	-	PT10B	0	C	-	PT14B	0	C	-
A2	PT5A	0	T	-	PT10A	0	T	-	PT14A	0	T	-
A3	PT4B	0	C	-	PT9B	0	C	-	PT13B	0	C	-
B3	PT4A	0	T	-	PT9A	0	T	-	PT13A	0	T	-
C4	PT3B	0	C	-	PT8B	0	C	-	PT12B	0	C	-
C3	PT3A	0	T	-	PT8A	0	T	-	PT12A	0	T	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C2	-	-	-	-	PT7B	0	C	-	PT11B	0	C	-
D3	PT2A	0	-	-	PT7A	0	T	DQS	PT11A	0	T	DQS
D7	-	-	-	-	PT6B	0	-	-	PT10B	0	-	-
D6	-	-	-	-	PT5A	0	-	-	PT9A	0	-	-
E4	-	-	-	-	PT4B	0	C	-	PT8B	0	C	-
D4	-	-	-	-	PT4A	0	T	-	PT8A	0	T	-
D5	-	-	-	-	PT3B	0	-	-	PT7B	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C1	CFG0	0	-	-	CFG0	0	-	-	CFG0	0	-	-
B2	CFG1	0	-	-	CFG1	0	-	-	CFG1	0	-	-
B1	DONE	0	-	-	DONE	0	-	-	DONE	0	-	-
A1	GND	-	-	-	GND	-	-	-	GND	-	-	-
A22	GND	-	-	-	GND	-	-	-	GND	-	-	-
AB1	GND	-	-	-	GND	-	-	-	GND	-	-	-
AB22	GND	-	-	-	GND	-	-	-	GND	-	-	-
H10	GND	-	-	-	GND	-	-	-	GND	-	-	-
H11	GND	-	-	-	GND	-	-	-	GND	-	-	-
H12	GND	-	-	-	GND	-	-	-	GND	-	-	-
H13	GND	-	-	-	GND	-	-	-	GND	-	-	-
H14	GND	-	-	-	GND	-	-	-	GND	-	-	-
J10	GND	-	-	-	GND	-	-	-	GND	-	-	-
J11	GND	-	-	-	GND	-	-	-	GND	-	-	-
J12	GND	-	-	-	GND	-	-	-	GND	-	-	-
J13	GND	-	-	-	GND	-	-	-	GND	-	-	-
J14	GND	-	-	-	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-	GND	-	-	-
K10	GND	-	-	-	GND	-	-	-	GND	-	-	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
K11	GND	-	-	-	GND	-	-	-	GND	-	-	-
K12	GND	-	-	-	GND	-	-	-	GND	-	-	-
K13	GND	-	-	-	GND	-	-	-	GND	-	-	-
K14	GND	-	-	-	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-	GND	-	-	-
L10	GND	-	-	-	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-	GND	-	-	-
L12	GND	-	-	-	GND	-	-	-	GND	-	-	-
L13	GND	-	-	-	GND	-	-	-	GND	-	-	-
L14	GND	-	-	-	GND	-	-	-	GND	-	-	-
L9	GND	-	-	-	GND	-	-	-	GND	-	-	-
M10	GND	-	-	-	GND	-	-	-	GND	-	-	-
M11	GND	-	-	-	GND	-	-	-	GND	-	-	-
M12	GND	-	-	-	GND	-	-	-	GND	-	-	-
M13	GND	-	-	-	GND	-	-	-	GND	-	-	-
M14	GND	-	-	-	GND	-	-	-	GND	-	-	-
M9	GND	-	-	-	GND	-	-	-	GND	-	-	-
N10	GND	-	-	-	GND	-	-	-	GND	-	-	-
N11	GND	-	-	-	GND	-	-	-	GND	-	-	-
N12	GND	-	-	-	GND	-	-	-	GND	-	-	-
N13	GND	-	-	-	GND	-	-	-	GND	-	-	-
N14	GND	-	-	-	GND	-	-	-	GND	-	-	-
N9	GND	-	-	-	GND	-	-	-	GND	-	-	-
P10	GND	-	-	-	GND	-	-	-	GND	-	-	-
P11	GND	-	-	-	GND	-	-	-	GND	-	-	-
P12	GND	-	-	-	GND	-	-	-	GND	-	-	-
P13	GND	-	-	-	GND	-	-	-	GND	-	-	-
P14	GND	-	-	-	GND	-	-	-	GND	-	-	-
P9	GND	-	-	-	GND	-	-	-	GND	-	-	-
R10	GND	-	-	-	GND	-	-	-	GND	-	-	-
R11	GND	-	-	-	GND	-	-	-	GND	-	-	-
R12	GND	-	-	-	GND	-	-	-	GND	-	-	-
R13	GND	-	-	-	GND	-	-	-	GND	-	-	-
R14	GND	-	-	-	GND	-	-	-	GND	-	-	-
H9	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
J15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
J8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
K15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
K8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
L15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
L8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
M15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
M8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
N15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
N8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
P15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
P8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
R9	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
G16	VCCAUX	-	-	-	VCCAUX	-	-	-	VCCAUX	-	-	-

Lead-free Packaging

Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3C-3QN208C	136	1.8/2.5/3.3V	-3	PQFP	208	COM	3.1K
LFXP3C-4QN208C	136	1.8/2.5/3.3V	-4	PQFP	208	COM	3.1K
LFXP3C-5QN208C	136	1.8/2.5/3.3V	-5	PQFP	208	COM	3.1K
LFXP3C-3TN144C	100	1.8/2.5/3.3V	-3	TQFP	144	COM	3.1K
LFXP3C-4TN144C	100	1.8/2.5/3.3V	-4	TQFP	144	COM	3.1K
LFXP3C-5TN144C	100	1.8/2.5/3.3V	-5	TQFP	144	COM	3.1K
LFXP3C-3TN100C	62	1.8/2.5/3.3V	-3	TQFP	100	COM	3.1K
LFXP3C-4TN100C	62	1.8/2.5/3.3V	-4	TQFP	100	COM	3.1K
LFXP3C-5TN100C	62	1.8/2.5/3.3V	-5	TQFP	100	COM	3.1K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6C-3FN256C	188	1.8/2.5/3.3V	-3	fpBGA	256	COM	5.8K
LFXP6C-4FN256C	188	1.8/2.5/3.3V	-4	fpBGA	256	COM	5.8K
LFXP6C-5FN256C	188	1.8/2.5/3.3V	-5	fpBGA	256	COM	5.8K
LFXP6C-3QN208C	142	1.8/2.5/3.3V	-3	PQFP	208	COM	5.8K
LFXP6C-4QN208C	142	1.8/2.5/3.3V	-4	PQFP	208	COM	5.8K
LFXP6C-5QN208C	142	1.8/2.5/3.3V	-5	PQFP	208	COM	5.8K
LFXP6C-3TN144C	100	1.8/2.5/3.3V	-3	TQFP	144	COM	5.8K
LFXP6C-4TN144C	100	1.8/2.5/3.3V	-4	TQFP	144	COM	5.8K
LFXP6C-5TN144C	100	1.8/2.5/3.3V	-5	TQFP	144	COM	5.8K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10C-3FN388C	244	1.8/2.5/3.3V	-3	fpBGA	388	COM	9.7K
LFXP10C-4FN388C	244	1.8/2.5/3.3V	-4	fpBGA	388	COM	9.7K
LFXP10C-5FN388C	244	1.8/2.5/3.3V	-5	fpBGA	388	COM	9.7K
LFXP10C-3FN256C	188	1.8/2.5/3.3V	-3	fpBGA	256	COM	9.7K
LFXP10C-4FN256C	188	1.8/2.5/3.3V	-4	fpBGA	256	COM	9.7K
LFXP10C-5FN256C	188	1.8/2.5/3.3V	-5	fpBGA	256	COM	9.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15C-3FN484C	300	1.8/2.5/3.3V	-3	fpBGA	484	COM	15.5K
LFXP15C-4FN484C	300	1.8/2.5/3.3V	-4	fpBGA	484	COM	15.5K
LFXP15C-5FN484C	300	1.8/2.5/3.3V	-5	fpBGA	484	COM	15.5K
LFXP15C-3FN388C	268	1.8/2.5/3.3V	-3	fpBGA	388	COM	15.5K
LFXP15C-4FN388C	268	1.8/2.5/3.3V	-4	fpBGA	388	COM	15.5K
LFXP15C-5FN388C	268	1.8/2.5/3.3V	-5	fpBGA	388	COM	15.5K
LFXP15C-3FN256C	188	1.8/2.5/3.3V	-3	fpBGA	256	COM	15.5K
LFXP15C-4FN256C	188	1.8/2.5/3.3V	-4	fpBGA	256	COM	15.5K
LFXP15C-5FN256C	188	1.8/2.5/3.3V	-5	fpBGA	256	COM	15.5K

LatticeXP Family Data Sheet Revision History

November 2007 **Data Sheet DS1001**

Revision History

Date	Version	Section	Change Summary
February 2005	01.0	—	Initial release.
April 2005	01.1	Architecture	EBR memory support section updated with clarification.
May 2005	01.2	Introduction	Added TransFR Reconfiguration to Features section.
		Architecture	Added TransFR section.
June 2005	01.3	Pinout Information	Added pinout information for LFXP3, LFXP6, LFXP15 and LFXP20.
July 2005	02.0	Introduction	Updated XP6, XP15 and XP20 EBR SRAM Bits and Block numbers.
		Architecture	Updated Per Quadrant Primary Clock Selection figure.
			Added Typical I/O Behavior During Power-up section.
			Updated Device Configuration section under Configuration and Testing.
		DC and Switching Characteristics	Clarified Hot Socketing Specification
			Updated Supply Current (Standby) Table
			Updated Initialization Supply Current Table
			Added Programming and Erase Flash Supply Current table
			Added LVDS Emulation section. Updated LVDS25E Output Termination Example figure and LVDS25E DC Conditions table.
			Updated Differential LVPECL diagram and LVPECL DC Conditions table.
			Deleted 5V Tolerant Input Buffer section. Updated RSDS figure and RSDS DC Conditions table.
			Updated sysCONFIG Port Timing Specifications
			Updated JTAG Port Timing Specifications. Added Flash Download Time table.
		Pinout Information	Updated Signal Descriptions table.
			Updated Logic Signal Connections Dual Function column.
		Ordering Information	Added lead-free ordering part numbers.
July 2005	02.1	DC and Switching Characteristics	Clarification of Flash Programming Junction Temperature
August 2005	02.2	Introduction	Added Sleep Mode feature.
		Architecture	Added Sleep Mode section.
		DC and Switching Characteristics	Added Sleep Mode Supply Current Table
			Added Sleep Mode Timing section
		Pinout Information	Added SLEEPN and TOE signal names, descriptions and footnotes.
			Added SLEEPN and TOE to pinout information and footnotes.
			Added footnote 3 to Logic Signal Connections tables for clarification on emulated LVDS output.
September 2005	03.0	Architecture	Added clarification of PCI clamp.
			Added clarification to SLEEPN Pin Characteristics section.
		DC and Switching Characteristics	DC Characteristics, added footnote 4 for clarification. Updated Supply Current (Sleep Mode), Supply Current (Standby), Initialization Supply Current, and Programming and Erase Flash Supply Current typical numbers.