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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	20000
Total RAM Bits	405504
Number of I/O	340
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp20c-5f484c

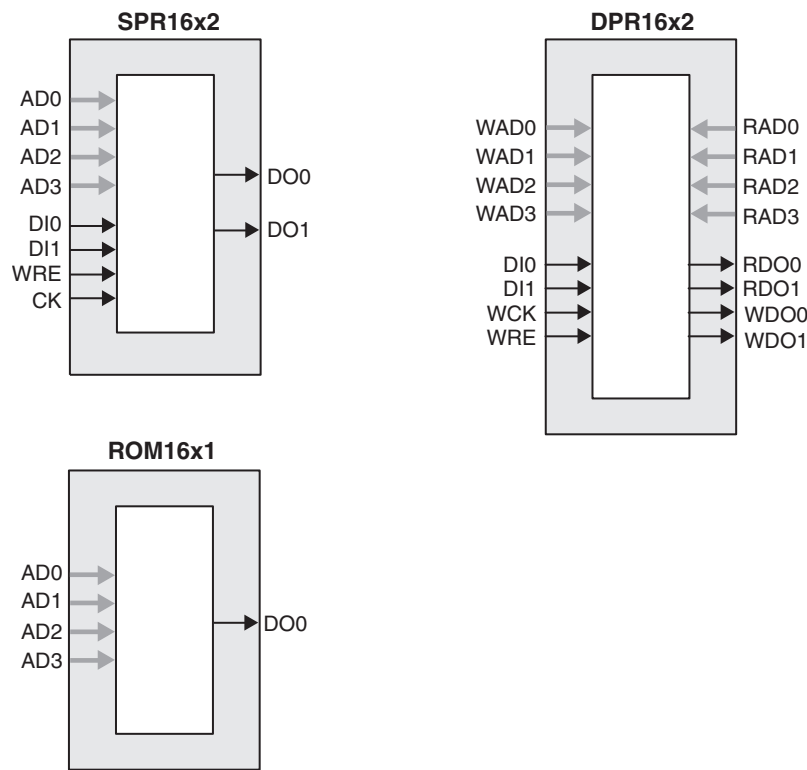
The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-4 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices, one Slice functions as the read-write port. The other companion Slice supports the read-only port. For more information on RAM mode in LatticeXP devices, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required for Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of Slices	1	2

Note: SPR = Single Port RAM, DPR = Dual Port RAM

Figure 2-4. Distributed Memory Primitives



ROM Mode: The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

Figure 2-26. DQS Local Bus

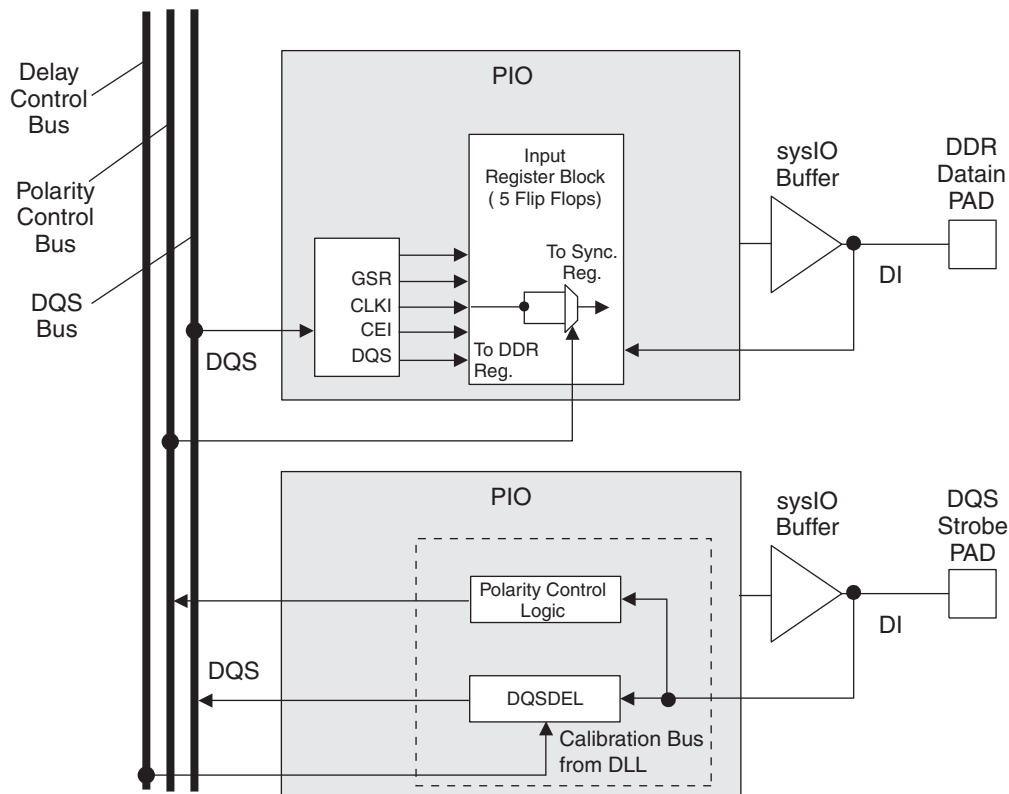


Figure 2-27. DLL Calibration Bus and DQS/DQS Transition Distribution

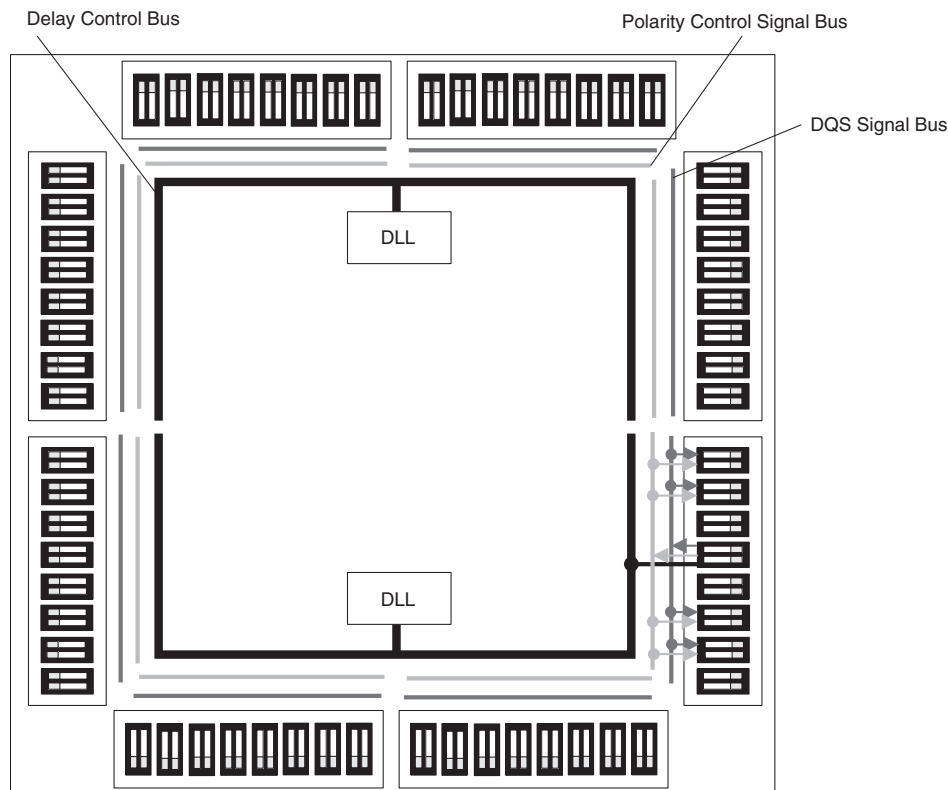
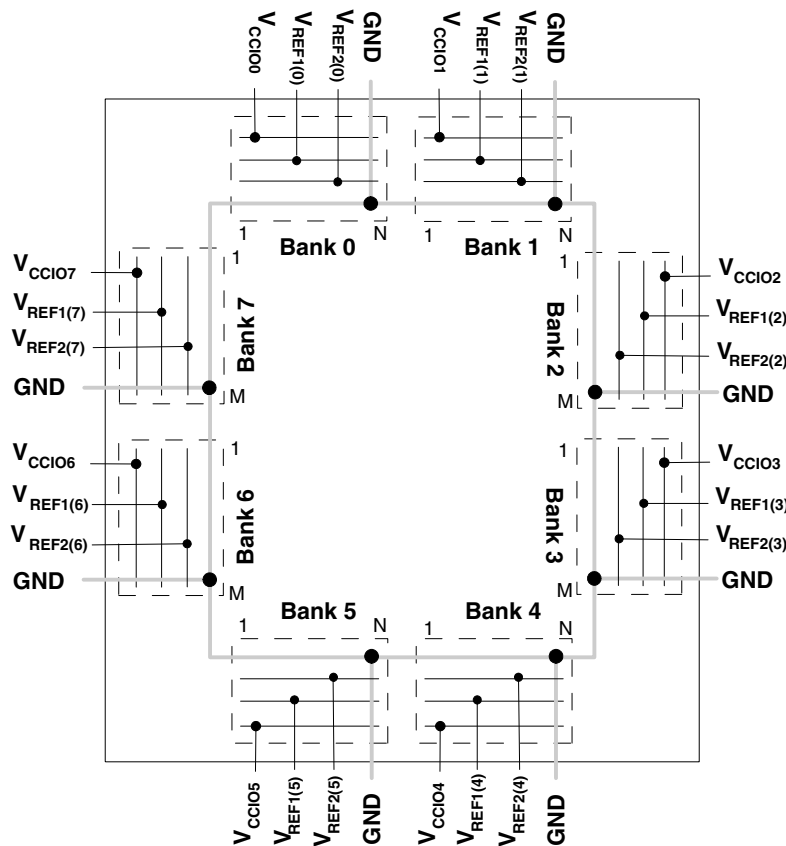


Figure 2-28. LatticeXP Banks



Note: N and M are the maximum number of I/Os per bank.

LatticeXP devices contain two types of sysIO buffer pairs.

1. Top and Bottom sysIO Buffer Pair (Single-Ended Outputs Only)

The sysIO buffer pairs in the top and bottom banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Only the I/Os on the top and bottom banks have PCI clamps. Note that the PCI clamp is enabled after V_{CC} , V_{CCAUX} and V_{CCIO} are at valid operating levels and the device has been configured.

2. Left and Right sysIO Buffer Pair (Differential and Single-Ended Outputs)

The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. The referenced input buffer can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

Select I/Os in the left and right banks have LVDS differential output drivers. Refer to the Logic Signal Connections tables for more information.

Absolute Maximum Ratings^{1, 2, 3, 4}

	XPE (1.2V)	XPC (1.8V/2.5V/3.3V)
Supply Voltage V_{CC}	-0.5 to 1.32V	-0.5 to 3.75V
Supply Voltage V_{CCP}	-0.5 to 1.32V	-0.5 to 3.75V
Supply Voltage V_{CCAUX}	-0.5 to 3.75V	-0.5 to 3.75V
Supply Voltage V_{CCJ}	-0.5 to 3.75V	-0.5 to 3.75V
Output Supply Voltage V_{CCIO}	-0.5 to 3.75V	-0.5 to 3.75V
I/O Tristate Voltage Applied ⁵	-0.5 to 3.75V	-0.5 to 3.75V
Dedicated Input Voltage Applied ⁵	-0.5 to 3.75V	-0.5 to 4.25V
Storage Temperature (Ambient)	-65 to 150°C	-65 to 150°C
Junction Temp. (Tj)	+125°C	+125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions outside of those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. All chip grounds are connected together to a common package GND plane.
5. Overshoot and undershoot of -2V to ($V_{IHMAX} + 2$) volts is permitted for a duration of <20ns.

Recommended Operating Conditions³

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Core Supply Voltage for 1.2V Devices	1.14	1.26	V
	Core Supply Voltage for 1.8V/2.5V/3.3V Devices	1.71	3.465	V
V_{CCP}	Supply Voltage for PLL for 1.2V Devices	1.14	1.26	V
	Supply Voltage for PLL for 1.8V/2.5V/3.3V Devices	1.71	3.465	V
V_{CCAUX} ⁴	Auxiliary Supply Voltage	3.135	3.465	V
V_{CCIO} ^{1, 2}	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ} ¹	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	85	C
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	C
$t_{JFLASHCOM}$	Junction Temperature, Flash Programming, Commercial	0	85	C
$t_{JFLASHIND}$	Junction Temperature, Flash Programming, Industrial	0	85	C

1. If V_{CCIO} or V_{CCJ} is set to 3.3V, they must be connected to the same power supply as V_{CCAUX} . For the XPE devices (1.2V V_{CC}), if V_{CCIO} or V_{CCJ} is set to 1.2V, they must be connected to the same power supply as V_{CC} .
2. See recommended voltages by I/O standard in subsequent table.
3. The system designer must ensure that the FPGA design stays within the specified junction temperature and package thermal capabilities of the device based on the expected operating frequency, activity factor and environment conditions of the system.
4. V_{CCAUX} ramp rate must not exceed 30mV/ μ s during power up when transitioning between 0V and 3.3V.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{IL}, I_{IH}^{1, 2, 4}$	Input or I/O Leakage	$0 \leq V_{IN} \leq (V_{CCIO} - 0.2V)$	—	—	10	μA
		$(V_{CCIO} - 0.2V) < V_{IN} \leq 3.6V$	—	—	40	μA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7 V_{CCIO}$	-30	—	-150	μA
I_{PD}	I/O Active Pull-down Current	$V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MAX)$	30	—	150	μA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL} (MAX)$	30	—	—	μA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	-30	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	150	μA
I_{BHHO}	Bus Hold High Overdrive current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	-150	μA
V_{BHT}	Bus Hold trip Points	$0 \leq V_{IN} \leq V_{IH} (MAX)$	$V_{IL} (MAX)$	—	$V_{IH} (MIN)$	V
C1	I/O Capacitance ³	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,$ $V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—	8	—	pf
C2	Dedicated Input Capacitance ³	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,$ $V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—	8	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. Not applicable to SLEEPN/TOE pin.

3. $T_A = 25^\circ C$, $f = 1.0MHz$

4. When V_{IH} is higher than V_{CCIO} , a transient current typically of 30ns in duration or less with a peak current of 6mA can be expected on the high-to-low transition.

Supply Current (Sleep Mode)^{1, 2, 3}

Symbol	Parameter	Device	Typ. ⁴	Max	Units
I_{CC}	Core Power Supply	LFXP3C	12	65	μA
		LFXP6C	14	75	μA
		LFXP10C	16	85	μA
		LFXP15C	18	95	μA
		LFXP20C	20	105	μA
I_{CCP}	PLL Power Supply (per PLL)	All LFXP 'C' Devices	1	5	μA
I_{CCAUX}	Auxiliary Power Supply	LFXP3C	2	90	μA
		LFXP6C	2	100	μA
		LFXP10C	2	110	μA
		LFXP15C	3	120	μA
		LFXP20C	4	130	μA
I_{CCIO}	Bank Power Supply ⁵	LFXP3C	2	20	μA
		LFXP6C	2	22	μA
		LFXP10C	2	24	μA
		LFXP15C	3	27	μA
		LFXP20C	4	30	μA
I_{CCJ}	VCCJ Power Supply	All LFXP 'C' Devices	1	5	μA

1. Assumes all inputs are configured as LVCMOS and held at the VCCIO or GND.

2. Frequency 0MHz.

3. User pattern: blank.

4. $T_A = 25^\circ C$, power supplies at nominal voltage.

5. Per bank.

Supply Current (Standby)^{1, 2, 3, 4}**Over Recommended Operating Conditions**

Symbol	Parameter	Device	Typ. ⁵	Units
I_{CC}	Core Power Supply	LFXP3E	15	mA
		LFXP6E	20	mA
		LFXP10E	35	mA
		LFXP15E	45	mA
		LFXP20E	55	mA
		LFXP3C	35	mA
		LFXP6C	40	mA
		LFXP10C	70	mA
		LFXP15C	80	mA
		LFXP20C	90	mA
I_{CCP}	PLL Power Supply (per PLL)	All	8	mA
I_{CCAUX}	Auxiliary Power Supply $V_{CCAUX} = 3.3V$	LFXP3E/C	22	mA
		LFXP6E/C	22	mA
		LFXP10E/C	30	mA
		LFXP15E/C	30	mA
		LFXP20E/C	30	mA
I_{CCIO}	Bank Power Supply ⁶	All	2	mA
I_{CCJ}	V_{CCJ} Power Supply	All	1	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the VCCIO or GND.

3. Frequency 0MHz.

4. User pattern: blank.

5. $T_A=25^{\circ}C$, power supplies at nominal voltage.

6. Per bank.

LatticeXP Internal Timing Parameters¹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register	—	1.61	—	1.94	—	2.32	ns
PLL Parameters								
t _{RSTREC}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
t _{RSTSU}	Reset Signal Setup Time	1.00	—	1.00	—	1.00	—	ns

1. Internal parameters are characterized but not tested on every device.
Timing v.F0.11

Power Supply and NC Connections

Signals	100 TQFP	144 TQFP	208 PQFP	256 fpBGA	388 fpBGA	484 fpBGA
V _{CC}	28, 77	14, 39, 73, 112	19, 35, 53, 80, 107, 151, 158, 182	D4, D13, E5, E12, M5, M12, N4, N13	H9, J8, J15, K8, K15, L8, L15, M8, M15, N8, N15, P8, P15, R9	F10, F13, G9, G10, G13, G14, H8, H15, J7, J16, K6, K7, K16, K17, N6, N7, N16, N17, P7, P16, R8, R15, T9, T10, T13, T14, U10, U13
V _{CCIO0}	94	133	189, 199	F7, F8	G8, G9, G10, G11, H8	F11, G11, H10, H11
V _{CCIO1}	82	119	167, 177	F9, F10	G12, G13, G14, G15, H15	F12, G12, H12, H13
V _{CCIO2}	65	98	140, 149	G11, H11	H16, J16, K16, L16	K15, L15, L16, L17
V _{CCIO3}	58	88	115, 125	J11, K11	M16, N16, P16, R16	M15, M16, M17, N15
V _{CCIO4}	47	61, 68	87, 97	L9, L10	R15, T12, T13, T14, T15	R12, R13, T12, U12
V _{CCIO5}	38	49	64, 74	L7, L8	R8, T8, T9, T10, T11	R10, R11, T11, U11
V _{CCIO6}	22	21	28, 41	J6, K6	M7, N7, P7, R7	M6, M7, M8, N8
V _{CCIO7}	7	8	13, 23	G6, H6	H7, J7, K7, L7	K8, L6, L7, L8
V _{CCJ}	73	108	154	D16	E20	E20
V _{CCP0}	17	19	25	H4	M2	L5
V _{CCP1}	60	91	128	J12	M21	L18
V _{CCAUX}	25, 71	36, 106	50, 152	E4, E13, M4, M13	G7, G16, T7, T16	G7, G8, G15, G16, H7, H16, R7, R16, T7, T8, T15, T16
GND ¹	10, 18, 21, 33, 43, 44, 52, 59, 68, 84, 90, 99	3, 11, 20, 28, 44, 54, 56, 64, 75, 85, 90, 101, 121, 127, 136	5, 7, 16, 26, 38, 47, 49, 59, 69, 79, 82, 92, 106, 109, 118, 121, 127, 130, 135, 143, 163, 172, 181, 184, 194, 207	A1, A16, F6, F11, G7, G8, G9, G10, H5, H7, H8, H9, H10, J7, J8, J9, J10, J13, K7, K8, K9, K10, L6, L11, T1, T16	A1, A22, H10, H11, H12, H13, H14, J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N1, N9, N10, N11, N12, N13, N14, N22, P9, P10, P11, P12, P13, P14, R10, R11, R12, R13, R14, AB1, AB22	A1, A2, A21, A22, B1, B22, H9, H14, J8, J9, J10, J11, J12, J13, J14, J15, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, M20, N2, N9, N10, N11, N12, N13, N14, P8, P9, P10, P11, P12, P13, P14, P15, R9, R14, AA1, AA22, AB1, AB2, AB21, AB22
NC ²	—	—	XP3: 27, 33, 34, 129, 133, 134	—	XP10: C2, C15, C16, C17, D4, D5, D6, D7, D16, D17, E4, E19, W3, W4, W7, W17, W18, W19, W20, Y3, Y15, Y16, AA1, AA2	XP15: B21, C4, C5, C6, C18, C19, C20, C21, D6, D18, E4, E6, E18, F6, L1, L19, L20, M1, M2, M19, M21, N1, N21, N22, P1, P2, U5, U6, U17, U18, V5, V6, V17, V18, W17, W18, W19, Y3, Y4, Y5

1. All grounds must be electrically connected at the board level.

2. NC pins should not be connected to any active signals, V_{CC} or GND.

LFXP3 Logic Signal Connections: 100 TQFP

Pin Number	Pin Function	Bank	Differential	Dual Function
1	CFG1	0	-	-
2	DONE	0	-	-
3	PROGRAMN	7	-	-
4	CCLK	7	-	-
5	PL3A	7	T	LUM0_PLLT_FB_A
6	PL3B	7	C	LUM0_PLLC_FB_A
7	VCCIO7	7	-	-
8	PL5A	7	-	VREF1_7
9	PL6B	7	-	VREF2_7
10	GNDIO7	7	-	-
11	PL7A	7	T ³	DQS
12	PL7B	7	C ³	-
13	PL8A	7	T	LUM0_PLLT_IN_A
14	PL8B	7	C	LUM0_PLLC_IN_A
15	PL9A	7	T ³	-
16	PL9B	7	C ³	-
17	VCCP0	-	-	-
18	GNDP0	-	-	-
19	PL12A	6	T	PCLKT6_0
20	PL12B	6	C	PCLKC6_0
21	GNDIO6	6	-	-
22	VCCIO6	6	-	-
23	PL18A	6	T ³	-
24	PL18B	6	C ³	-
25	VCCAUX	-	-	-
26	SLEEPN ¹ /TOE ²	-	-	-
27	INITN	5	-	-
28	VCC	-	-	-
29	PB2B	5	-	VREF1_5
30	PB5B	5	-	VREF2_5
31	PB8A	5	T	-
32	PB8B	5	C	-
33	GNDIO5	5	-	-
34	PB9A	5	-	-
35	PB10B	5	-	-
36	PB11A	5	T	DQS
37	PB11B	5	C	-
38	VCCIO5	5	-	-
39	PB12A	5	T	-
40	PB12B	5	C	-
41	PB13A	5	T	-
42	PB13B	5	C	-
43	GND	-	-	-

LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
139	PT6A	0	-	DI	PT9A	0	-	DI
140	PT5A	0	-	CSN	PT8A	0	-	CSN
141	PT3B	0	-	VREF2_0	PT6B	0	-	VREF2_0
142	CFG0	0	-	-	CFG0	0	-	-
143	CFG1	0	-	-	CFG1	0	-	-
144	DONE	0	-	-	DONE	0	-	-

1. Applies to LFXP "C" only.
2. Applies to LFXP "E" only.
3. Supports dedicated LVDS outputs.

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
185	PT13A	0	T	CS1N	PT16A	0	T	CS1N
186	PT12B	0	C	PCLKC0_0	PT15B	0	C	PCLKC0_0
187	PT12A	0	T	PCLKT0_0	PT15A	0	T	PCLKT0_0
188	PT11B	0	C	-	PT14B	0	C	-
189	VCCIO0	0	-	-	VCCIO0	0	-	-
190	PT11A	0	T	DQS	PT14A	0	T	DQS
191	PT10B	0	-	-	PT13B	0	-	-
192	PT9A	0	-	DOUT	PT12A	0	-	DOUT
193	PT8B	0	C	-	PT11B	0	C	-
194	GNDIO0	0	-	-	GNDIO0	0	-	-
195	PT8A	0	T	WRITEN	PT11A	0	T	WRITEN
196	PT7B	0	C	-	PT10B	0	C	-
197	PT7A	0	T	VREF1_0	PT10A	0	T	VREF1_0
198	PT6B	0	C	-	PT9B	0	C	-
199	VCCIO0	0	-	-	VCCIO0	0	-	-
200	PT6A	0	T	DI	PT9A	0	T	DI
201	PT5B	0	C	-	PT8B	0	C	-
202	PT5A	0	T	CSN	PT8A	0	T	CSN
203	PT4B	0	C	-	PT7B	0	C	-
204	PT4A	0	T	-	PT7A	0	T	-
205	PT3B	0	-	VREF2_0	PT6B	0	-	VREF2_0
206	PT2B	0	-	-	PT5B	0	-	-
207	GND	-	-	-	GND	-	-	-
208	CFG0	0	-	-	CFG0	0	-	-

1. Applies to LFXP "C" only.
2. Applies to LFXP "E" only.
3. Supports dedicated LVDS outputs.

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
T7	PB23B	5	C	-	PB27B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
P8	PB24A	5	T	-	PB28A	5	T	-
T8	PB24B	5	C	-	PB28B	5	C	-
R8	PB25A	5	T	-	PB29A	5	T	-
T9	PB25B	5	C	-	PB29B	5	C	-
R9	PB26A	4	T	-	PB30A	4	T	-
P9	PB26B	4	C	-	PB30B	4	C	-
T10	PB27A	4	T	PCLKT4_0	PB31A	4	T	PCLKT4_0
T11	PB27B	4	C	PCLKC4_0	PB31B	4	C	PCLKC4_0
-	GNDIO4	4	-	-	GNDIO4	4	-	-
R10	PB28A	4	T	-	PB32A	4	T	-
P10	PB28B	4	C	-	PB32B	4	C	-
N9	PB29A	4	-	-	PB33A	4	-	-
M9	PB30B	4	-	-	PB34B	4	-	-
R12	PB31A	4	T	DQS	PB35A	4	T	DQS
T12	PB31B	4	C	VREF1_4	PB35B	4	C	VREF1_4
P13	PB32A	4	T	-	PB36A	4	T	-
R13	PB32B	4	C	-	PB36B	4	C	-
M11	PB33A	4	T	-	PB37A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
N11	PB33B	4	C	-	PB37B	4	C	-
N10	PB34A	4	T	-	PB38A	4	T	-
M10	PB34B	4	C	-	PB38B	4	C	-
T13	PB35A	4	T	-	PB39A	4	T	-
P14	PB35B	4	C	-	PB39B	4	C	-
R11	PB36A	4	T	VREF2_4	PB40A	4	T	VREF2_4
P12	PB36B	4	C	-	PB40B	4	C	-
T14	PB37A	4	-	-	PB41A	4	-	-
R14	PB38B	4	-	-	PB42B	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
P11	PB39A	4	T	DQS	PB43A	4	T	DQS
N12	PB39B	4	C	-	PB43B	4	C	-
T15	PB40A	4	T	-	PB44A	4	T	-
R15	PB40B	4	C	-	PB44B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
P15	PR38B	3	C	RLM0_PLLC_FB_A	PR42B	3	C	RLM0_PLLC_FB_A
N15	PR38A	3	T	RLM0_PLLT_FB_A	PR42A	3	T	RLM0_PLLT_FB_A

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
Y10	PB11B	5	C	-	PB16B	5	C	-	PB20B	5	C	-
AA7	PB12A	5	T	-	PB17A	5	T	-	PB21A	5	T	-
AB7	PB12B	5	C	VREF2_5	PB17B	5	C	VREF2_5	PB21B	5	C	VREF2_5
Y7	PB13A	5	T	-	PB18A	5	T	-	PB22A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
AA8	PB13B	5	C	-	PB18B	5	C	-	PB22B	5	C	-
AB8	PB14A	5	T	-	PB19A	5	T	-	PB23A	5	T	-
Y8	PB14B	5	C	-	PB19B	5	C	-	PB23B	5	C	-
AB9	PB15A	5	T	-	PB20A	5	T	-	PB24A	5	T	-
AA9	PB15B	5	C	-	PB20B	5	C	-	PB24B	5	C	-
W10	PB16A	5	-	-	PB21A	5	-	-	PB25A	5	-	-
W11	PB17B	5	-	-	PB22B	5	-	-	PB26B	5	-	-
AB10	PB18A	5	T	DQS	PB23A	5	T	DQS	PB27A	5	T	DQS
AA10	PB18B	5	C	-	PB23B	5	C	-	PB27B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
AA11	PB19A	5	T	-	PB24A	5	T	-	PB28A	5	T	-
AB11	PB19B	5	C	-	PB24B	5	C	-	PB28B	5	C	-
Y11	PB20A	5	T	-	PB25A	5	T	-	PB29A	5	T	-
Y12	PB20B	5	C	-	PB25B	5	C	-	PB29B	5	C	-
AB12	PB21A	4	T	-	PB26A	4	T	-	PB30A	4	T	-
AA12	PB21B	4	C	-	PB26B	4	C	-	PB30B	4	C	-
AB13	PB22A	4	T	PCLKT4_0	PB27A	4	T	PCLKT4_0	PB31A	4	T	PCLKT4_0
AA13	PB22B	4	C	PCLKC4_0	PB27B	4	C	PCLKC4_0	PB31B	4	C	PCLKC4_0
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA14	PB23A	4	T	-	PB28A	4	T	-	PB32A	4	T	-
AB14	PB23B	4	C	-	PB28B	4	C	-	PB32B	4	C	-
W12	PB24A	4	-	-	PB29A	4	-	-	PB33A	4	-	-
W13	PB25B	4	-	-	PB30B	4	-	-	PB34B	4	-	-
AA15	PB26A	4	T	DQS	PB31A	4	T	DQS	PB35A	4	T	DQS
AB15	PB26B	4	C	VREF1_4	PB31B	4	C	VREF1_4	PB35B	4	C	VREF1_4
AA16	PB27A	4	T	-	PB32A	4	T	-	PB36A	4	T	-
AB16	PB27B	4	C	-	PB32B	4	C	-	PB36B	4	C	-
Y17	PB28A	4	T	-	PB33A	4	T	-	PB37A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA17	PB28B	4	C	-	PB33B	4	C	-	PB37B	4	C	-
Y13	PB29A	4	T	-	PB34A	4	T	-	PB38A	4	T	-
Y14	PB29B	4	C	-	PB34B	4	C	-	PB38B	4	C	-
AB17	PB30A	4	T	-	PB35A	4	T	-	PB39A	4	T	-
Y18	PB30B	4	C	-	PB35B	4	C	-	PB39B	4	C	-
AA18	PB31A	4	T	VREF2_4	PB36A	4	T	VREF2_4	PB40A	4	T	VREF2_4
AB18	PB31B	4	C	-	PB36B	4	C	-	PB40B	4	C	-
Y19	PB32A	4	-	-	PB37A	4	-	-	PB41A	4	-	-
AB19	PB33B	4	-	-	PB38B	4	-	-	PB42B	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA19	PB34A	4	T	DQS	PB39A	4	T	DQS	PB43A	4	T	DQS
Y20	PB34B	4	C	-	PB39B	4	C	-	PB43B	4	C	-
W14	PB35A	4	T	-	PB40A	4	T	-	PB44A	4	T	-
W15	PB35B	4	C	-	PB40B	4	C	-	PB44B	4	C	-
AB20	PB36A	4	T	-	PB41A	4	T	-	PB45A	4	T	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
K11	GND	-	-	-	GND	-	-	-	GND	-	-	-
K12	GND	-	-	-	GND	-	-	-	GND	-	-	-
K13	GND	-	-	-	GND	-	-	-	GND	-	-	-
K14	GND	-	-	-	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-	GND	-	-	-
L10	GND	-	-	-	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-	GND	-	-	-
L12	GND	-	-	-	GND	-	-	-	GND	-	-	-
L13	GND	-	-	-	GND	-	-	-	GND	-	-	-
L14	GND	-	-	-	GND	-	-	-	GND	-	-	-
L9	GND	-	-	-	GND	-	-	-	GND	-	-	-
M10	GND	-	-	-	GND	-	-	-	GND	-	-	-
M11	GND	-	-	-	GND	-	-	-	GND	-	-	-
M12	GND	-	-	-	GND	-	-	-	GND	-	-	-
M13	GND	-	-	-	GND	-	-	-	GND	-	-	-
M14	GND	-	-	-	GND	-	-	-	GND	-	-	-
M9	GND	-	-	-	GND	-	-	-	GND	-	-	-
N10	GND	-	-	-	GND	-	-	-	GND	-	-	-
N11	GND	-	-	-	GND	-	-	-	GND	-	-	-
N12	GND	-	-	-	GND	-	-	-	GND	-	-	-
N13	GND	-	-	-	GND	-	-	-	GND	-	-	-
N14	GND	-	-	-	GND	-	-	-	GND	-	-	-
N9	GND	-	-	-	GND	-	-	-	GND	-	-	-
P10	GND	-	-	-	GND	-	-	-	GND	-	-	-
P11	GND	-	-	-	GND	-	-	-	GND	-	-	-
P12	GND	-	-	-	GND	-	-	-	GND	-	-	-
P13	GND	-	-	-	GND	-	-	-	GND	-	-	-
P14	GND	-	-	-	GND	-	-	-	GND	-	-	-
P9	GND	-	-	-	GND	-	-	-	GND	-	-	-
R10	GND	-	-	-	GND	-	-	-	GND	-	-	-
R11	GND	-	-	-	GND	-	-	-	GND	-	-	-
R12	GND	-	-	-	GND	-	-	-	GND	-	-	-
R13	GND	-	-	-	GND	-	-	-	GND	-	-	-
R14	GND	-	-	-	GND	-	-	-	GND	-	-	-
H9	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
J15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
J8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
K15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
K8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
L15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
L8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
M15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
M8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
N15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
N8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
P15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
P8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
R9	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
G16	VCCAUX	-	-	-	VCCAUX	-	-	-	VCCAUX	-	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
F5	PROGRAMN	7	-	-	PROGRAMN	7	-	-
E3	CCLK	7	-	-	CCLK	7	-	-
C1	PL2B	7	-	-	PL2B	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
G5	PL3A	7	T ³	-	PL3A	7	T ³	-
G6	PL3B	7	C ³	-	PL3B	7	C ³	-
F4	PL4A	7	T	-	PL4A	7	T	-
F3	PL4B	7	C	-	PL4B	7	C	-
G4	PL5A	7	T ³	-	PL5A	7	T ³	-
G3	PL5B	7	C ³	-	PL5B	7	C ³	-
D1	PL6A	7	T ³	-	PL6A	7	T ³	-
D2	PL6B	7	C ³	-	PL6B	7	C ³	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
E1	PL7A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A
E2	PL7B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A
H5	PL8A	7	T ³	-	PL8A	7	T ³	-
H6	PL8B	7	C ³	-	PL8B	7	C ³	-
H4	PL9A	7	-	-	PL9A	7	-	-
H3	PL10B	7	-	VREF1_7	PL10B	7	-	VREF1_7
F1	PL11A	7	T ³	DQS	PL11A	7	T ³	DQS
F2	PL11B	7	C ³	-	PL11B	7	C ³	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
J5	PL12A	7	T	-	PL12A	7	T	-
J6	PL12B	7	C	-	PL12B	7	C	-
G1	PL13A	7	T ³	-	PL13A	7	T ³	-
G2	PL13B	7	C ³	-	PL13B	7	C ³	-
J4	PL15A	7	T ³	-	PL15A	7	T ³	-
J3	PL15B	7	C ³	-	PL15B	7	C ³	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
H1	PL16A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A
H2	PL16B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A
J1	PL17A	7	T ³	-	PL17A	7	T ³	-
J2	PL17B	7	C ³	-	PL17B	7	C ³	-
K3	PL18A	7	-	VREF2_7	PL18A	7	-	VREF2_7
K2	PL19B	7	-	-	PL19B	7	-	-
K4	PL20A	7	T ³	DQS	PL20A	7	T ³	DQS
-	GNDIO7	7	-	-	GNDIO7	7	-	-
K5	PL20B	7	C ³	-	PL20B	7	C ³	-
K1	PL21A	7	T	-	PL21A	7	T	-
L2	PL21B	7	C	-	PL21B	7	C	-
L4	PL22A	7	T ³	-	PL22A	7	T ³	-
L3	PL22B	7	C ³	-	PL22B	7	C ³	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
AB5	PB16A	5	T	-	PB20A	5	T	-
AB6	PB16B	5	C	-	PB20B	5	C	-
AA8	PB17A	5	T	-	PB21A	5	T	-
AA9	PB17B	5	C	VREF2_5	PB21B	5	C	VREF2_5
W10	PB18A	5	T	-	PB22A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
V10	PB18B	5	C	-	PB22B	5	C	-
AB7	PB19A	5	T	-	PB23A	5	T	-
AB8	PB19B	5	C	-	PB23B	5	C	-
AB9	PB20A	5	T	-	PB24A	5	T	-
AB10	PB20B	5	C	-	PB24B	5	C	-
Y10	PB21A	5	-	-	PB25A	5	-	-
AA10	PB22B	5	-	-	PB26B	5	-	-
W11	PB23A	5	T	DQS	PB27A	5	T	DQS
V11	PB23B	5	C	-	PB27B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y11	PB24A	5	T	-	PB28A	5	T	-
AA11	PB24B	5	C	-	PB28B	5	C	-
AB11	PB25A	5	T	-	PB29A	5	T	-
AB12	PB25B	5	C	-	PB29B	5	C	-
Y12	PB26A	4	T	-	PB30A	4	T	-
AA12	PB26B	4	C	-	PB30B	4	C	-
W12	PB27A	4	T	PCLKT4_0	PB31A	4	T	PCLKT4_0
V12	PB27B	4	C	PCLKC4_0	PB31B	4	C	PCLKC4_0
-	GNDIO4	4	-	-	GNDIO4	4	-	-
AB13	PB28A	4	T	-	PB32A	4	T	-
AB14	PB28B	4	C	-	PB32B	4	C	-
AA13	PB29A	4	-	-	PB33A	4	-	-
Y13	PB30B	4	-	-	PB34B	4	-	-
AB15	PB31A	4	T	DQS	PB35A	4	T	DQS
AB16	PB31B	4	C	VREF1_4	PB35B	4	C	VREF1_4
V13	PB32A	4	T	-	PB36A	4	T	-
W13	PB32B	4	C	-	PB36B	4	C	-
AA14	PB33A	4	T	-	PB37A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA15	PB33B	4	C	-	PB37B	4	C	-
AB17	PB34A	4	T	-	PB38A	4	T	-
AB18	PB34B	4	C	-	PB38B	4	C	-
W14	PB35A	4	T	-	PB39A	4	T	-
Y14	PB35B	4	C	-	PB39B	4	C	-
U14	PB36A	4	T	VREF2_4	PB40A	4	T	VREF2_4
V14	PB36B	4	C	-	PB40B	4	C	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
J15	GND	-	-	-	GND	-	-	-
J8	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-
K10	GND	-	-	-	GND	-	-	-
K11	GND	-	-	-	GND	-	-	-
K12	GND	-	-	-	GND	-	-	-
K13	GND	-	-	-	GND	-	-	-
K14	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-
L10	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-
L12	GND	-	-	-	GND	-	-	-
L13	GND	-	-	-	GND	-	-	-
L14	GND	-	-	-	GND	-	-	-
L9	GND	-	-	-	GND	-	-	-
M10	GND	-	-	-	GND	-	-	-
M11	GND	-	-	-	GND	-	-	-
M12	GND	-	-	-	GND	-	-	-
M13	GND	-	-	-	GND	-	-	-
M14	GND	-	-	-	GND	-	-	-
M9	GND	-	-	-	GND	-	-	-
N10	GND	-	-	-	GND	-	-	-
N11	GND	-	-	-	GND	-	-	-
N12	GND	-	-	-	GND	-	-	-
N13	GND	-	-	-	GND	-	-	-
N14	GND	-	-	-	GND	-	-	-
N9	GND	-	-	-	GND	-	-	-
P10	GND	-	-	-	GND	-	-	-
P11	GND	-	-	-	GND	-	-	-
P12	GND	-	-	-	GND	-	-	-
P13	GND	-	-	-	GND	-	-	-
P14	GND	-	-	-	GND	-	-	-
P15	GND	-	-	-	GND	-	-	-
P8	GND	-	-	-	GND	-	-	-
P9	GND	-	-	-	GND	-	-	-
R14	GND	-	-	-	GND	-	-	-
R9	GND	-	-	-	GND	-	-	-
F10	VCC	-	-	-	VCC	-	-	-
F13	VCC	-	-	-	VCC	-	-	-
G10	VCC	-	-	-	VCC	-	-	-
G13	VCC	-	-	-	VCC	-	-	-
G14	VCC	-	-	-	VCC	-	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
G9	VCC	-	-	-	VCC	-	-	-
H15	VCC	-	-	-	VCC	-	-	-
H8	VCC	-	-	-	VCC	-	-	-
J16	VCC	-	-	-	VCC	-	-	-
J7	VCC	-	-	-	VCC	-	-	-
K16	VCC	-	-	-	VCC	-	-	-
K17	VCC	-	-	-	VCC	-	-	-
K6	VCC	-	-	-	VCC	-	-	-
K7	VCC	-	-	-	VCC	-	-	-
N16	VCC	-	-	-	VCC	-	-	-
N17	VCC	-	-	-	VCC	-	-	-
N6	VCC	-	-	-	VCC	-	-	-
N7	VCC	-	-	-	VCC	-	-	-
P16	VCC	-	-	-	VCC	-	-	-
P7	VCC	-	-	-	VCC	-	-	-
R15	VCC	-	-	-	VCC	-	-	-
R8	VCC	-	-	-	VCC	-	-	-
T10	VCC	-	-	-	VCC	-	-	-
T13	VCC	-	-	-	VCC	-	-	-
T14	VCC	-	-	-	VCC	-	-	-
T9	VCC	-	-	-	VCC	-	-	-
U10	VCC	-	-	-	VCC	-	-	-
U13	VCC	-	-	-	VCC	-	-	-
G15	VCCAUX	-	-	-	VCCAUX	-	-	-
G16	VCCAUX	-	-	-	VCCAUX	-	-	-
G7	VCCAUX	-	-	-	VCCAUX	-	-	-
G8	VCCAUX	-	-	-	VCCAUX	-	-	-
H16	VCCAUX	-	-	-	VCCAUX	-	-	-
H7	VCCAUX	-	-	-	VCCAUX	-	-	-
R16	VCCAUX	-	-	-	VCCAUX	-	-	-
R7	VCCAUX	-	-	-	VCCAUX	-	-	-
T15	VCCAUX	-	-	-	VCCAUX	-	-	-
T16	VCCAUX	-	-	-	VCCAUX	-	-	-
T7	VCCAUX	-	-	-	VCCAUX	-	-	-
T8	VCCAUX	-	-	-	VCCAUX	-	-	-
F11	VCCIO0	0	-	-	VCCIO0	0	-	-
G11	VCCIO0	0	-	-	VCCIO0	0	-	-
H10	VCCIO0	0	-	-	VCCIO0	0	-	-
H11	VCCIO0	0	-	-	VCCIO0	0	-	-
F12	VCCIO1	1	-	-	VCCIO1	1	-	-
G12	VCCIO1	1	-	-	VCCIO1	1	-	-
H12	VCCIO1	1	-	-	VCCIO1	1	-	-

Industrial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15E-3F484I	300	1.2V	-3	fpBGA	484	IND	15.5K
LFXP15E-4F484I	300	1.2V	-4	fpBGA	484	IND	15.5K
LFXP15E-3F388I	268	1.2V	-3	fpBGA	388	IND	15.5K
LFXP15E-4F388I	268	1.2V	-4	fpBGA	388	IND	15.5K
LFXP15E-3F256I	188	1.2V	-3	fpBGA	256	IND	15.5K
LFXP15E-4F256I	188	1.2V	-4	fpBGA	256	IND	15.5K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20E-3F484I	340	1.2V	-3	fpBGA	484	IND	19.7K
LFXP20E-4F484I	340	1.2V	-4	fpBGA	484	IND	19.7K
LFXP20E-3F388I	268	1.2V	-3	fpBGA	388	IND	19.7K
LFXP20E-4F388I	268	1.2V	-4	fpBGA	388	IND	19.7K
LFXP20E-3F256I	188	1.2V	-3	fpBGA	256	IND	19.7K
LFXP20E-4F256I	188	1.2V	-4	fpBGA	256	IND	19.7K

Revision History

Date	Version	Section	Change Summary
February 2005	01.0	—	Initial release.
April 2005	01.1	Architecture	EBR memory support section updated with clarification.
May 2005	01.2	Introduction	Added TransFR Reconfiguration to Features section.
		Architecture	Added TransFR section.
June 2005	01.3	Pinout Information	Added pinout information for LFXP3, LFXP6, LFXP15 and LFXP20.
July 2005	02.0	Introduction	Updated XP6, XP15 and XP20 EBR SRAM Bits and Block numbers.
		Architecture	Updated Per Quadrant Primary Clock Selection figure.
			Added Typical I/O Behavior During Power-up section.
			Updated Device Configuration section under Configuration and Testing.
	02.0	DC and Switching Characteristics	Clarified Hot Socketing Specification
			Updated Supply Current (Standby) Table
			Updated Initialization Supply Current Table
			Added Programming and Erase Flash Supply Current table
			Added LVDS Emulation section. Updated LVDS25E Output Termination Example figure and LVDS25E DC Conditions table.
			Updated Differential LVPECL diagram and LVPECL DC Conditions table.
			Deleted 5V Tolerant Input Buffer section. Updated RSDS figure and RSDS DC Conditions table.
			Updated sysCONFIG Port Timing Specifications
			Updated JTAG Port Timing Specifications. Added Flash Download Time table.
		Pinout Information	Updated Signal Descriptions table.
		Ordering Information	Updated Logic Signal Connections Dual Function column.
			Added lead-free ordering part numbers.
July 2005	02.1	DC and Switching Characteristics	Clarification of Flash Programming Junction Temperature
August 2005	02.2	Introduction	Added Sleep Mode feature.
		Architecture	Added Sleep Mode section.
		DC and Switching Characteristics	Added Sleep Mode Supply Current Table
			Added Sleep Mode Timing section
		Pinout Information	Added SLEEPN and TOE signal names, descriptions and footnotes.
			Added SLEEPN and TOE to pinout information and footnotes.
September 2005	03.0	Architecture	Added footnote 3 to Logic Signal Connections tables for clarification on emulated LVDS output.
			Added clarification of PCI clamp.
		DC and Switching Characteristics	Added clarification to SLEEPN Pin Characteristics section.
			DC Characteristics, added footnote 4 for clarification. Updated Supply Current (Sleep Mode), Supply Current (Standby), Initialization Supply Current, and Programming and Erase Flash Supply Current typical numbers.