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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	20000
Total RAM Bits	405504
Number of I/O	268
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	388-BBGA
Supplier Device Package	388-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp20c-5fn388c

Features

■ Non-volatile, Infinitely Reconfigurable

- Instant-on – powers up in microseconds
- No external configuration memory
- Excellent design security, no bit stream to intercept
- Reconfigure SRAM based logic in milliseconds
- SRAM and non-volatile memory programmable through system configuration and JTAG ports

■ Sleep Mode

- Allows up to 1000x static current reduction

■ TransFR™ Reconfiguration (TFR)

- In-field logic update while system operates

■ Extensive Density and Package Options

- 3.1K to 19.7K LUT4s
- 62 to 340 I/Os
- Density migration supported

■ Embedded and Distributed Memory

- 54 Kbits to 396 Kbits sysMEM™ Embedded Block RAM
- Up to 79 Kbits distributed RAM
- Flexible memory resources:
 - Distributed and block memory

■ Flexible I/O Buffer

- Programmable sysIO™ buffer supports wide range of interfaces:
 - LVCMOS 3.3/2.5/1.8/1.5/1.2
 - LVTTTL
 - SSTL 18 Class I
 - SSTL 3/2 Class I, II
 - HSTL15 Class I, III
 - HSTL 18 Class I, II, III
 - PCI
 - LVDS, Bus-LVDS, LVPECL, RSDS

■ Dedicated DDR Memory Support

- Implements interface up to DDR333 (166MHz)

■ sysCLOCK™ PLLs

- Up to 4 analog PLLs per device
- Clock multiply, divide and phase shifting

■ System Level Support

- IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
- Onboard oscillator for configuration
- Devices operate with 3.3V, 2.5V, 1.8V or 1.2V power supply

Table 1-1. LatticeXP Family Selection Guide

Device	LFXP3	LFXP6	LFXP10	LFXP15	LFXP20
PFU/PFF Rows	16	24	32	40	44
PFU/PFF Columns	24	30	38	48	56
PFU/PFF (Total)	384	720	1216	1932	2464
LUTs (K)	3	6	10	15	20
Distributed RAM (KBits)	12	23	39	61	79
EBR SRAM (KBits)	54	72	216	324	396
EBR SRAM Blocks	6	8	24	36	44
V _{CC} Voltage	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V
PLLs	2	2	4	4	4
Max. I/O	136	188	244	300	340
Packages and I/O Combinations:					
100-pin TQFP (14 x 14 mm)	62				
144-pin TQFP (20 x 20 mm)	100	100			
208-pin PQFP (28 x 28 mm)	136	142			
256-ball fpBGA (17 x 17 mm)		188	188	188	188
388-ball fpBGA (23 x 23 mm)			244	268	268
484-ball fpBGA (23 x 23 mm)				300	340

Table 2-6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

Figure 2-14 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

Figure 2-29 provides a pictorial representation of the different programming ports and modes available in the LatticeXP devices.

On power-up, the FPGA SRAM is ready to be configured with the sysCONFIG port active. The IEEE 1149.1 serial mode can be activated any time after power-up by sending the appropriate command through the TAP port.

Leave Alone I/O

When using 1532 mode for non-volatile memory programming, users may specify I/Os as high, low, tristated or held at current value. This provides excellent flexibility for implementing systems where reprogramming occurs on-the-fly.

TransFR (Transparent Field Reconfiguration)

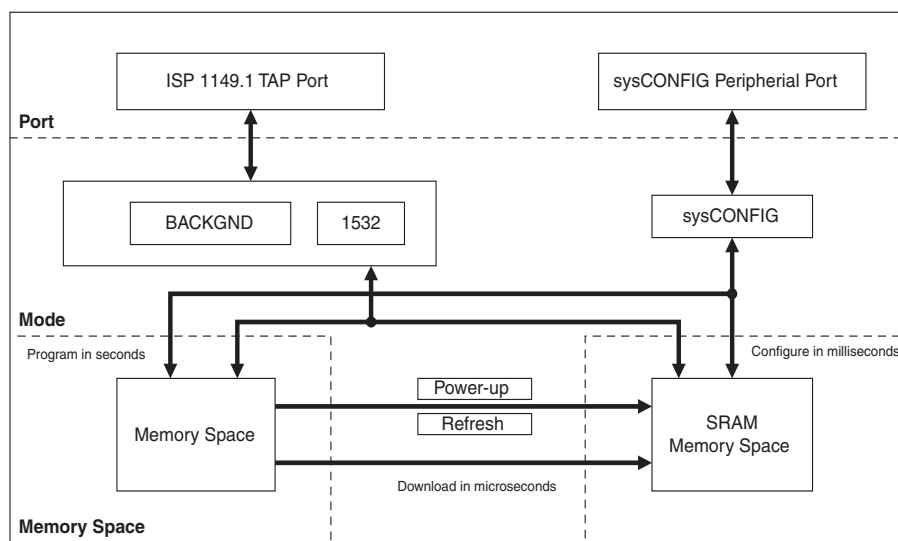
TransFR (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. See Lattice technical note #TN1087, *Minimizing System Interruption During Configuration Using TransFR Technology*, for details.

Security

The LatticeXP devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile memory spaces. Once set, the only way to clear security bits is to erase the memory space.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

Figure 2-29. ispXP Block Diagram



Internal Logic Analyzer Capability (ispTRACY)

All LatticeXP devices support an internal logic analyzer diagnostic feature. The diagnostic features provide capabilities similar to an external logic analyzer, such as programmable event and trigger condition and deep trace memory. This feature is enabled by Lattice's ispTRACY. The ispTRACY utility is added into the user design at compile time.

For more information on ispTRACY, please see information regarding additional technical documentation at the end of this data sheet.

Oscillator

Every LatticeXP device has an internal CMOS oscillator which is used to derive a master serial clock for configuration. The oscillator and the master serial clock run continuously in the configuration mode. The default value of the

Absolute Maximum Ratings^{1, 2, 3, 4}

	XPE (1.2V)	XPC (1.8V/2.5V/3.3V)
Supply Voltage V_{CC}	-0.5 to 1.32V	-0.5 to 3.75V
Supply Voltage V_{CCP}	-0.5 to 1.32V	-0.5 to 3.75V
Supply Voltage V_{CCAUX}	-0.5 to 3.75V	-0.5 to 3.75V
Supply Voltage V_{CCJ}	-0.5 to 3.75V	-0.5 to 3.75V
Output Supply Voltage V_{CCIO}	-0.5 to 3.75V	-0.5 to 3.75V
I/O Tristate Voltage Applied ⁵	-0.5 to 3.75V	-0.5 to 3.75V
Dedicated Input Voltage Applied ⁵	-0.5 to 3.75V	-0.5 to 4.25V
Storage Temperature (Ambient)	-65 to 150°C	-65 to 150°C
Junction Temp. (Tj)	+125°C	+125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions outside of those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. All chip grounds are connected together to a common package GND plane.
5. Overshoot and undershoot of -2V to ($V_{IHMAX} + 2$) volts is permitted for a duration of <20ns.

Recommended Operating Conditions³

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Core Supply Voltage for 1.2V Devices	1.14	1.26	V
	Core Supply Voltage for 1.8V/2.5V/3.3V Devices	1.71	3.465	V
V_{CCP}	Supply Voltage for PLL for 1.2V Devices	1.14	1.26	V
	Supply Voltage for PLL for 1.8V/2.5V/3.3V Devices	1.71	3.465	V
V_{CCAUX}^4	Auxiliary Supply Voltage	3.135	3.465	V
$V_{CCIO}^{1, 2}$	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}^1	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	85	C
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	C
$t_{JFLASHCOM}$	Junction Temperature, Flash Programming, Commercial	0	85	C
$t_{JFLASHIND}$	Junction Temperature, Flash Programming, Industrial	0	85	C

1. If V_{CCIO} or V_{CCJ} is set to 3.3V, they must be connected to the same power supply as V_{CCAUX} . For the XPE devices (1.2V V_{CC}), if V_{CCIO} or V_{CCJ} is set to 1.2V, they must be connected to the same power supply as V_{CC} .
2. See recommended voltages by I/O standard in subsequent table.
3. The system designer must ensure that the FPGA design stays within the specified junction temperature and package thermal capabilities of the device based on the expected operating frequency, activity factor and environment conditions of the system.
4. V_{CCAUX} ramp rate must not exceed 30mV/ μ s during power up when transitioning between 0V and 3.3V.

sysCLOCK PLL Timing**Over Recommended Operating Conditions**

Parameter	Descriptions	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		25	—	375	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		25	—	375	MHz
f_{OUT2}	K-Divider Output Frequency (CLKOK)		0.195	—	187.5	MHz
f_{VCO}	PLL VCO Frequency		375	—	750	MHz
f_{PFD}	Phase Detector Input Frequency		25	—	—	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default duty cycle elected ³	45	50	55	%
t_{PH}^4	Output Phase Accuracy		—	—	0.05	UI
t_{OPJIT}^1	Output Clock Period Jitter	$f_{OUT} \geq 100\text{MHz}$	—	—	+/- 125	ps
		$f_{OUT} < 100\text{MHz}$	—	—	0.02	UIPP
t_{SK}	Input Clock to Output Clock Skew	Divider ratio = integer	—	—	+/- 200	ps
t_W	Output Clock Pulse Width	At 90% or 10% ³	1	—	—	ns
t_{LOCK}^2	PLL Lock-in Time		—	—	150	us
t_{PA}	Programmable Delay Unit		100	250	400	ps
t_{IPJIT}	Input Clock Period Jitter		—	—	+/- 200	ps
t_{FBKDLy}	External Feedback Delay		—	—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t_{RST}	RST Pulse Width		10	—	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

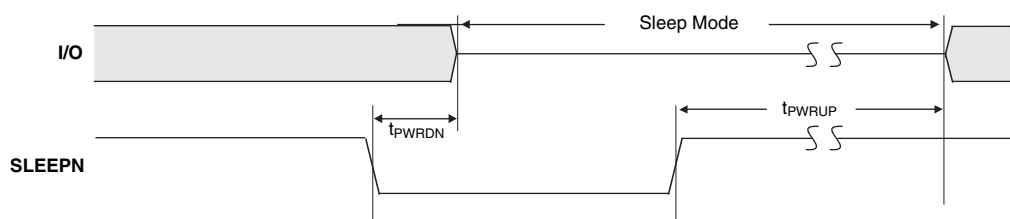
3. Using LVDS output buffers.

4. As compared to CLKOP output.

Timing v.F0.11

LatticeXP “C” Sleep Mode Timing

Parameter	Descriptions	Min.	Typ.	Max.	Units
t_{PWRDN}	SLEEPN Low to I/O Tristate	—	20	32	ns
t_{PWRUP}	SLEEPN High to Power Up	LFXP3	—	1.4	ms
		LFXP6	—	1.7	ms
		LFXP10	—	1.1	ms
		LFXP15	—	1.4	ms
		LFXP20	—	1.7	ms
$t_{WSLEEPN}$	SLEEPN Pulse Width to Initiate Sleep Mode	400	—	—	ns
t_{WAWAKE}	SLEEPN Pulse Rejection	—	—	120	ns



Switching Test Conditions

Figure 3-13 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Figure 3-5.

Figure 3-13. Output Test Load, LVTTTL and LVCMOS Standards

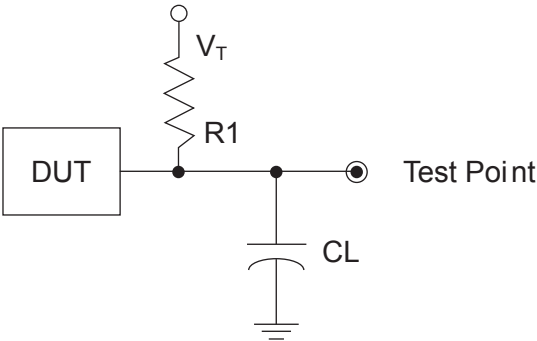


Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R ₁	C _L	Timing Ref.	V _T
LVTTTL and other LVCMOS settings (L -> H, H -> L)	∞	0pF	LVCMOS 3.3 = 1.5V	—
			LVCMOS 2.5 = V _{CCIO} /2	—
			LVCMOS 1.8 = V _{CCIO} /2	—
			LVCMOS 1.5 = V _{CCIO} /2	—
			LVCMOS 1.2 = V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z -> H)	188	0pF	V _{CCIO} /2	V _{OL}
LVCMOS 2.5 I/O (Z -> L)			V _{CCIO} /2	V _{OH}
LVCMOS 2.5 I/O (H -> Z)			V _{OH} - 0.15	V _{OL}
LVCMOS 2.5 I/O (L -> Z)			V _{OL} + 0.15	V _{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
93	PB19B	4	C	VREF1_4	PB22B	4	C	VREF1_4
94	PB20A	4	T	-	PB23A	4	T	-
95	PB20B	4	C	-	PB23B	4	C	-
96	PB21A	4	T	-	PB24A	4	T	-
97	VCCIO4	4	-	-	VCCIO4	4	-	-
98	PB21B	4	C	-	PB24B	4	C	-
99	PB22A	4	T	-	PB25A	4	T	-
100	PB22B	4	C	-	PB25B	4	C	-
101	PB23A	4	T	-	PB26A	4	T	-
102	PB23B	4	C	-	PB26B	4	C	-
103	PB24A	4	T	VREF2_4	PB27A	4	-	VREF2_4
104	PB24B	4	C	-	PB30A	4	T	DQS
105	PB25A	4	-	-	PB30B	4	C	-
106	GND	-	-	-	GND	-	-	-
107	VCC	-	-	-	VCC	-	-	-
108	PR18B	3	C ³	-	PR26B	3	C ³	-
109	GNDIO3	3	-	-	GNDIO3	3	-	-
110	PR18A	3	T ³	-	PR26A	3	T ³	-
111	PR17B	3	C	-	PR25B	3	C	-
112	PR17A	3	T	-	PR25A	3	T	-
113	PR16B	3	C ³	-	PR24B	3	C ³	-
114	PR16A	3	T ³	DQS	PR24A	3	T ³	DQS
115	VCCIO3	3	-	-	VCCIO3	3	-	-
116	PR15B	3	-	VREF1_3	PR23B	3	-	VREF1_3
117	PR14A	3	-	VREF2_3	PR22A	3	-	VREF2_3
118	GNDIO3	3	-	-	GNDIO3	3	-	-
119	PR13B	3	C	-	PR21B	3	C ³	-
120	PR13A	3	T	-	PR21A	3	T ³	-
121	GND	-	-	-	GND	-	-	-
122	PR12B	3	C	-	PR20B	3	C	-
123	PR12A	3	T	-	PR20A	3	T	-
124	PR11B	3	C	-	PR19B	3	C ³	-
125	VCCIO3	3	-	-	VCCIO3	3	-	-
126	PR11A	3	T	-	PR19A	3	T ³	-
127	GNDP1	-	-	-	GNDP1	-	-	-
128	VCCP1	-	-	-	VCCP1	-	-	-
129	NC	-	-	-	PR13A	2	-	-
130	GND	-	-	-	GND	-	-	-
131	PR9B	2	C	PCLKC2_0	PR12B	2	C	PCLKC2_0
132	PR9A	2	T	PCLKT2_0	PR12A	2	T	PCLKT2_0
133	NC	-	-	-	PR11B	2	C ³	-
134	NC	-	-	-	PR11A	2	T ³	-
135	GNDIO2	2	-	-	GNDIO2	2	-	-
136	PR8B	2	C	RUM0_PLLC_IN_A	PR8B	2	C	RUM0_PLLC_IN_A
137	PR8A	2	T	RUM0_PLLT_IN_A	PR8A	2	T	RUM0_PLLT_IN_A
138	PR7B	2	C ³	-	PR7B	2	C ³	-

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA

Ball Number	LFXP6				LFXP10			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
C2	PROGRAMN	7	-	-	PROGRAMN	7	-	-
C1	CCLK	7	-	-	CCLK	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
D2	PL3A	7	T	LUM0_PLLT_FB_A	PL3A	7	T	LUM0_PLLT_FB_A
D3	PL3B	7	C	LUM0_PLLC_FB_A	PL3B	7	C	LUM0_PLLC_FB_A
D1	PL2A	7	T ³	-	PL5A	7	-	-
E2	PL5A	7	-	VREF1_7	PL6B	7	-	VREF1_7
-	GNDIO7	7	-	-	GNDIO7	7	-	-
E1	PL7A	7	T ³	DQS	PL7A	7	T ³	DQS
F1	PL7B	7	C ³	-	PL7B	7	C ³	-
E3	PL12A	7	T	-	PL8A	7	T	-
F4	PL12B	7	C	-	PL8B	7	C	-
F3	PL4A	7	T ³	-	PL9A	7	T ³	-
F2	PL4B	7	C ³	-	PL9B	7	C ³	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
G1	PL2B	7	C ³	-	PL11B	7	-	-
G3	PL8A	7	T	LUM0_PLLT_IN_A	PL12A	7	T	LUM0_PLLT_IN_A
G2	PL8B	7	C	LUM0_PLLC_IN_A	PL12B	7	C	LUM0_PLLC_IN_A
H1	PL9A	7	T ³	-	PL13A	7	T ³	-
H2	PL9B	7	C ³	-	PL13B	7	C ³	-
G4	PL6B	7	-	VREF2_7	PL14A	7	-	VREF2_7
G5	PL14A	7	-	-	PL15B	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
J1	PL11A	7	T ³	-	PL16A	7	T ³	DQS
J2	PL11B	7	C ³	-	PL16B	7	C ³	-
H3	PL13A	7	T ³	-	PL18A	7	T ³	-
J3	PL13B	7	C ³	-	PL18B	7	C ³	-
H4	VCCP0	-	-	-	VCCP0	-	-	-
H5	GNDP0	-	-	-	GNDP0	-	-	-
K1	PL17A	6	T	PCLKT6_0	PL20A	6	T	PCLKT6_0
K2	PL17B	6	C	PCLKC6_0	PL20B	6	C	PCLKC6_0
-	GNDIO6	6	-	-	GNDIO6	6	-	-
J4	PL15B	6	-	-	PL22A	6	-	-
J5	PL22A	6	-	VREF1_6	PL23B	6	-	VREF1_6
L1	PL16A	6	T ³	-	PL24A	6	T ³	DQS
L2	PL16B	6	C ³	-	PL24B	6	C ³	-
M1	PL18A	6	T ³	-	PL25A	6	T	LLM0_PLLT_IN_A
M2	PL18B	6	C ³	-	PL25B	6	C	LLM0_PLLC_IN_A
K3	PL19A	6	T ³	-	PL26A	6	T ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
L3	PL19B	6	C ³	-	PL26B	6	C ³	-
L4	PL21A	6	T ³	-	PL28A	6	-	-

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP6				LFXP10			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
R8	PB16A	5	T	-	PB20A	5	T	-
T9	PB16B	5	C	-	PB20B	5	C	-
R9	PB17A	4	T	-	PB21A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
P9	PB17B	4	C	-	PB21B	4	C	-
T10	PB18A	4	T	PCLKT4_0	PB22A	4	T	PCLKT4_0
T11	PB18B	4	C	PCLKC4_0	PB22B	4	C	PCLKC4_0
R10	PB19A	4	T	-	PB23A	4	T	-
P10	PB19B	4	C	-	PB23B	4	C	-
N9	PB20A	4	-	-	PB24A	4	-	-
M9	PB21B	4	-	-	PB25B	4	-	-
R12	PB22A	4	T	DQS	PB26A	4	T	DQS
-	GNDIO4	4	-	-	GNDIO4	4	-	-
T12	PB22B	4	C	VREF1_4	PB26B	4	C	VREF1_4
P13	PB23A	4	T	-	PB27A	4	T	-
R13	PB23B	4	C	-	PB27B	4	C	-
M11	PB24A	4	T	-	PB28A	4	T	-
N11	PB24B	4	C	-	PB28B	4	C	-
N10	PB25A	4	T	-	PB29A	4	T	-
M10	PB25B	4	C	-	PB29B	4	C	-
T13	PB26A	4	T	-	PB30A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
P14	PB26B	4	C	-	PB30B	4	C	-
R11	PB27A	4	T	VREF2_4	PB31A	4	T	VREF2_4
P12	PB27B	4	C	-	PB31B	4	C	-
T14	PB28A	4	-	-	PB32A	4	-	-
R14	PB29B	4	-	-	PB33B	4	-	-
P11	PB30A	4	T	DQS	PB34A	4	T	DQS
N12	PB30B	4	C	-	PB34B	4	C	-
T15	PB31A	4	T	-	PB35A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
R15	PB31B	4	C	-	PB35B	4	C	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
P15	PR26B	3	C ³	-	PR34B	3	C	RLM0_PLLC_FB_A
N15	PR26A	3	T ³	-	PR34A	3	T	RLM0_PLLT_FB_A
P16	PR24B	3	C ³	-	PR33B	3	C ³	-
R16	PR24A	3	T ³	DQS	PR33A	3	T ³	DQS
M15	PR15B	3	-	-	PR32B	3	-	-
N14	PR23B	3	-	VREF1_3	PR31A	3	-	VREF1_3
-	GNDIO3	3	-	-	GNDIO3	3	-	-
M14	PR25B	3	C	-	PR29B	3	C	-
L13	PR25A	3	T	-	PR29A	3	T	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
F4	PROGRAMN	7	-	-	PROGRAMN	7	-	-	PROGRAMN	7	-	-
G4	CCLK	7	-	-	CCLK	7	-	-	CCLK	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
D2	PL2A	7	T ³	-	PL6A	7	T ³	-	PL6A	7	T ³	-
D1	PL2B	7	C ³	-	PL6B	7	C ³	-	PL6B	7	C ³	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
E2	PL3A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A
E3	PL3B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A
F3	PL4A	7	T ³	-	PL8A	7	T ³	-	PL8A	7	T ³	-
F2	PL4B	7	C ³	-	PL8B	7	C ³	-	PL8B	7	C ³	-
H4	PL5A	7	-	-	PL9A	7	-	-	PL9A	7	-	-
H3	PL6B	7	-	VREF1_7	PL10B	7	-	VREF1_7	PL10B	7	-	VREF1_7
G3	PL7A	7	T ³	DQS	PL11A	7	T ³	DQS	PL11A	7	T ³	DQS
G2	PL7B	7	C ³	-	PL11B	7	C ³	-	PL11B	7	C ³	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
F1	PL8A	7	T	-	PL12A	7	T	-	PL12A	7	T	-
E1	PL8B	7	C	-	PL12B	7	C	-	PL12B	7	C	-
J4	PL9A	7	T ³	-	PL13A	7	T ³	-	PL13A	7	T ³	-
K4	PL9B	7	C ³	-	PL13B	7	C ³	-	PL13B	7	C ³	-
G1	PL11A	7	T ³	-	PL15A	7	T ³	-	PL15A	7	T ³	-
H2	PL11B	7	C ³	-	PL15B	7	C ³	-	PL15B	7	C ³	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
J2	PL12A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A
H1	PL12B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A
J1	PL13A	7	T ³	-	PL17A	7	T ³	-	PL17A	7	T ³	-
K2	PL13B	7	C ³	-	PL17B	7	C ³	-	PL17B	7	C ³	-
K3	PL14A	7	-	VREF2_7	PL18A	7	-	VREF2_7	PL18A	7	-	VREF2_7
J3	PL15B	7	-	-	PL19B	7	-	-	PL19B	7	-	-
K1	PL16A	7	T ³	DQS	PL20A	7	T ³	DQS	PL20A	7	T ³	DQS
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
L2	PL16B	7	C ³	-	PL20B	7	C ³	-	PL20B	7	C ³	-
L3	PL17A	7	T	-	PL21A	7	T	-	PL21A	7	T	-
L4	PL17B	7	C	-	PL21B	7	C	-	PL21B	7	C	-
L1	PL18A	7	T ³	-	PL22A	7	T ³	-	PL22A	7	T ³	-
M1	PL18B	7	C ³	-	PL22B	7	C ³	-	PL22B	7	C ³	-
M2	VCCP0	-	-	-	VCCP0	-	-	-	VCCP0	-	-	-
N1	GNDP0	-	-	-	GNDP0	-	-	-	GNDP0	-	-	-
M3	PL19A	6	T ³	-	PL23A	6	T ³	-	PL27A	6	T ³	-
M4	PL19B	6	C ³	-	PL23B	6	C ³	-	PL27B	6	C ³	-
P1	PL20A	6	T	PCLKT6_0	PL24A	6	T	PCLKT6_0	PL28A	6	T	PCLKT6_0
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
N2	PL20B	6	C	PCLKC6_0	PL24B	6	C	PCLKC6_0	PL28B	6	C	PCLKC6_0
R1	PL21A	6	T ³	-	PL25A	6	T ³	-	PL29A	6	T ³	-
P2	PL21B	6	C ³	-	PL25B	6	C ³	-	PL29B	6	C ³	-
N3	PL22A	6	-	-	PL26A	6	-	-	PL30A	6	-	-
N4	PL23B	6	-	VREF1_6	PL27B	6	-	VREF1_6	PL31B	6	-	VREF1_6
T1	PL24A	6	T ³	DQS	PL28A	6	T ³	DQS	PL32A	6	T ³	DQS
R2	PL24B	6	C ³	-	PL28B	6	C ³	-	PL32B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
U1	PL25A	6	T	LLM0_PLLT_IN_A	PL29A	6	T	LLM0_PLLT_IN_A	PL33A	6	T	LLM0_PLLT_IN_A
T2	PL25B	6	C	LLM0_PLLC_IN_A	PL29B	6	C	LLM0_PLLC_IN_A	PL33B	6	C	LLM0_PLLC_IN_A
V1	PL26A	6	T ³	-	PL30A	6	T ³	-	PL34A	6	T ³	-
U2	PL26B	6	C ³	-	PL30B	6	C ³	-	PL34B	6	C ³	-
W1	PL28A	6	T ³	-	PL32A	6	T ³	-	PL36A	6	T ³	-
V2	PL28B	6	C ³	-	PL32B	6	C ³	-	PL36B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	-	-	-	GNDIO6	6	-	-
P3	PL29A	6	T	-	PL33A	6	T	-	PL37A	6	T	-
P4	PL29B	6	C	-	PL33B	6	C	-	PL37B	6	C	-
Y1	PL30A	6	T ³	-	PL34A	6	T ³	-	PL38A	6	T ³	-
W2	PL30B	6	C ³	-	PL34B	6	C ³	-	PL38B	6	C ³	-
R3	PL31A	6	-	VREF2_6	PL35A	6	-	VREF2_6	PL39A	6	-	VREF2_6
R4	PL32B	6	-	-	PL36B	6	-	-	PL40B	6	-	-
T3	PL33A	6	T ³	DQS	PL37A	6	T ³	DQS	PL41A	6	T ³	DQS
T4	PL33B	6	C ³	-	PL37B	6	C ³	-	PL41B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
V4	PL34A	6	T	LLM0_PLLT_FB_A	PL38A	6	T	LLM0_PLLT_FB_A	PL42A	6	T	LLM0_PLLT_FB_A
V3	PL34B	6	C	LLM0_PLLC_FB_A	PL38B	6	C	LLM0_PLLC_FB_A	PL42B	6	C	LLM0_PLLC_FB_A
U4	PL35A	6	T ³	-	PL39A	6	T ³	-	PL43A	6	T ³	-
U3	PL35B	6	C ³	-	PL39B	6	C ³	-	PL43B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
W5	SLEEPN ¹ / TOE ²	-	-	-	SLEEPN ¹ / TOE ²	-	-	-	SLEEPN ¹ / TOE ²	-	-	-
Y2	INITN	5	-	-	INITN	5	-	-	INITN	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y3	-	-	-	-	PB3B	5	-	-	PB7B	5	-	-
W3	-	-	-	-	PB4A	5	T	-	PB8A	5	T	-
W4	-	-	-	-	PB4B	5	C	-	PB8B	5	C	-
AA2	-	-	-	-	PB5A	5	-	-	PB9A	5	-	-
AA1	-	-	-	-	PB6B	5	-	-	PB10B	5	-	-
W6	PB2A	5	-	-	PB7A	5	T	DQS	PB11A	5	T	DQS
W7	-	-	-	-	PB7B	5	C	-	PB11B	5	C	-
Y4	PB3A	5	T	-	PB8A	5	T	-	PB12A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y5	PB3B	5	C	-	PB8B	5	C	-	PB12B	5	C	-
AB2	PB4A	5	T	-	PB9A	5	T	-	PB13A	5	T	-
AA3	PB4B	5	C	-	PB9B	5	C	-	PB13B	5	C	-
AB3	PB5A	5	T	-	PB10A	5	T	-	PB14A	5	T	-
AA4	PB5B	5	C	-	PB10B	5	C	-	PB14B	5	C	-
W8	PB6A	5	T	-	PB11A	5	T	-	PB15A	5	T	-
W9	PB6B	5	C	-	PB11B	5	C	-	PB15B	5	C	-
AB4	PB7A	5	T	VREF1_5	PB12A	5	T	VREF1_5	PB16A	5	T	VREF1_5
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
AA5	PB7B	5	C	-	PB12B	5	C	-	PB16B	5	C	-
AB5	PB8A	5	-	-	PB13A	5	-	-	PB17A	5	-	-
Y6	PB9B	5	-	-	PB14B	5	-	-	PB18B	5	-	-
AA6	PB10A	5	T	DQS	PB15A	5	T	DQS	PB19A	5	T	DQS
AB6	PB10B	5	C	-	PB15B	5	C	-	PB19B	5	C	-
Y9	PB11A	5	T	-	PB16A	5	T	-	PB20A	5	T	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
M21	VCCP1	-	-	-	VCCP1	-	-	-	VCCP1	-	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
M22	PR18B	2	C ³	-	PR22B	2	C ³	-	PR22B	2	C ³	-
L22	PR18A	2	T ³	-	PR22A	2	T ³	-	PR22A	2	T ³	-
K22	PR17B	2	C	PCLKC2_0	PR21B	2	C	PCLKC2_0	PR21B	2	C	PCLKC2_0
K21	PR17A	2	T	PCLKT2_0	PR21A	2	T	PCLKT2_0	PR21A	2	T	PCLKT2_0
L19	PR16B	2	C ³	-	PR20B	2	C ³	-	PR20B	2	C ³	-
K20	PR16A	2	T ³	DQS	PR20A	2	T ³	DQS	PR20A	2	T ³	DQS
L20	PR15B	2	-	-	PR19B	2	-	-	PR19B	2	-	-
L21	PR14A	2	-	VREF1_2	PR18A	2	-	VREF1_2	PR18A	2	-	VREF1_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
J22	PR13B	2	C ³	-	PR17B	2	C ³	-	PR17B	2	C ³	-
J21	PR13A	2	T ³	-	PR17A	2	T ³	-	PR17A	2	T ³	-
H22	PR12B	2	C	RUM0_PLLC_IN_A	PR16B	2	C	RUM0_PLLC_IN_A	PR16B	2	C	RUM0_PLLC_IN_A
H21	PR12A	2	T	RUM0_PLLT_IN_A	PR16A	2	T	RUM0_PLLT_IN_A	PR16A	2	T	RUM0_PLLT_IN_A
K19	PR11B	2	C ³	-	PR15B	2	C ³	-	PR15B	2	C ³	-
J19	PR11A	2	T ³	-	PR15A	2	T ³	-	PR15A	2	T ³	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
J20	PR9B	2	C ³	-	PR13B	2	C ³	-	PR13B	2	C ³	-
H20	PR9A	2	T ³	-	PR13A	2	T ³	-	PR13A	2	T ³	-
H19	PR8B	2	C	-	PR12B	2	C	-	PR12B	2	C	-
G19	PR8A	2	T	-	PR12A	2	T	-	PR12A	2	T	-
G22	PR7B	2	C ³	-	PR11B	2	C ³	-	PR11B	2	C ³	-
G21	PR7A	2	T ³	DQS	PR11A	2	T ³	DQS	PR11A	2	T ³	DQS
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
F20	PR6B	2	-	-	PR10B	2	-	-	PR10B	2	-	-
G20	PR5A	2	-	VREF2_2	PR9A	2	-	VREF2_2	PR9A	2	-	VREF2_2
F22	PR4B	2	C ³	-	PR8B	2	C ³	-	PR8B	2	C ³	-
F21	PR4A	2	T ³	-	PR8A	2	T ³	-	PR8A	2	T ³	-
E22	PR3B	2	C	RUM0_PLLC_FB_A	PR7B	2	C	RUM0_PLLC_FB_A	PR7B	2	C	RUM0_PLLC_FB_A
E21	PR3A	2	T	RUM0_PLLT_FB_A	PR7A	2	T	RUM0_PLLT_FB_A	PR7A	2	T	RUM0_PLLT_FB_A
D22	PR2B	2	C ³	-	PR6B	2	C ³	-	PR6B	2	C ³	-
D21	PR2A	2	T ³	-	PR6A	2	T ³	-	PR6A	2	T ³	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
F19	TDO	-	-	-	TDO	-	-	-	TDO	-	-	-
E20	VCCJ	-	-	-	VCCJ	-	-	-	VCCJ	-	-	-
D20	TDI	-	-	-	TDI	-	-	-	TDI	-	-	-
D19	TMS	-	-	-	TMS	-	-	-	TMS	-	-	-
D18	TCK	-	-	-	TCK	-	-	-	TCK	-	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
E19	-	-	-	-	PT48A	1	-	-	PT52A	1	-	-
D17	-	-	-	-	PT47B	1	C	-	PT51B	1	C	-
D16	-	-	-	-	PT47A	1	T	DQS	PT51A	1	T	DQS
C16	-	-	-	-	PT46B	1	-	-	PT50B	1	-	-
C15	-	-	-	-	PT45A	1	-	-	PT49A	1	-	-
C17	-	-	-	-	PT44B	1	C	-	PT48B	1	C	-
C18	PT39A	1	-	-	PT44A	1	T	-	PT48A	1	T	-
C19	PT38B	1	C	-	PT43B	1	C	-	PT47B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
C20	PT38A	1	T	-	PT43A	1	T	-	PT47A	1	T	-
C21	PT37B	1	C	-	PT42B	1	C	-	PT46B	1	C	-
C22	PT37A	1	T	-	PT42A	1	T	-	PT46A	1	T	-
B22	PT36B	1	C	-	PT41B	1	C	-	PT45B	1	C	-
A21	PT36A	1	T	-	PT41A	1	T	-	PT45A	1	T	-
D15	PT35B	1	C	-	PT40B	1	C	-	PT44B	1	C	-
D14	PT35A	1	T	-	PT40A	1	T	-	PT44A	1	T	-
B21	PT34B	1	C	VREF1_1	PT39B	1	C	VREF1_1	PT43B	1	C	VREF1_1
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
A20	PT34A	1	T	DQS	PT39A	1	T	DQS	PT43A	1	T	DQS
B20	PT33B	1	-	-	PT38B	1	-	-	PT42B	1	-	-
A19	PT32A	1	-	-	PT37A	1	-	-	PT41A	1	-	-
B19	PT31B	1	C	-	PT36B	1	C	-	PT40B	1	C	-
A18	PT31A	1	T	-	PT36A	1	T	-	PT40A	1	T	-
C14	PT30B	1	C	-	PT35B	1	C	-	PT39B	1	C	-
C13	PT30A	1	T	D0	PT35A	1	T	D0	PT39A	1	T	D0
B18	PT29B	1	C	D1	PT34B	1	C	D1	PT38B	1	C	D1
A17	PT29A	1	T	VREF2_1	PT34A	1	T	VREF2_1	PT38A	1	T	VREF2_1
B17	PT28B	1	C	-	PT33B	1	C	-	PT37B	1	C	-
A16	PT28A	1	T	D2	PT33A	1	T	D2	PT37A	1	T	D2
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
B16	PT27B	1	C	D3	PT32B	1	C	D3	PT36B	1	C	D3
A15	PT27A	1	T	-	PT32A	1	T	-	PT36A	1	T	-
B15	PT26B	1	C	-	PT31B	1	C	-	PT35B	1	C	-
A14	PT26A	1	T	DQS	PT31A	1	T	DQS	PT35A	1	T	DQS
D13	PT25B	1	-	-	PT30B	1	-	-	PT34B	1	-	-
D12	PT24A	1	-	D4	PT29A	1	-	D4	PT33A	1	-	D4
B14	PT23B	1	C	-	PT28B	1	C	-	PT32B	1	C	-
A13	PT23A	1	T	D5	PT28A	1	T	D5	PT32A	1	T	D5
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
B13	PT22B	1	C	D6	PT27B	1	C	D6	PT31B	1	C	D6
A12	PT22A	1	T	-	PT27A	1	T	-	PT31A	1	T	-
B12	PT21B	1	C	D7	PT26B	1	C	D7	PT30B	1	C	D7
C12	PT21A	1	T	-	PT26A	1	T	-	PT30A	1	T	-
C11	PT20B	0	C	BUSY	PT25B	0	C	BUSY	PT29B	0	C	BUSY
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
B11	PT20A	0	T	CS1N	PT25A	0	T	CS1N	PT29A	0	T	CS1N
A11	PT19B	0	C	PCLKC0_0	PT24B	0	C	PCLKC0_0	PT28B	0	C	PCLKC0_0
A10	PT19A	0	T	PCLKT0_0	PT24A	0	T	PCLKT0_0	PT28A	0	T	PCLKT0_0
B10	PT18B	0	C	-	PT23B	0	C	-	PT27B	0	C	-
B9	PT18A	0	T	DQS	PT23A	0	T	DQS	PT27A	0	T	DQS
D11	PT17B	0	-	-	PT22B	0	-	-	PT26B	0	-	-
D10	PT16A	0	-	DOUT	PT21A	0	-	DOUT	PT25A	0	-	DOUT
A9	PT15B	0	C	-	PT20B	0	C	-	PT24B	0	C	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C8	PT15A	0	T	WRITEN	PT20A	0	T	WRITEN	PT24A	0	T	WRITEN
B8	PT14B	0	C	-	PT19B	0	C	-	PT23B	0	C	-
A8	PT14A	0	T	VREF1_0	PT19A	0	T	VREF1_0	PT23A	0	T	VREF1_0
C7	PT13B	0	C	-	PT18B	0	C	-	PT22B	0	C	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L1	-	-	-	-	PL23A	7	T ³	-
M1	-	-	-	-	PL23B	7	C ³	-
M2	-	-	-	-	PL24A	7	-	-
L5	VCCP0	-	-	-	VCCP0	-	-	-
N2	GNDP0	-	-	-	GNDP0	-	-	-
N1	-	-	-	-	PL25B	6	-	-
P2	-	-	-	-	PL26A	6	T ³	-
P1	-	-	-	-	PL26B	6	C ³	-
M4	PL23A	6	T ³	-	PL27A	6	T ³	-
M3	PL23B	6	C ³	-	PL27B	6	C ³	-
R2	PL24A	6	T	PCLKT6_0	PL28A	6	T	PCLKT6_0
-	GNDIO6	6	-	-	GNDIO6	6	-	-
R1	PL24B	6	C	PCLKC6_0	PL28B	6	C	PCLKC6_0
N3	PL25A	6	T ³	-	PL29A	6	T ³	-
N4	PL25B	6	C ³	-	PL29B	6	C ³	-
M5	PL26A	6	-	-	PL30A	6	-	-
N5	PL27B	6	-	VREF1_6	PL31B	6	-	VREF1_6
T2	PL28A	6	T ³	DQS	PL32A	6	T ³	DQS
T1	PL28B	6	C ³	-	PL32B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
U2	PL29A	6	T	LLM0_PLLT_IN_A	PL33A	6	T	LLM0_PLLT_IN_A
U1	PL29B	6	C	LLM0_PLLC_IN_A	PL33B	6	C	LLM0_PLLC_IN_A
P3	PL30A	6	T ³	-	PL34A	6	T ³	-
P4	PL30B	6	C ³	-	PL34B	6	C ³	-
P6	PL32A	6	T ³	-	PL36A	6	T ³	-
P5	PL32B	6	C ³	-	PL36B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
V2	PL33A	6	T	-	PL37A	6	T	-
V1	PL33B	6	C	-	PL37B	6	C	-
W2	PL34A	6	T ³	-	PL38A	6	T ³	-
W1	PL34B	6	C ³	-	PL38B	6	C ³	-
R3	PL35A	6	-	VREF2_6	PL39A	6	-	VREF2_6
R4	PL36B	6	-	-	PL40B	6	-	-
R6	PL37A	6	T ³	DQS	PL41A	6	T ³	DQS
R5	PL37B	6	C ³	-	PL41B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
Y2	PL38A	6	T	LLM0_PLLT_FB_A	PL42A	6	T	LLM0_PLLT_FB_A
Y1	PL38B	6	C	LLM0_PLLC_FB_A	PL42B	6	C	LLM0_PLLC_FB_A
T3	PL39A	6	T ³	-	PL43A	6	T ³	-
T4	PL39B	6	C ³	-	PL43B	6	C ³	-
W3	PL40A	6	T ³	-	PL44A	6	T ³	-
V3	PL40B	6	C ³	-	PL44B	6	C ³	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
J21	PR20B	2	C ³	-	PR20B	2	C ³	-
J22	PR20A	2	T ³	DQS	PR20A	2	T ³	DQS
K18	PR19B	2	-	-	PR19B	2	-	-
K19	PR18A	2	-	VREF1_2	PR18A	2	-	VREF1_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
K21	PR17B	2	C ³	-	PR17B	2	C ³	-
K20	PR17A	2	T ³	-	PR17A	2	T ³	-
H21	PR16B	2	C	RUM0_PLLC_IN_A	PR16B	2	C	RUM0_PLLC_IN_A
H22	PR16A	2	T	RUM0_PLLT_IN_A	PR16A	2	T	RUM0_PLLT_IN_A
J20	PR15B	2	C ³	-	PR15B	2	C ³	-
J19	PR15A	2	T ³	-	PR15A	2	T ³	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
J17	PR13B	2	C ³	-	PR13B	2	C ³	-
J18	PR13A	2	T ³	-	PR13A	2	T ³	-
G21	PR12B	2	C	-	PR12B	2	C	-
G22	PR12A	2	T	-	PR12A	2	T	-
F21	PR11B	2	C ³	-	PR11B	2	C ³	-
F22	PR11A	2	T ³	DQS	PR11A	2	T ³	DQS
-	GNDIO2	2	-	-	GNDIO2	2	-	-
H20	PR10B	2	-	-	PR10B	2	-	-
H19	PR9A	2	-	VREF2_2	PR9A	2	-	VREF2_2
H17	PR8B	2	C ³	-	PR8B	2	C ³	-
H18	PR8A	2	T ³	-	PR8A	2	T ³	-
E21	PR7B	2	C	RUM0_PLLC_FB_A	PR7B	2	C	RUM0_PLLC_FB_A
E22	PR7A	2	T	RUM0_PLLT_FB_A	PR7A	2	T	RUM0_PLLT_FB_A
D21	PR6B	2	C ³	-	PR6B	2	C ³	-
D22	PR6A	2	T ³	-	PR6A	2	T ³	-
G20	PR5B	2	C ³	-	PR5B	2	C ³	-
G19	PR5A	2	T ³	-	PR5A	2	T ³	-
G17	PR4B	2	C	-	PR4B	2	C	-
G18	PR4A	2	T	-	PR4A	2	T	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
F18	PR3B	2	C ³	-	PR3B	2	C ³	-
F19	PR3A	2	T ³	-	PR3A	2	T ³	-
C22	PR2B	2	-	-	PR2B	2	-	-
F20	TDO	-	-	-	TDO	-	-	-
E20	VCCJ	-	-	-	VCCJ	-	-	-
D19	TDI	-	-	-	TDI	-	-	-
E19	TMS	-	-	-	TMS	-	-	-
D20	TCK	-	-	-	TCK	-	-	-
C20	-	-	-	-	PT56A	1	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
D18	-	-	-	-	PT55B	1	C	-
E18	-	-	-	-	PT55A	1	T	-
C19	-	-	-	-	PT54B	1	C	-
C18	-	-	-	-	PT54A	1	T	-
C21	-	-	-	-	PT53B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B21	-	-	-	-	PT53A	1	T	-
E17	PT48B	1	C	-	PT52B	1	C	-
E16	PT48A	1	T	-	PT52A	1	T	-
C17	PT47B	1	C	-	PT51B	1	C	-
D17	PT47A	1	T	DQS	PT51A	1	T	DQS
F17	PT46B	1	-	-	PT50B	1	-	-
F16	PT45A	1	-	-	PT49A	1	-	-
C16	PT44B	1	C	-	PT48B	1	C	-
D16	PT44A	1	T	-	PT48A	1	T	-
A20	PT43B	1	C	-	PT47B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B20	PT43A	1	T	-	PT47A	1	T	-
A19	PT42B	1	C	-	PT46B	1	C	-
B19	PT42A	1	T	-	PT46A	1	T	-
C15	PT41B	1	C	-	PT45B	1	C	-
D15	PT41A	1	T	-	PT45A	1	T	-
A18	PT40B	1	C	-	PT44B	1	C	-
B18	PT40A	1	T	-	PT44A	1	T	-
F15	PT39B	1	C	VREF1_1	PT43B	1	C	VREF1_1
-	GNDIO1	1	-	-	GNDIO1	1	-	-
E15	PT39A	1	T	DQS	PT43A	1	T	DQS
A17	PT38B	1	-	-	PT42B	1	-	-
B17	PT37A	1	-	-	PT41A	1	-	-
E14	PT36B	1	C	-	PT40B	1	C	-
F14	PT36A	1	T	-	PT40A	1	T	-
D14	PT35B	1	C	-	PT39B	1	C	-
C14	PT35A	1	T	D0	PT39A	1	T	D0
A16	PT34B	1	C	D1	PT38B	1	C	D1
B16	PT34A	1	T	VREF2_1	PT38A	1	T	VREF2_1
A15	PT33B	1	C	-	PT37B	1	C	-
B15	PT33A	1	T	D2	PT37A	1	T	D2
-	GNDIO1	1	-	-	GNDIO1	1	-	-
E13	PT32B	1	C	D3	PT36B	1	C	D3
D13	PT32A	1	T	-	PT36A	1	T	-
C13	PT31B	1	C	-	PT35B	1	C	-
B13	PT31A	1	T	DQS	PT35A	1	T	DQS

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
G9	VCC	-	-	-	VCC	-	-	-
H15	VCC	-	-	-	VCC	-	-	-
H8	VCC	-	-	-	VCC	-	-	-
J16	VCC	-	-	-	VCC	-	-	-
J7	VCC	-	-	-	VCC	-	-	-
K16	VCC	-	-	-	VCC	-	-	-
K17	VCC	-	-	-	VCC	-	-	-
K6	VCC	-	-	-	VCC	-	-	-
K7	VCC	-	-	-	VCC	-	-	-
N16	VCC	-	-	-	VCC	-	-	-
N17	VCC	-	-	-	VCC	-	-	-
N6	VCC	-	-	-	VCC	-	-	-
N7	VCC	-	-	-	VCC	-	-	-
P16	VCC	-	-	-	VCC	-	-	-
P7	VCC	-	-	-	VCC	-	-	-
R15	VCC	-	-	-	VCC	-	-	-
R8	VCC	-	-	-	VCC	-	-	-
T10	VCC	-	-	-	VCC	-	-	-
T13	VCC	-	-	-	VCC	-	-	-
T14	VCC	-	-	-	VCC	-	-	-
T9	VCC	-	-	-	VCC	-	-	-
U10	VCC	-	-	-	VCC	-	-	-
U13	VCC	-	-	-	VCC	-	-	-
G15	VCCAUX	-	-	-	VCCAUX	-	-	-
G16	VCCAUX	-	-	-	VCCAUX	-	-	-
G7	VCCAUX	-	-	-	VCCAUX	-	-	-
G8	VCCAUX	-	-	-	VCCAUX	-	-	-
H16	VCCAUX	-	-	-	VCCAUX	-	-	-
H7	VCCAUX	-	-	-	VCCAUX	-	-	-
R16	VCCAUX	-	-	-	VCCAUX	-	-	-
R7	VCCAUX	-	-	-	VCCAUX	-	-	-
T15	VCCAUX	-	-	-	VCCAUX	-	-	-
T16	VCCAUX	-	-	-	VCCAUX	-	-	-
T7	VCCAUX	-	-	-	VCCAUX	-	-	-
T8	VCCAUX	-	-	-	VCCAUX	-	-	-
F11	VCCIO0	0	-	-	VCCIO0	0	-	-
G11	VCCIO0	0	-	-	VCCIO0	0	-	-
H10	VCCIO0	0	-	-	VCCIO0	0	-	-
H11	VCCIO0	0	-	-	VCCIO0	0	-	-
F12	VCCIO1	1	-	-	VCCIO1	1	-	-
G12	VCCIO1	1	-	-	VCCIO1	1	-	-
H12	VCCIO1	1	-	-	VCCIO1	1	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
H13	VCCIO1	1	-	-	VCCIO1	1	-	-
K15	VCCIO2	2	-	-	VCCIO2	2	-	-
L15	VCCIO2	2	-	-	VCCIO2	2	-	-
L16	VCCIO2	2	-	-	VCCIO2	2	-	-
L17	VCCIO2	2	-	-	VCCIO2	2	-	-
M15	VCCIO3	3	-	-	VCCIO3	3	-	-
M16	VCCIO3	3	-	-	VCCIO3	3	-	-
M17	VCCIO3	3	-	-	VCCIO3	3	-	-
N15	VCCIO3	3	-	-	VCCIO3	3	-	-
R12	VCCIO4	4	-	-	VCCIO4	4	-	-
R13	VCCIO4	4	-	-	VCCIO4	4	-	-
T12	VCCIO4	4	-	-	VCCIO4	4	-	-
U12	VCCIO4	4	-	-	VCCIO4	4	-	-
R10	VCCIO5	5	-	-	VCCIO5	5	-	-
R11	VCCIO5	5	-	-	VCCIO5	5	-	-
T11	VCCIO5	5	-	-	VCCIO5	5	-	-
U11	VCCIO5	5	-	-	VCCIO5	5	-	-
M6	VCCIO6	6	-	-	VCCIO6	6	-	-
M7	VCCIO6	6	-	-	VCCIO6	6	-	-
M8	VCCIO6	6	-	-	VCCIO6	6	-	-
N8	VCCIO6	6	-	-	VCCIO6	6	-	-
K8	VCCIO7	7	-	-	VCCIO7	7	-	-
L6	VCCIO7	7	-	-	VCCIO7	7	-	-
L7	VCCIO7	7	-	-	VCCIO7	7	-	-
L8	VCCIO7	7	-	-	VCCIO7	7	-	-

1. Applies to LFXP "C" only.

2. Applies to LFXP "E" only.

3. Supports dedicated LVDS outputs.

Lead-free Packaging**Commercial**

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3C-3QN208C	136	1.8/2.5/3.3V	-3	PQFP	208	COM	3.1K
LFXP3C-4QN208C	136	1.8/2.5/3.3V	-4	PQFP	208	COM	3.1K
LFXP3C-5QN208C	136	1.8/2.5/3.3V	-5	PQFP	208	COM	3.1K
LFXP3C-3TN144C	100	1.8/2.5/3.3V	-3	TQFP	144	COM	3.1K
LFXP3C-4TN144C	100	1.8/2.5/3.3V	-4	TQFP	144	COM	3.1K
LFXP3C-5TN144C	100	1.8/2.5/3.3V	-5	TQFP	144	COM	3.1K
LFXP3C-3TN100C	62	1.8/2.5/3.3V	-3	TQFP	100	COM	3.1K
LFXP3C-4TN100C	62	1.8/2.5/3.3V	-4	TQFP	100	COM	3.1K
LFXP3C-5TN100C	62	1.8/2.5/3.3V	-5	TQFP	100	COM	3.1K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6C-3FN256C	188	1.8/2.5/3.3V	-3	fpBGA	256	COM	5.8K
LFXP6C-4FN256C	188	1.8/2.5/3.3V	-4	fpBGA	256	COM	5.8K
LFXP6C-5FN256C	188	1.8/2.5/3.3V	-5	fpBGA	256	COM	5.8K
LFXP6C-3QN208C	142	1.8/2.5/3.3V	-3	PQFP	208	COM	5.8K
LFXP6C-4QN208C	142	1.8/2.5/3.3V	-4	PQFP	208	COM	5.8K
LFXP6C-5QN208C	142	1.8/2.5/3.3V	-5	PQFP	208	COM	5.8K
LFXP6C-3TN144C	100	1.8/2.5/3.3V	-3	TQFP	144	COM	5.8K
LFXP6C-4TN144C	100	1.8/2.5/3.3V	-4	TQFP	144	COM	5.8K
LFXP6C-5TN144C	100	1.8/2.5/3.3V	-5	TQFP	144	COM	5.8K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10C-3FN388C	244	1.8/2.5/3.3V	-3	fpBGA	388	COM	9.7K
LFXP10C-4FN388C	244	1.8/2.5/3.3V	-4	fpBGA	388	COM	9.7K
LFXP10C-5FN388C	244	1.8/2.5/3.3V	-5	fpBGA	388	COM	9.7K
LFXP10C-3FN256C	188	1.8/2.5/3.3V	-3	fpBGA	256	COM	9.7K
LFXP10C-4FN256C	188	1.8/2.5/3.3V	-4	fpBGA	256	COM	9.7K
LFXP10C-5FN256C	188	1.8/2.5/3.3V	-5	fpBGA	256	COM	9.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15C-3FN484C	300	1.8/2.5/3.3V	-3	fpBGA	484	COM	15.5K
LFXP15C-4FN484C	300	1.8/2.5/3.3V	-4	fpBGA	484	COM	15.5K
LFXP15C-5FN484C	300	1.8/2.5/3.3V	-5	fpBGA	484	COM	15.5K
LFXP15C-3FN388C	268	1.8/2.5/3.3V	-3	fpBGA	388	COM	15.5K
LFXP15C-4FN388C	268	1.8/2.5/3.3V	-4	fpBGA	388	COM	15.5K
LFXP15C-5FN388C	268	1.8/2.5/3.3V	-5	fpBGA	388	COM	15.5K
LFXP15C-3FN256C	188	1.8/2.5/3.3V	-3	fpBGA	256	COM	15.5K
LFXP15C-4FN256C	188	1.8/2.5/3.3V	-4	fpBGA	256	COM	15.5K
LFXP15C-5FN256C	188	1.8/2.5/3.3V	-5	fpBGA	256	COM	15.5K

Industrial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10E-3FN388I	244	1.2V	-3	fpBGA	388	IND	9.7K
LFXP10E-4FN388I	244	1.2V	-4	fpBGA	388	IND	9.7K
LFXP10E-3FN256I	188	1.2V	-3	fpBGA	256	IND	9.7K
LFXP10E-4FN256I	188	1.2V	-4	fpBGA	256	IND	9.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15E-3FN484I	300	1.2V	-3	fpBGA	484	IND	15.5K
LFXP15E-4FN484I	300	1.2V	-4	fpBGA	484	IND	15.5K
LFXP15E-3FN388I	268	1.2V	-3	fpBGA	388	IND	15.5K
LFXP15E-4FN388I	268	1.2V	-4	fpBGA	388	IND	15.5K
LFXP15E-3FN256I	188	1.2V	-3	fpBGA	256	IND	15.5K
LFXP15E-4FN256I	188	1.2V	-4	fpBGA	256	IND	15.5K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20E-3FN484I	340	1.2V	-3	fpBGA	484	IND	19.7K
LFXP20E-4FN484I	340	1.2V	-4	fpBGA	484	IND	19.7K
LFXP20E-3FN388I	268	1.2V	-3	fpBGA	388	IND	19.7K
LFXP20E-4FN388I	268	1.2V	-4	fpBGA	388	IND	19.7K
LFXP20E-3FN256I	188	1.2V	-3	fpBGA	256	IND	19.7K
LFXP20E-4FN256I	188	1.2V	-4	fpBGA	256	IND	19.7K