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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	20000
Total RAM Bits	405504
Number of I/O	268
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	388-BBGA
Supplier Device Package	388-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp20e-4f388c

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## Lattice Semiconductor

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-4 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices, one Slice functions as the read-write port. The other companion Slice supports the read-only port. For more information on RAM mode in LatticeXP devices, please see details of additional technical documentation at the end of this data sheet.

### Table 2-3. Number of Slices Required for Implementing Distributed RAM

	SPR16x2	DPR16x2				
Number of Slices	1	2				
Note: SPR = Single Port RAM, DPR = Dual Port RAM						

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	~ /	<b></b>	 	Duline	



**ROM Mode:** The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

#### **PFU Modes of Operation**

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

### Lattice Semiconductor

### Figure 2-6. Secondary Clock Sources



## **Clock Routing**

The clock routing structure in LatticeXP devices consists of four Primary Clock lines and a Secondary Clock network per quadrant. The primary clocks are generated from MUXs located in each quadrant. Figure 2-7 shows this clock routing. The four secondary clocks are generated from MUXs located in each quadrant as shown in Figure 2-8. Each slice derives its clock from the primary clock lines, secondary clock lines and routing as shown in Figure 2-9.





## Lattice Semiconductor

### Figure 2-8. Per Quadrant Secondary Clock Selection



### Figure 2-9. Slice Clock Selection



## sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signals to the feedback divider: from CLKOP (PLL internal), from clock net (CLKOP or CLKOS) or from a user clock (PIN or logic). There is a PLL\_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the t<sub>LOCK</sub> parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

### Figure 2-17. PIC Diagram



In the LatticeXP family, seven PIOs or four (3.5) PICs are grouped together to provide two LVDS differential pairs, one PIC pair and one single I/O, as shown in Figure 2-18.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as "T" and "C"). The PAD Labels "T" and "C" distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 14 PIOs (a group of 8 PICs) contains a delay element to facilitate the generation of DQS signals as shown in Figure 2-19. The DQS signal feeds the DQS bus which spans the set of 13 PIOs (8 PICs). The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table in this data sheet.

Figure 2-25. Tristate Register Block



\*Latch is transparent when input is low.

### Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing and a DQS signal provided from the programmable DQS pin. The clock can optionally be inverted.

The clock enable and local reset signals are selected from the routing and optionally inverted. The global tristate signal is passed through this block.

## DDR Memory Support

Implementing high performance DDR memory interfaces requires dedicated DDR register structures in the input (for read operations) and in the output (for write operations). As indicated in the PIO Logic section, the LatticeXP devices provide this capability. In addition to these registers, the LatticeXP devices contain two elements to simplify the design of input structures for read operations: the DQS delay block and polarity control logic.

## DLL Calibrated DQS Delay Block

Source Synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment, however in DDR memories the clock (referred to as DQS) is not free running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds the polarity control logic which controls the polarity of the clock to the sync registers in the input register blocks. Figures 2-26 and 2-27 show how the polarity control logic are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two DLLs on opposite sides of the device. Each DLL compensates DQS Delays in its half of the device as shown in Figure 2-27. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

### Figure 2-26. DQS Local Bus



Figure 2-27. DLL Calibration Bus and DQS/DQS Transition Distribution



Table 2-8. Supported	<b>Output Standards</b>
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Output Standard	Drive	V <sub>CCIO</sub> (Nom.)
Single-ended Interfaces	•	
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVCMOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVCMOS25	4mA, 8mA, 12mA 16mA, 20mA	2.5
LVCMOS18	4mA, 8mA, 12mA 16mA	1.8
LVCMOS15	4mA, 8mA	1.5
LVCMOS12	2mA, 6mA	1.2
LVCMOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVCMOS15, Open Drain	4mA, 8mA	—
LVCMOS12, Open Drain	2mA. 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II, III	N/A	1.8
HSTL15 Class I, III	N/A	1.5
SSTL3 Class I, II	N/A	3.3
SSTL2 Class I, II	N/A	2.5
SSTL18 Class I	N/A	1.8
Differential Interfaces	•	
Differential SSTL3, Class I, II	N/A	3.3
Differential SSTL2, Class I, II	N/A	2.5
Differential SSTL18, Class I	N/A	1.8
Differential HSTL18, Class I, II, III	N/A	1.8
Differential HSTL15, Class I, III	N/A	1.5
LVDS	N/A	2.5
BLVDS <sup>1</sup>	N/A	2.5
LVPECL <sup>1</sup>	N/A	3.3

1. Emulated with external resistors.

## Hot Socketing

The LatticeXP devices have been carefully designed to ensure predictable behavior during power-up and powerdown. Power supplies can be sequenced in any order. During power up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits, which allows easy integration with the rest of the system. These capabilities make the LatticeXP ideal for many multiple power supply and hot-swap applications.

## Sleep Mode

The LatticeXP "C" devices ( $V_{CC} = 1.8/2.5/3.3V$ ) have a sleep mode that allows standby current to be reduced by up to three orders of magnitude during periods of system inactivity. Entry and exit to Sleep Mode is controlled by the SLEEPN pin.

During Sleep Mode, the FPGA logic is non-operational, registers and EBR contents are not maintained and I/Os are tri-stated. Do not enter Sleep Mode during device programming or configuration operation. In Sleep Mode, power supplies can be maintained in their normal operating range, eliminating the need for external switching of power supplies. Table 2-9 compares the characteristics of Normal, Off and Sleep Modes.

# Hot Socketing Specifications<sup>1, 2, 3, 4, 5, 6</sup>

Symbol	Parameter	Condition	Min.	Тур.	Max.	Units
I <sub>DK</sub>	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX.)	-		+/-1000	μΑ

1. Insensitive to sequence of  $V_{CC}$ ,  $V_{CCAUX}$  and  $V_{CCIO}$ . However, assumes monotonic rise/fall rates for  $V_{CC}$ ,  $V_{CCAUX}$  and  $V_{CCIO}$ . 2.  $0 \le V_{CC} \le V_{CC}$  (MAX) or  $0 \le V_{CCAUX} \le V_{CCAUX}$  (MAX). 3.  $0 \le V_{CCIO} \le V_{CCIO}$  (MAX) for top and bottom I/O banks. 4.  $0.2 \le V_{CCIO} \le V_{CCIO}$  (MAX) for left and right I/O banks. 5.  $I_{DK}$  is additive to  $I_{PU}$ ,  $I_{PW}$  or  $I_{BH}$ . 6. LVCMOS and LVTTL only.

## Figure 3-4. RSDS (Reduced Swing Differential Standard)



### Table 3-4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z <sub>OUT</sub>	Output impedance	20	ohms
R <sub>S</sub>	Driver series resistor	300	ohms
R <sub>P</sub>	Driver parallel resistor	121	ohms
R <sub>T</sub>	Receiver termination	100	ohms
V <sub>OH</sub>	Output high voltage	1.35	V
V <sub>OL</sub>	Output low voltage	1.15	V
V <sub>OD</sub>	Output differential voltage	0.20	V
V <sub>CM</sub>	Output common mode voltage	1.25	V
Z <sub>BACK</sub>	Back impedance	101.5	ohms
I <sub>DC</sub>	DC output current	3.66	mA

# LatticeXP Internal Timing Parameters<sup>1</sup> (Continued)

**Over Recommended Operating Conditions** 

		-5		-4		-3		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
t <sub>RSTO_EBR</sub>	Reset To Output Delay Time from EBR Output Register	_	1.61	_	1.94	_	2.32	ns
PLL Parameters								
t <sub>RSTREC</sub>	Reset Recovery to Rising Clock	1.00	_	1.00	-	1.00	—	ns
t <sub>RSTSU</sub>	Reset Signal Setup Time	1.00	-	1.00	_	1.00	—	ns

1. Internal parameters are characterized but not tested on every device. Timing v.F0.11

## LatticeXP sysCONFIG Port Timing Specifications

Over	Recommended	Operating	Conditions
••••		• por a mig	•••••••

Parameter	Description	Min.	Max.	Units
sysCONFIG By	te Data Flow	I	1	
t <sub>SUCBDI</sub>	Byte D[0:7] Setup Time to CCLK	7	_	ns
t <sub>HCBDI</sub>	Byte D[0:7] Hold Time to CCLK	3	—	ns
t <sub>CODO</sub>	Clock to Dout in Flowthrough Mode	—	12	ns
t <sub>SUCS</sub>	CS[0:1] Setup Time to CCLK	7	—	ns
t <sub>HCS</sub>	CS[0:1] Hold Time to CCLK	2	—	ns
t <sub>SUWD</sub>	Write Signal Setup Time to CCLK	7	—	ns
t <sub>HWD</sub>	Write Signal Hold Time to CCLK	2	—	ns
t <sub>DCB</sub>	CCLK to BUSY Delay Time	—	12	ns
t <sub>CORD</sub>	Clock to Out for Read Data	_	12	ns
sysCONFIG By	te Slave Clocking	•		•
t <sub>BSCH</sub>	Byte Slave Clock Minimum High Pulse	6	—	ns
t <sub>BSCL</sub>	Byte Slave Clock Minimum Low Pulse	8	—	ns
t <sub>BSCYC</sub>	Byte Slave Clock Cycle Time	15	—	ns
sysCONFIG Se	rial (Bit) Data Flow			
t <sub>SUSCDI</sub>	DI (Data In) Setup Time to CCLK	7	—	ns
t <sub>HSCDI</sub>	DI (Data In) Hold Time to CCLK	2	—	ns
t <sub>CODO</sub>	Clock to Dout in Flowthrough Mode	_	12	ns
sysCONFIG Se	rial Slave Clocking			
t <sub>SSCH</sub>	Serial Slave Clock Minimum High Pulse	6	—	ns
t <sub>SSCL</sub>	Serial Slave Clock Minimum Low Pulse	6	—	ns
sysCONFIG PC	DR, Initialization and Wake Up			
t <sub>ICFG</sub>	Minimum Vcc to INIT High	—	50	ms
t <sub>VMC</sub>	Time from t <sub>ICFG</sub> to Valid Master Clock	—	2	us
t <sub>PRGMRJ</sub>	Program Pin Pulse Rejection	—	7	ns
t <sub>PRGM</sub> <sup>2</sup>	PROGRAMN Low Time to Start Configuration	25	—	ns
t <sub>DINIT</sub>	INIT Low Time	—	1	ms
t <sub>DPPINIT</sub>	Delay Time from PROGRAMN Low to INIT Low	—	37	ns
t <sub>DINITD</sub>	Delay Time from PROGRAMN Low to DONE Low	_	37	ns
t <sub>IODISS</sub>	User I/O Disable from PROGRAMN Low	_	25	ns
t <sub>IOENSS</sub>	User I/O Enabled Time from CCLK Edge During Wake-up Sequence	—	25	ns
t <sub>MWC</sub>	Additional Wake Master Clock Signals after Done Pin High	120	—	cycles
Configuration I	Master Clock (CCLK)			
Frequency <sup>1</sup>		Selected Value - 30%	Selected Value + 30%	MHz
Duty Cycle		40	60	%

1. See Table 2-10 for available CCLK frequencies.

2. The threshold level for PROGRAMN, as well as for CFG[1] and CFG[0], is determined by  $V_{CC}$ , such that the threshold =  $V_{CC}/2$ . Timing v.F0.11

## **Switching Test Conditions**

Figure 3-13 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Figure 3-5.

### Figure 3-13. Output Test Load, LVTTL and LVCMOS Standards



Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R <sub>1</sub>	CL	Timing Ref.	VT
			LVCMOS 3.3 = 1.5V	—
	8	0pF	LVCMOS 2.5 = $V_{CCIO}/2$	—
LVTTL and other LVCMOS settings (L -> H, H -> L)			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = V <sub>CCIO</sub> /2	—
LVCMOS 2.5 I/O (Z -> H)			V <sub>CCIO</sub> /2	V <sub>OL</sub>
LVCMOS 2.5 I/O (Z -> L)	188	0nE	V <sub>CCIO</sub> /2	V <sub>OH</sub>
LVCMOS 2.5 I/O (H -> Z)	100	орі	V <sub>OH</sub> - 0.15	V <sub>OL</sub>
LVCMOS 2.5 I/O (L -> Z)			V <sub>OL</sub> + 0.15	V <sub>OH</sub>

Note: Output test conditions for all other interfaces are determined by the respective standards.

# LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

			LFXP6		LFXP10			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L15	PR21B	3	C <sup>3</sup>	-	PR28B	3	C <sup>3</sup>	-
L14	PR21A	3	T <sup>3</sup>	-	PR28A	3	T <sup>3</sup>	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
L12	PR17B	3	С	-	PR26A	3	-	-
M16	PR20B	3	С	-	PR25B	3	С	RLM0_PLLC_IN_A
N16	PR20A	3	Т	-	PR25A	3	Т	RLM0_PLLT_IN_A
K14	PR19B	3	C <sup>3</sup>	-	PR24B	3	C <sup>3</sup>	-
K15	PR19A	3	T <sup>3</sup>	-	PR24A	3	T <sup>3</sup>	DQS
K12	PR17A	3	Т	-	PR23B	3	-	-
K13	PR22A	3	-	VREF2_3	PR22A	3	-	VREF2_3
-	GNDIO3	3	-	-	GNDIO3	3	-	-
L16	PR18B	3	C <sup>3</sup>	-	PR21B	3	C <sup>3</sup>	-
K16	PR18A	3	T <sup>3</sup>	-	PR21A	3	T <sup>3</sup>	-
J15	PR16B	3	C <sup>3</sup>	-	PR19B	3	C <sup>3</sup>	-
J14	PR16A	3	T <sup>3</sup>	-	PR19A	3	T <sup>3</sup>	-
J13	GNDP1	-	-	-	GNDP1	-	-	-
J12	VCCP1	-	-	-	VCCP1	-	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
J16	PR12B	2	С	PCLKC2_0	PR17B	2	С	PCLKC2_0
H16	PR12A	2	Т	PCLKT2_0	PR17A	2	Т	PCLKT2_0
H13	PR13B	2	C <sup>3</sup>	-	PR16B	2	C <sup>3</sup>	-
H12	PR13A	2	T <sup>3</sup>	-	PR16A	2	T <sup>3</sup>	DQS
H15	PR2B	2	C <sup>3</sup>	-	PR15B	2	-	-
H14	PR6B	2	-	VREF1_2	PR14A	2	-	VREF1_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G15	PR11B	2	C <sup>3</sup>	-	PR13B	2	C <sup>3</sup>	-
G14	PR11A	2	T <sup>3</sup>	-	PR13A	2	T <sup>3</sup>	-
G16	PR8B	2	С	RUM0_PLLC_IN_A	PR12B	2	С	RUM0_PLLC_IN_A
F16	PR8A	2	Т	RUM0_PLLT_IN_A	PR12A	2	Т	RUM0_PLLT_IN_A
G13	PR2A	2	T <sup>3</sup>	-	PR11B	2	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G12	PR9B	2	C <sup>3</sup>	-	PR8B	2	С	-
F13	PR9A	2	T <sup>3</sup>	-	PR8A	2	Т	-
B16	PR7B	2	C <sup>3</sup>	-	PR7B	2	C <sup>3</sup>	-
C16	PR7A	2	T <sup>3</sup>	DQS	PR7A	2	T <sup>3</sup>	DQS
F15	PR14A	2	-	-	PR6B	2	-	-
E15	PR5A	2	-	VREF2_2	PR5A	2	-	VREF2_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
F14	PR4B	2	C <sup>3</sup>	-	PR4B	2	C <sup>3</sup>	-
E14	PR4A	2	T <sup>3</sup>	-	PR4A	2	T <sup>3</sup>	-
D15	PR3B	2	С	RUM0_PLLC_FB_A	PR3B	2	С	RUM0_PLLC_FB_A
C15	PR3A	2	Т	RUM0_PLLT_FB_A	PR3A	2	Т	RUM0_PLLT_FB_A

# LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

			LFXP6				LFXP10	
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
E16	TDO	-	-	-	TDO	-	-	-
D16	VCCJ	-	-	-	VCCJ	-	-	-
D14	TDI	-	-	-	TDI	-	-	-
C14	TMS	-	-	-	TMS	-	-	-
B14	ТСК	-	-	-	ТСК	-	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
A15	PT31B	1	C	-	PT35B	1	C	-
B15	PT31A	1	Т	-	PT35A	1	Т	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
D12	PT28A	1	-	VREF1_1	PT34B	1	C	VREF1_1
C11	PT30A	1	Т	DQS	PT34A	1	Т	DQS
A14	PT29B	1	-	-	PT33B	1	-	-
B13	PT30B	1	С	-	PT32A	1	-	-
F12	PT27B	1	С	-	PT31B	1	C	-
E11	PT27A	1	Т	-	PT31A	1	Т	-
A13	PT26B	1	С	-	PT30B	1	C	-
C13	PT26A	1	Т	D0	PT30A	1	Т	D0
-	GNDIO1	1	-	-	GNDIO1	1	-	-
C10	PT25B	1	С	D1	PT29B	1	C	D1
E10	PT25A	1	Т	VREF2_1	PT29A	1	Т	VREF2_1
A12	PT24B	1	С	-	PT28B	1	C	-
B12	PT24A	1	Т	D2	PT28A	1	Т	D2
C12	PT23B	1	С	D3	PT27B	1	С	D3
A11	PT23A	1	Т	-	PT27A	1	Т	-
B11	PT22B	1	С	-	PT26B	1	C	-
D11	PT22A	1	Т	DQS	PT26A	1	Т	DQS
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B9	PT21B	1	-	-	PT25B	1	-	-
D9	PT20A	1	-	D4	PT24A	1	-	D4
A10	PT19B	1	C	-	PT23B	1	С	-
B10	PT19A	1	Т	D5	PT23A	1	Т	D5
D10	PT18B	1	С	D6	PT22B	1	С	D6
A9	PT18A	1	Т	-	PT22A	1	Т	-
C9	PT17B	1	C	D7	PT21B	1	С	D7
C8	PT17A	1	Т	-	PT21A	1	Т	-
E9	PT16B	0	С	BUSY	PT20B	0	С	BUSY
-	GNDIO0	0	-	-	GNDIO0	0	-	-
B8	PT16A	0	Т	CS1N	PT20A	0	Т	CS1N
A8	PT15B	0	C	PCLKC0_0	PT19B	0	C	PCLKC0_0
A7	PT15A	0	Т	PCLKT0_0	PT19A	0	Т	PCLKT0_0
B7	PT14B	0	С	-	PT18B	0	С	-
C7	PT14A	0	Т	DQS	PT18A	0	Т	DQS

# LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

		L	LFXP10	)		L	FXP1	5		L	FXP20	)
Ball Number	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
AA20	PB36B	4	С	-	PB41B	4	С	-	PB45B	4	С	-
AB21	PB37A	4	Т	-	PB42A	4	Т	-	PB46A	4	Т	-
AA21	PB37B	4	С	-	PB42B	4	С	-	PB46B	4	С	-
AA22	PB38A	4	Т	-	PB43A	4	Т	-	PB47A	4	Т	-
Y21	PB38B	4	С	-	PB43B	4	С	-	PB47B	4	С	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
W16	PB39A	4	-	-	PB44A	4	Т	-	PB48A	4	Т	-
W17	-	-	-	-	PB44B	4	С	-	PB48B	4	С	-
Y15	-	-	-	-	PB45A	4	-	-	PB49A	4	-	-
Y16	-	-	-	-	PB46B	4	-	-	PB50B	4	-	-
W19	-	-	-	-	PB47A	4	Т	DQS	PB51A	4	Т	DQS
W18	-	-	-	-	PB47B	4	С	-	PB51B	4	С	-
W20	-	-	-	-	PB48A	4	-	-	PB52A	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
T20	PR35B	3	C <sup>3</sup>	-	PR39B	3	C <sup>3</sup>	-	PR43B	3	C <sup>3</sup>	-
T19	PR35A	3	T <sup>3</sup>	-	PR39A	3	T <sup>3</sup>	-	PR43A	3	T <sup>3</sup>	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
U19	PR34B	3	С	RLM0_PLLC_FB_A	PR38B	3	С	RLM0_PLLC_FB_A	PR42B	3	С	RLM0_PLLC_FB_A
U20	PR34A	3	Т	RLM0_PLLT_FB_A	PR38A	3	Т	RLM0_PLLT_FB_A	PR42A	3	Т	RLM0_PLLT_FB_A
V19	PR33B	3	C <sup>3</sup>	-	PR37B	3	C <sup>3</sup>	-	PR41B	3	C <sup>3</sup>	-
V20	PR33A	3	T <sup>3</sup>	DQS	PR37A	3	T <sup>3</sup>	DQS	PR41A	3	T <sup>3</sup>	DQS
R19	PR32B	3	-	-	PR36B	3	-	-	PR40B	3	-	-
R20	PR31A	3	-	VREF1_3	PR35A	3	-	VREF1_3	PR39A	3	-	VREF1_3
W21	PR30B	3	C <sup>3</sup>	-	PR34B	3	C <sup>3</sup>	-	PR38B	3	C <sup>3</sup>	-
Y22	PR30A	3	T <sup>3</sup>	-	PR34A	3	T <sup>3</sup>	-	PR38A	3	Т³	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
P19	PR29B	3	С	-	PR33B	3	С	-	PR37B	3	С	-
P20	PR29A	3	Т	-	PR33A	3	Т	-	PR37A	3	Т	-
V21	PR28B	3	C <sup>3</sup>	-	PR32B	3	C <sup>3</sup>	-	PR36B	3	C <sup>3</sup>	-
W22	PR28A	3	T <sup>3</sup>	-	PR32A	3	T <sup>3</sup>	-	PR36A	3	Т³	-
U21	PR26B	3	C <sup>3</sup>	-	PR30B	3	C <sup>3</sup>	-	PR34B	3	C <sup>3</sup>	-
V22	PR26A	3	T <sup>3</sup>	-	PR30A	3	T <sup>3</sup>	-	PR34A	3	T <sup>3</sup>	-
T21	PR25B	3	С	RLM0_PLLC_IN_A	PR29B	3	С	RLM0_PLLC_IN_A	PR33B	3	С	RLM0_PLLC_IN_A
U22	PR25A	3	т	RLM0_PLLT_IN_A	PR29A	3	Т	RLM0_PLLT_IN_A	PR33A	3	Т	RLM0_PLLT_IN_A
-	GNDIO3	3	-		GNDIO3	3	-		GNDIO3	3	-	
R21	PR24B	3	C <sup>3</sup>	-	PR28B	3	C <sup>3</sup>	-	PR32B	3	C <sup>3</sup>	-
T22	PR24A	3	T <sup>3</sup>	DQS	PR28A	3	T <sup>3</sup>	DQS	PR32A	3	T <sup>3</sup>	DQS
N19	PR23B	3	-	-	PR27B	3	-	-	PR31B	3	-	-
N20	PR22A	3	-	VREF2 3	PR26A	3	-	VREF2 3	PR30A	3	-	VREF2 3
R22	PR21B	3	C <sup>3</sup>	-	PR25B	3	C <sup>3</sup>	-	PR29B	3	C <sup>3</sup>	-
P22	PR21A	3	T <sup>3</sup>	-	PR25A	3	T <sup>3</sup>	-	PR29A	3	T <sup>3</sup>	-
P21	PR20B	3	С	_	PR24B	3	С	-	PR28B	3	С	-
N21	PR20A	3	T	-	PR24A	3	T	-	PR28A	3	T	-
	GNDIO3	3	<u>-</u>	_	GNDIO3	3	-	_	GNDIO3	3	-	-
M20	PR19B	3	C3	_	PB23B	3	C <sup>3</sup>	-	PR27B	3	C <sup>3</sup>	-
M19	PR19A	3	т <sup>3</sup>	_	PR23A	3	T <sup>3</sup>	_	PR27A	3	T <sup>3</sup>	-
N22	GNDP1	-	<u>-</u>	_	GNDP1	-	-	_	GNDP1	-	-	-
1122	GINDET	<u> </u>	l -			1	-		GNDET	-	-	-

# LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

		L	LFXP10	)		L	FXP15	5		LFXP20		
Ball Number	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
A7	PT13A	0	Т	DI	PT18A	0	Т	DI	PT22A	0	Т	DI
B7	PT12B	0	С	-	PT17B	0	С	-	PT21B	0	С	-
C6	PT12A	0	Т	CSN	PT17A	0	Т	CSN	PT21A	0	Т	CSN
C10	PT11B	0	С	-	PT16B	0	С	-	PT20B	0	С	-
C9	PT11A	0	Т	-	PT16A	0	Т	-	PT20A	0	Т	-
A6	PT10B	0	С	VREF2_0	PT15B	0	С	VREF2_0	PT19B	0	С	VREF2_0
B6	PT10A	0	Т	DQS	PT15A	0	Т	DQS	PT19A	0	Т	DQS
A5	PT9B	0	-	-	PT14B	0	-	-	PT18B	0	-	-
B5	PT8A	0	-	-	PT13A	0	-	-	PT17A	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C5	PT7B	0	С	-	PT12B	0	С	-	PT16B	0	С	-
A4	PT7A	0	Т	-	PT12A	0	Т	-	PT16A	0	Т	-
D9	PT6B	0	С	-	PT11B	0	С	-	PT15B	0	С	-
D8	PT6A	0	Т	-	PT11A	0	Т	-	PT15A	0	Т	-
B4	PT5B	0	С	-	PT10B	0	С	-	PT14B	0	С	-
A2	PT5A	0	Т	-	PT10A	0	Т	-	PT14A	0	Т	-
A3	PT4B	0	С	-	PT9B	0	С	-	PT13B	0	С	-
B3	PT4A	0	Т	-	PT9A	0	Т	-	PT13A	0	Т	-
C4	PT3B	0	С	-	PT8B	0	С	-	PT12B	0	С	-
C3	PT3A	0	Т	-	PT8A	0	Т	-	PT12A	0	Т	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C2	-	-	-	-	PT7B	0	С	-	PT11B	0	С	-
D3	PT2A	0	-	-	PT7A	0	Т	DQS	PT11A	0	Т	DQS
D7	-	-	-	-	PT6B	0	-	-	PT10B	0	-	-
D6	-	-	-	-	PT5A	0	-	-	PT9A	0	-	-
E4	-	-	-	-	PT4B	0	С	-	PT8B	0	С	-
D4	-	-	-	-	PT4A	0	Т	-	PT8A	0	Т	-
D5	-	-	-	-	PT3B	0	-	-	PT7B	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C1	CFG0	0	-	-	CFG0	0	-	-	CFG0	0	-	-
B2	CFG1	0	-	-	CFG1	0	-	-	CFG1	0	-	-
B1	DONE	0	-	-	DONE	0	-	-	DONE	0	-	-
A1	GND	-	-	-	GND	-	-	-	GND	-	-	-
A22	GND	-	-	-	GND	-	-	-	GND	-	-	-
AB1	GND	-	-	-	GND	-	-	-	GND	-	-	-
AB22	GND	-	-	-	GND	-	-	-	GND	-	-	-
H10	GND	-	-	-	GND	-	-	-	GND	-	-	-
H11	GND	-	-	-	GND	-	-	-	GND	-	-	-
H12	GND	-	-	-	GND	-	-	-	GND	-	-	-
H13	GND	-	-	-	GND	-	-	-	GND	-	-	-
H14	GND	-	-	-	GND	-	-	-	GND	-	-	-
J10	GND	-	-	-	GND	-	-	-	GND	-	-	-
J11	GND	- 1	-	-	GND	-	-	-	GND	-	-	-
J12	GND	-	-	-	GND	-	-	-	GND	-	-	-
J13	GND	-	-	-	GND	-	-	-	GND	-	-	-
J14	GND	-	-	-	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-	GND	-	-	-
K10	GND	-	-	-	GND	-	-	-	GND	-	-	-
L		1	I	1			L			1	L	1

# LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA

			LFXP15				LFXP20	
Ball	Ball			Dual	Ball			Dual
Number	Function	Bank	Differential	Function	Function	Bank	Differential	Function
F5	PROGRAMN	7	-	-	PROGRAMN	7	-	-
E3	CCLK	7	-	-	CCLK	7	-	-
C1	PL2B	7	-	-	PL2B	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
G5	PL3A	7	T³	-	PL3A	7	T <sup>3</sup>	-
G6	PL3B	7	C <sup>3</sup>	-	PL3B	7	C <sup>3</sup>	-
F4	PL4A	7	Т	-	PL4A	7	Т	-
F3	PL4B	7	С	-	PL4B	7	С	-
G4	PL5A	7	T <sup>3</sup>	-	PL5A	7	T <sup>3</sup>	-
G3	PL5B	7	C <sup>3</sup>	-	PL5B	7	C <sup>3</sup>	-
D1	PL6A	7	T <sup>3</sup>	-	PL6A	7	T <sup>3</sup>	-
D2	PL6B	7	C <sup>3</sup>	-	PL6B	7	C <sup>3</sup>	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
E1	PL7A	7	Т	LUM0_PLLT_FB_A	PL7A	7	Т	LUM0_PLLT_FB_A
E2	PL7B	7	С	LUM0_PLLC_FB_A	PL7B	7	С	LUM0_PLLC_FB_A
H5	PL8A	7	T <sup>3</sup>	-	PL8A	7	T <sup>3</sup>	-
H6	PL8B	7	C <sup>3</sup>	-	PL8B	7	C <sup>3</sup>	-
H4	PL9A	7	-	-	PL9A	7	-	-
H3	PL10B	7	-	VREF1_7	PL10B	7	-	VREF1_7
F1	PL11A	7	T <sup>3</sup>	DQS	PL11A	7	T <sup>3</sup>	DQS
F2	PL11B	7	C <sup>3</sup>	-	PL11B	7	C <sup>3</sup>	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
J5	PL12A	7	Т	-	PL12A	7	Т	-
J6	PL12B	7	С	-	PL12B	7	С	-
G1	PL13A	7	T <sup>3</sup>	-	PL13A	7	T <sup>3</sup>	-
G2	PL13B	7	C <sup>3</sup>	-	PL13B	7	C <sup>3</sup>	-
J4	PL15A	7	T <sup>3</sup>	-	PL15A	7	T <sup>3</sup>	-
J3	PL15B	7	C <sup>3</sup>	-	PL15B	7	C <sup>3</sup>	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
H1	PL16A	7	Т	LUMO PLLT IN A	PL16A	7	Т	LUMO PLLT IN A
H2	PL16B	7	С	LUMO PLLC IN A	PL16B	7	С	LUMO PLLC IN A
	PL17A	7	T <sup>3</sup>	-	PL17A	7	T <sup>3</sup>	•
J2	PL17B	7	C <sup>3</sup>	-	PL17B	7	C <sup>3</sup>	-
K3	PL18A	7	-	VREF2_7	PL18A	7	-	VREF2_7
K2	PL19B	7	-	-	PL19B	7	-	-
K4	PL20A	7	T <sup>3</sup>	DOS	PI 20A	7	T <sup>3</sup>	DOS
-	GNDIO7	7	-		GNDIO7	7	-	
K5	PI 20B	7	C <sup>3</sup>	-	PI 20B	7	C <sup>3</sup>	
K1	PI 21A	7	т	-	PI 21A	7	т	-
12	PI 21R	7	, C		PI 21R	7	C.	_
	PI 224	7	т <sup>3</sup>		PI 224	7	т <sup>3</sup>	-
12		7		-		7		-
LO	FL22D	1	0	-	FL22D	1	0	-

# LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

			LFXP15				LFXP20	
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
G9	VCC	-	-	-	VCC	-	-	-
H15	VCC	-	-	-	VCC	-	-	-
H8	VCC	-	-	-	VCC	-	-	-
J16	VCC	-	-	-	VCC	-	-	-
J7	VCC	-	-	-	VCC	-	-	-
K16	VCC	-	-	-	VCC	-	-	-
K17	VCC	-	-	-	VCC	-	-	-
K6	VCC	-	-	-	VCC	-	-	-
K7	VCC	-	-	-	VCC	-	-	-
N16	VCC	-	-	-	VCC	-	-	-
N17	VCC	-	-	-	VCC	-	-	-
N6	VCC	-	-	-	VCC	-	-	-
N7	VCC	-	-	-	VCC	-	-	-
P16	VCC	-	-	-	VCC	-	-	-
P7	VCC	-	-	-	VCC	-	-	-
R15	VCC	-	-	-	VCC	-	-	-
R8	VCC	-	-	-	VCC	-	-	-
T10	VCC	-	-	-	VCC	-	-	-
T13	VCC	-	-	-	VCC	-	-	-
T14	VCC	-	-	-	VCC	-	-	-
Т9	VCC	-	-	-	VCC	-	-	-
U10	VCC	-	-	-	VCC	-	-	-
U13	VCC	-	-	-	VCC	-	-	-
G15	VCCAUX	-	-	-	VCCAUX	-	-	-
G16	VCCAUX	-	-	-	VCCAUX	-	-	-
G7	VCCAUX	-	-	-	VCCAUX	-	-	-
G8	VCCAUX	-	-	-	VCCAUX	-	-	-
H16	VCCAUX	-	-	-	VCCAUX	-	-	-
H7	VCCAUX	-	-	-	VCCAUX	-	-	-
R16	VCCAUX	-	-	-	VCCAUX	-	-	-
R7	VCCAUX	-	-	-	VCCAUX	-	-	-
T15	VCCAUX	-	-	-	VCCAUX	-	-	-
T16	VCCAUX	-	-	-	VCCAUX	-	-	-
T7	VCCAUX	-	-	-	VCCAUX	-	-	-
T8	VCCAUX	-	-	-	VCCAUX	-	-	-
F11	VCCIO0	0	-	-	VCCIO0	0	-	-
G11	VCCIO0	0	-	-	VCCIO0	0	-	-
H10	VCCIO0	0	-	-	VCCIO0	0	-	-
H11	VCCIO0	0	-	-	VCCIO0	0	-	-
F12	VCCIO1	1	-	-	VCCIO1	1	-	-
G12	VCCIO1	1	-	-	VCCIO1	1	-	-
H12	VCCIO1	1	-	-	VCCIO1	1	-	-

			•	,			
Part Number	l/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6E-3F256C	188	1.2V	-3	fpBGA	256	COM	5.8K
LFXP6E-4F256C	188	1.2V	-4	fpBGA	256	COM	5.8K
LFXP6E-5F256C	188	1.2V	-5	fpBGA	256	COM	5.8K
LFXP6E-3Q208C	142	1.2V	-3	PQFP	208	COM	5.8K
LFXP6E-4Q208C	142	1.2V	-4	PQFP	208	COM	5.8K
LFXP6E-5Q208C	142	1.2V	-5	PQFP	208	COM	5.8K
LFXP6E-3T144C	100	1.2V	-3	TQFP	144	COM	5.8K
LFXP6E-4T144C	100	1.2V	-4	TQFP	144	COM	5.8K
LFXP6E-5T144C	100	1.2V	-5	TQFP	144	COM	5.8K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10E-3F388C	244	1.2V	-3	fpBGA	388	COM	9.7K
LFXP10E-4F388C	244	1.2V	-4	fpBGA	388	COM	9.7K
LFXP10E-5F388C	244	1.2V	-5	fpBGA	388	COM	9.7K
LFXP10E-3F256C	188	1.2V	-3	fpBGA	256	COM	9.7K
LFXP10E-4F256C	188	1.2V	-4	fpBGA	256	COM	9.7K
LFXP10E-5F256C	188	1.2V	-5	fpBGA	256	COM	9.7K

Part Number	l/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15E-3F484C	300	1.2V	-3	fpBGA	484	COM	15.5K
LFXP15E-4F484C	300	1.2V	-4	fpBGA	484	COM	15.5K
LFXP15E-5F484C	300	1.2V	-5	fpBGA	484	COM	15.5K
LFXP15E-3F388C	268	1.2V	-3	fpBGA	388	COM	15.5K
LFXP15E-4F388C	268	1.2V	-4	fpBGA	388	COM	15.5K
LFXP15E-5F388C	268	1.2V	-5	fpBGA	388	COM	15.5K
LFXP15E-3F256C	188	1.2V	-3	fpBGA	256	COM	15.5K
LFXP15E-4F256C	188	1.2V	-4	fpBGA	256	COM	15.5K
LFXP15E-5F256C	188	1.2V	-5	fpBGA	256	COM	15.5K

## Commercial (Cont.)

			•	,			
Part Number	l/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10E-3FN388I	244	1.2V	-3	fpBGA	388	IND	9.7K
LFXP10E-4FN388I	244	1.2V	-4	fpBGA	388	IND	9.7K
LFXP10E-3FN256I	188	1.2V	-3	fpBGA	256	IND	9.7K
LFXP10E-4FN256I	188	1.2V	-4	fpBGA	256	IND	9.7K

### Industrial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15E-3FN484I	300	1.2V	-3	fpBGA	484	IND	15.5K
LFXP15E-4FN484I	300	1.2V	-4	fpBGA	484	IND	15.5K
LFXP15E-3FN388I	268	1.2V	-3	fpBGA	388	IND	15.5K
LFXP15E-4FN388I	268	1.2V	-4	fpBGA	388	IND	15.5K
LFXP15E-3FN256I	188	1.2V	-3	fpBGA	256	IND	15.5K
LFXP15E-4FN256I	188	1.2V	-4	fpBGA	256	IND	15.5K

Part Number	l/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20E-3FN484I	340	1.2V	-3	fpBGA	484	IND	19.7K
LFXP20E-4FN484I	340	1.2V	-4	fpBGA	484	IND	19.7K
LFXP20E-3FN388I	268	1.2V	-3	fpBGA	388	IND	19.7K
LFXP20E-4FN388I	268	1.2V	-4	fpBGA	388	IND	19.7K
LFXP20E-3FN256I	188	1.2V	-3	fpBGA	256	IND	19.7K
LFXP20E-4FN256I	188	1.2V	-4	fpBGA	256	IND	19.7K