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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	20000
Total RAM Bits	405504
Number of I/O	268
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	388-BBGA
Supplier Device Package	388-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp20e-4fn388c

Table 2-4. PFU Modes of Operation

Logic	Ripple	RAM ¹	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR16x2 x 4 DPR16x2 x 2	ROM16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR16x4 x 2 DPR16x4 x 1	ROM16x2 x 4
LUT 6x 2 or MUX 8x1 x 2	2-bit Counter x 4	SPR16x8 x 1	ROM16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM16x8 x 1

1. These modes are not available in PFF blocks

Routing

There are many resources provided in the LatticeXP devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal, vertical and diagonal directions. The x2 and x6 resources are buffered allowing both short and long connections routing between PFUs.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock Distribution Network

The clock inputs are selected from external I/O, the sysCLOCK™ PLLs or routing. These clock inputs are fed through the chip via a clock distribution system.

Primary Clock Sources

LatticeXP devices derive clocks from three primary sources: PLL outputs, dedicated clock inputs and routing. LatticeXP devices have two to four sysCLOCK PLLs, located on the left and right sides of the device. There are four dedicated clock inputs, one on each side of the device. Figure 2-5 shows the 20 primary clock sources.

Table 2-6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

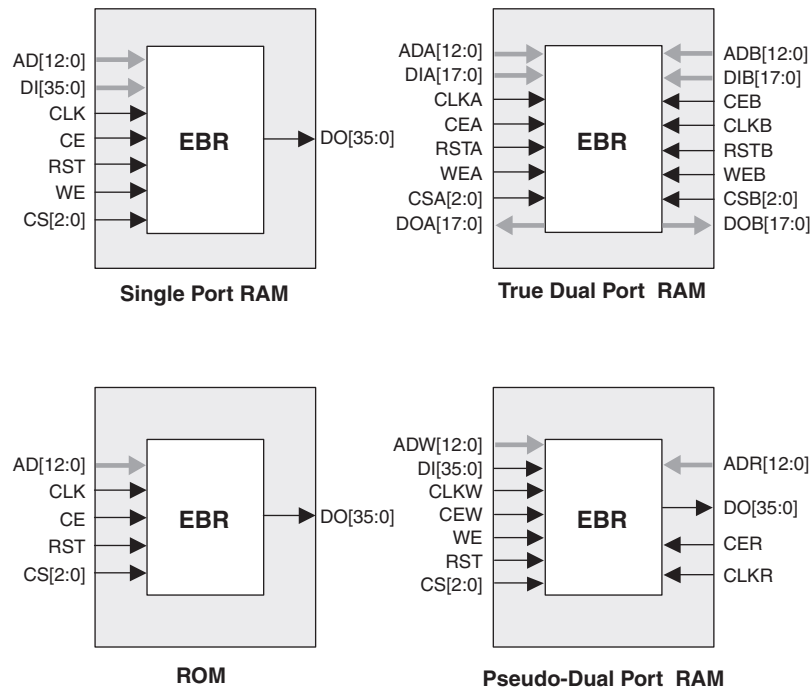
Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

Figure 2-14 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

Figure 2-14. sysMEM Memory Primitives



The EBR memory supports three forms of write behavior for single port or dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** - a copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-15.

Initialization Supply Current^{1, 2, 3, 4, 5, 6}

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ. ⁷	Units
I _{CC}	Core Power Supply	LFXP3E	40	mA
		LFXP6E	50	mA
		LFXP10E	110	mA
		LFXP15E	140	mA
		LFXP20E	250	mA
		LFXP3C	60	mA
		LFXP6C	70	mA
		LFXP10C	150	mA
		LFXP15C	180	mA
		LFXP20C	290	mA
I _{CCAUX}	Auxiliary Power Supply V _{CCAUX} = 3.3V	LFXP3E/C	50	mA
		LFXP6E/C	60	mA
		LFXP10E/C	90	mA
		LFXP15 /C	110	mA
		LFXP20E/C	130	mA
I _{CCJ}	V _{CCJ} Power Supply	All	2	mA

1. Until DONE signal is active.
2. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
4. Frequency 0MHz.
5. Typical user pattern.
6. Assume normal bypass capacitor/decoupling capacitor across the supply.
7. T_A=25°C, power supplies at nominal voltage.

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

LVDS25E

The top and bottom side of LatticeXP devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

Figure 3-1. LVDS25E Output Termination Example

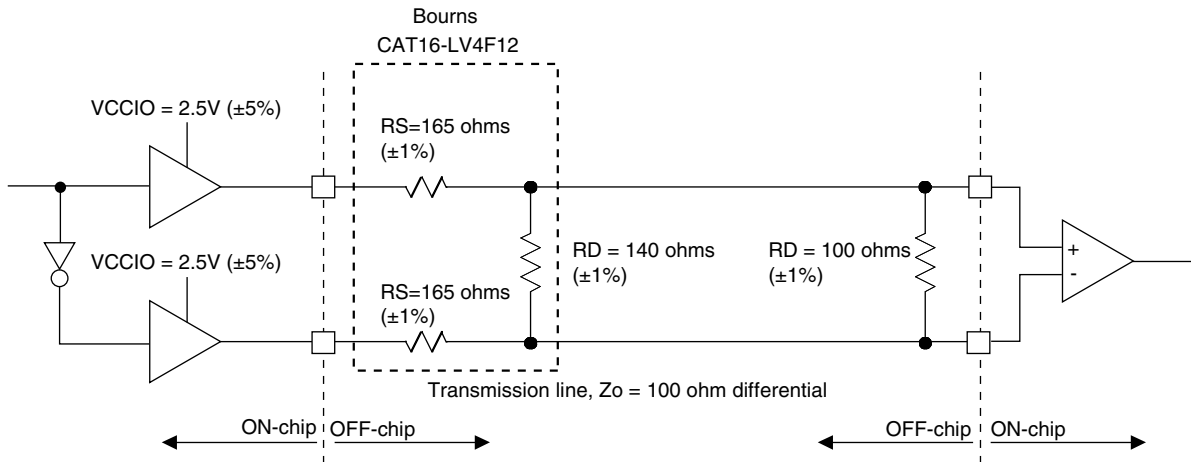


Table 3-1. LVDS25E DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100	ohms
I_{DC}	DC output current	3.66	mA

BLVDS

The LatticeXP devices support BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Timing Diagrams

PFU Timing Diagrams

Figure 3-6. Slice Single/Dual Port Write Cycle Timing

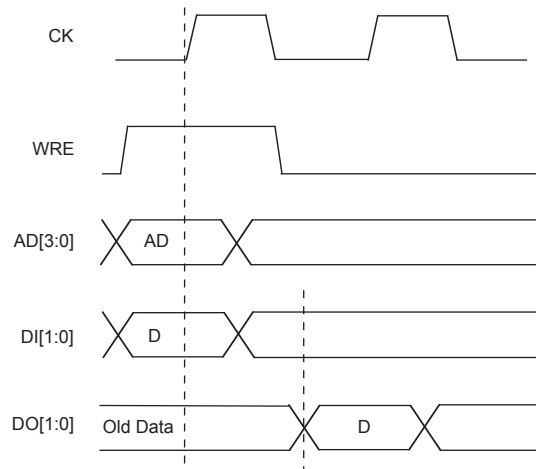
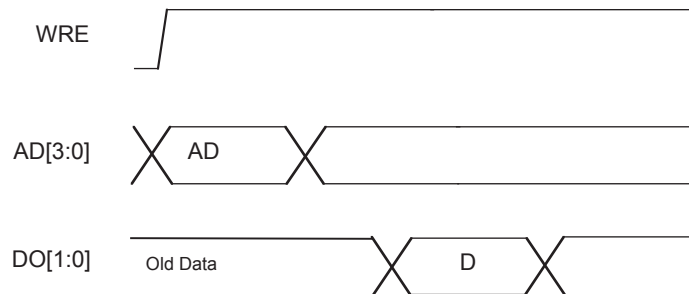


Figure 3-7. Slice Single /Dual Port Read Cycle Timing



LatticeXP sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
sysCONFIG Byte Data Flow				
t _{SUCBDI}	Byte D[0:7] Setup Time to CCLK	7	—	ns
t _{HCBDI}	Byte D[0:7] Hold Time to CCLK	3	—	ns
t _{CODO}	Clock to Dout in Flowthrough Mode	—	12	ns
t _{SUCS}	CS[0:1] Setup Time to CCLK	7	—	ns
t _{HCS}	CS[0:1] Hold Time to CCLK	2	—	ns
t _{SUWD}	Write Signal Setup Time to CCLK	7	—	ns
t _{HWD}	Write Signal Hold Time to CCLK	2	—	ns
t _{DCB}	CCLK to BUSY Delay Time	—	12	ns
t _{CORD}	Clock to Out for Read Data	—	12	ns
sysCONFIG Byte Slave Clocking				
t _{BSCH}	Byte Slave Clock Minimum High Pulse	6	—	ns
t _{BSCL}	Byte Slave Clock Minimum Low Pulse	8	—	ns
t _{BSCYC}	Byte Slave Clock Cycle Time	15	—	ns
sysCONFIG Serial (Bit) Data Flow				
t _{SUSCDI}	DI (Data In) Setup Time to CCLK	7	—	ns
t _{HSCDI}	DI (Data In) Hold Time to CCLK	2	—	ns
t _{CODO}	Clock to Dout in Flowthrough Mode	—	12	ns
sysCONFIG Serial Slave Clocking				
t _{SSCH}	Serial Slave Clock Minimum High Pulse	6	—	ns
t _{SSCL}	Serial Slave Clock Minimum Low Pulse	6	—	ns
sysCONFIG POR, Initialization and Wake Up				
t _{ICFG}	Minimum V _{CC} to INIT High	—	50	ms
t _{VMC}	Time from t _{ICFG} to Valid Master Clock	—	2	us
t _{PRGMRJ}	Program Pin Pulse Rejection	—	7	ns
t _{PRGM} ²	PROGRAMN Low Time to Start Configuration	25	—	ns
t _{DINIT}	INIT Low Time	—	1	ms
t _{DPPINIT}	Delay Time from PROGRAMN Low to INIT Low	—	37	ns
t _{DINITD}	Delay Time from PROGRAMN Low to DONE Low	—	37	ns
t _{IODISS}	User I/O Disable from PROGRAMN Low	—	25	ns
t _{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence	—	25	ns
t _{MWC}	Additional Wake Master Clock Signals after Done Pin High	120	—	cycles
Configuration Master Clock (CCLK)				
Frequency ¹		Selected Value - 30%	Selected Value + 30%	MHz
Duty Cycle		40	60	%

1. See Table 2-10 for available CCLK frequencies.

2. The threshold level for PROGRAMN, as well as for CFG[1] and CFG[0], is determined by V_{CC}, such that the threshold = V_{CC}/2.
Timing v.F0.11

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
P[Edge] [Row/Column Number*]_[A/B]	I/O	<p>[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).</p> <p>[Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.</p> <p>[A/B] indicates the PIO within the PIC to which the pad is connected.</p> <p>Some of these user programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic.</p> <p>During configuration, the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.</p>
GSRN	I	Global RESET signal. (Active low). Any I/O pin can be configured to be GSRN.
NC	—	No connect.
GND	—	GND - Ground. Dedicated Pins.
V _{CC}	—	V _{CC} - The power supply pins for core logic. Dedicated Pins.
V _{CCAUX}	—	V _{CCAUX} - The Auxiliary power supply pin. It powers all the differential and referenced input buffers. Dedicated Pins.
V _{CCP0}	—	Voltage supply pins for ULM0PLL (and LLM1PLL ¹).
V _{CCP1}	—	Voltage supply pins for URM0PLL (and LRM1PLL ¹).
GNDP0	—	Ground pins for ULM0PLL (and LLM1PLL ¹).
GNDP1	—	Ground pins for URM0PLL (and LRM1PLL ¹).
V _{CCIOx}	—	V _{CCIO} - The power supply pins for I/O bank x. Dedicated Pins.
V _{REF1(x)} , V _{REF2(x)}	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V _{REF} inputs. When not used, they may be used as I/O pins.
PLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_PLL[T, C]_IN_A	—	Reference clock (PLL) input Pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A, B, C...at each side.
[LOC][num]_PLL[T, C]_FB_A	—	Optional feedback (PLL) input Pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A, B, C...at each side.
PCLK[T, C]_[n:0]_[3:0]	—	Primary Clock Pads, T = true and C = complement, n per side, indexed by bank and 0,1, 2, 3 within bank.
[LOC]DQS[num]	—	DQS input Pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = Ball function number. Any pad can be configured to be DQS output.

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
1	CFG1	0	-	-	CFG1	0	-	-
2	DONE	0	-	-	DONE	0	-	-
3	PROGRAMN	7	-	-	PROGRAMN	7	-	-
4	CCLK	7	-	-	CCLK	7	-	-
5	GND	-	-	-	GND	-	-	-
6	PL2A	7	T ³	-	PL2A	7	T ³	-
7	GNDIO7	7	-	-	GNDIO7	7	-	-
8	PL2B	7	C ³	-	PL2B	7	C ³	-
9	PL3A	7	T	LUM0_PLLT_FB_A	PL3A	7	T	LUM0_PLLT_FB_A
10	PL3B	7	C	LUM0_PLLC_FB_A	PL3B	7	C	LUM0_PLLC_FB_A
11	PL4A	7	T ³	-	PL4A	7	T ³	-
12	PL4B	7	C ³	-	PL4B	7	C ³	-
13	VCCIO7	7	-	-	VCCIO7	7	-	-
14	PL5A	7	-	VREF1_7	PL5A	7	-	VREF1_7
15	PL6B	7	-	VREF2_7	PL6B	7	-	VREF2_7
16	GNDIO7	7	-	-	GNDIO7	7	-	-
17	PL7A	7	T ³	DQS	PL7A	7	T ³	DQS
18	PL7B	7	C ³	-	PL7B	7	C ³	-
19	VCC	-	-	-	VCC	-	-	-
20	PL8A	7	T	LUM0_PLLT_IN_A	PL8A	7	T	LUM0_PLLT_IN_A
21	PL8B	7	C	LUM0_PLLC_IN_A	PL8B	7	C	LUM0_PLLC_IN_A
22	PL9A	7	T ³	-	PL9A	7	T ³	-
23	VCCIO7	7	-	-	VCCIO7	7	-	-
24	PL9B	7	C ³	-	PL9B	7	C ³	-
25	VCCP0	-	-	-	VCCP0	-	-	-
26	GNDP0	-	-	-	GNDP0	-	-	-
27	NC	-	-	-	PL15B	6	-	-
28	VCCIO6	6	-	-	VCCIO6	6	-	-
29	PL11A	6	T ³	-	PL16A	6	T ³	-
30	PL11B	6	C ³	-	PL16B	6	C ³	-
31	PL12A	6	T	PCLKT6_0	PL17A	6	T	PCLKT6_0
32	PL12B	6	C	PCLKC6_0	PL17B	6	C	PCLKC6_0
33	NC	-	-	-	PL18A	6	T ³	-
34	NC	-	-	-	PL18B	6	C ³	-
35	VCC	-	-	-	VCC	-	-	-
36	PL13A	6	T ³	-	PL21A	6	T ³	-
37	PL13B	6	C ³	-	PL21B	6	C ³	-
38	GNDIO6	6	-	-	GNDIO6	6	-	-
39	PL14A	6	-	VREF1_6	PL22A	6	-	VREF1_6
40	PL15B	6	-	VREF2_6	PL23B	6	-	VREF2_6
41	VCCIO6	6	-	-	VCCIO6	6	-	-
42	PL16A	6	T ³	DQS	PL24A	6	T ³	DQS
43	PL16B	6	C ³	-	PL24B	6	C ³	-
44	PL17A	6	T	-	PL25A	6	T	-
45	PL17B	6	C	-	PL25B	6	C	-
46	PL18A	6	T ³	-	PL26A	6	T ³	-

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
93	PB19B	4	C	VREF1_4	PB22B	4	C	VREF1_4
94	PB20A	4	T	-	PB23A	4	T	-
95	PB20B	4	C	-	PB23B	4	C	-
96	PB21A	4	T	-	PB24A	4	T	-
97	VCCIO4	4	-	-	VCCIO4	4	-	-
98	PB21B	4	C	-	PB24B	4	C	-
99	PB22A	4	T	-	PB25A	4	T	-
100	PB22B	4	C	-	PB25B	4	C	-
101	PB23A	4	T	-	PB26A	4	T	-
102	PB23B	4	C	-	PB26B	4	C	-
103	PB24A	4	T	VREF2_4	PB27A	4	-	VREF2_4
104	PB24B	4	C	-	PB30A	4	T	DQS
105	PB25A	4	-	-	PB30B	4	C	-
106	GND	-	-	-	GND	-	-	-
107	VCC	-	-	-	VCC	-	-	-
108	PR18B	3	C ³	-	PR26B	3	C ³	-
109	GNDIO3	3	-	-	GNDIO3	3	-	-
110	PR18A	3	T ³	-	PR26A	3	T ³	-
111	PR17B	3	C	-	PR25B	3	C	-
112	PR17A	3	T	-	PR25A	3	T	-
113	PR16B	3	C ³	-	PR24B	3	C ³	-
114	PR16A	3	T ³	DQS	PR24A	3	T ³	DQS
115	VCCIO3	3	-	-	VCCIO3	3	-	-
116	PR15B	3	-	VREF1_3	PR23B	3	-	VREF1_3
117	PR14A	3	-	VREF2_3	PR22A	3	-	VREF2_3
118	GNDIO3	3	-	-	GNDIO3	3	-	-
119	PR13B	3	C	-	PR21B	3	C ³	-
120	PR13A	3	T	-	PR21A	3	T ³	-
121	GND	-	-	-	GND	-	-	-
122	PR12B	3	C	-	PR20B	3	C	-
123	PR12A	3	T	-	PR20A	3	T	-
124	PR11B	3	C	-	PR19B	3	C ³	-
125	VCCIO3	3	-	-	VCCIO3	3	-	-
126	PR11A	3	T	-	PR19A	3	T ³	-
127	GNDP1	-	-	-	GNDP1	-	-	-
128	VCCP1	-	-	-	VCCP1	-	-	-
129	NC	-	-	-	PR13A	2	-	-
130	GND	-	-	-	GND	-	-	-
131	PR9B	2	C	PCLKC2_0	PR12B	2	C	PCLKC2_0
132	PR9A	2	T	PCLKT2_0	PR12A	2	T	PCLKT2_0
133	NC	-	-	-	PR11B	2	C ³	-
134	NC	-	-	-	PR11A	2	T ³	-
135	GNDIO2	2	-	-	GNDIO2	2	-	-
136	PR8B	2	C	RUM0_PLLC_IN_A	PR8B	2	C	RUM0_PLLC_IN_A
137	PR8A	2	T	RUM0_PLLT_IN_A	PR8A	2	T	RUM0_PLLT_IN_A
138	PR7B	2	C ³	-	PR7B	2	C ³	-

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
139	PR7A	2	T ³	DQS	PR7A	2	T ³	DQS
140	VCCIO2	2	-	-	VCCIO2	2	-	-
141	PR6B	2	-	VREF1_2	PR6B	2	-	VREF1_2
142	PR5A	2	-	VREF2_2	PR5A	2	-	VREF2_2
143	GNDIO2	2	-	-	GNDIO2	2	-	-
144	PR4B	2	C ³	-	PR4B	2	C ³	-
145	PR4A	2	T ³	-	PR4A	2	T ³	-
146	PR3B	2	C	RUM0_PLLC_FB_A	PR3B	2	C	RUM0_PLLC_FB_A
147	PR3A	2	T	RUM0_PLLT_FB_A	PR3A	2	T	RUM0_PLLT_FB_A
148	PR2B	2	C ³	-	PR2B	2	C ³	-
149	VCCIO2	2	-	-	VCCIO2	2	-	-
150	PR2A	2	T ³	-	PR2A	2	T ³	-
151	VCC	-	-	-	VCC	-	-	-
152	VCCAUX	-	-	-	VCCAUX	-	-	-
153	TDO	-	-	-	TDO	-	-	-
154	VCCJ	-	-	-	VCCJ	-	-	-
155	TDI	-	-	-	TDI	-	-	-
156	TMS	-	-	-	TMS	-	-	-
157	TCK	-	-	-	TCK	-	-	-
158	VCC	-	-	-	VCC	-	-	-
159	PT25A	1	-	VREF1_1	PT28A	1	-	VREF1_1
160	PT24B	1	C	-	PT27B	1	C	-
161	PT24A	1	T	-	PT27A	1	T	-
162	PT23A	1	-	D0	PT26A	1	-	D0
163	GNDIO1	1	-	-	GNDIO1	1	-	-
164	PT22B	1	C	D1	PT25B	1	C	D1
165	PT22A	1	T	VREF2_1	PT25A	1	T	VREF2_1
166	PT21A	1	-	D2	PT24A	1	-	D2
167	VCCIO1	1	-	-	VCCIO1	1	-	-
168	PT20B	1	C	D3	PT23B	1	C	D3
169	PT20A	1	T	-	PT23A	1	T	-
170	PT19B	1	C	-	PT22B	1	C	-
171	PT19A	1	T	DQS	PT22A	1	T	DQS
172	GNDIO1	1	-	-	GNDIO1	1	-	-
173	PT18B	1	-	-	PT21B	1	-	-
174	PT17A	1	-	D4	PT20A	1	-	D4
175	PT16B	1	C	-	PT19B	1	C	-
176	PT16A	1	T	D5	PT19A	1	T	D5
177	VCCIO1	1	-	-	VCCIO1	1	-	-
178	PT15B	1	C	D6	PT18B	1	C	D6
179	PT15A	1	T	-	PT18A	1	T	-
180	PT14B	1	-	D7	PT17B	1	-	D7
181	GND	-	-	-	GND	-	-	-
182	VCC	-	-	-	VCC	-	-	-
183	PT13B	0	C	BUSY	PT16B	0	C	BUSY
184	GNDIO0	0	-	-	GNDIO0	0	-	-

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP6				LFXP10			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
E8	PT13B	0	-	-	PT17B	0	-	-
D8	PT12A	0	-	DOUT	PT16A	0	-	DOUT
A6	PT11B	0	C	-	PT15B	0	C	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
C6	PT11A	0	T	WRITEN	PT15A	0	T	WRITEN
E7	PT10B	0	C	-	PT14B	0	C	-
D7	PT10A	0	T	VREF1_0	PT14A	0	T	VREF1_0
A5	PT9B	0	C	-	PT13B	0	C	-
B5	PT9A	0	T	DI	PT13A	0	T	DI
A4	PT8B	0	C	-	PT12B	0	C	-
B6	PT8A	0	T	CSN	PT12A	0	T	CSN
E6	PT7B	0	C	-	PT11B	0	C	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
D6	PT7A	0	T	-	PT11A	0	T	-
D5	PT6B	0	C	VREF2_0	PT10B	0	C	VREF2_0
A3	PT6A	0	T	DQS	PT10A	0	T	DQS
B3	PT5B	0	-	-	PT9B	0	-	-
B2	PT4A	0	-	-	PT8A	0	-	-
A2	PT3B	0	C	-	PT7B	0	C	-
B1	PT3A	0	T	-	PT7A	0	T	-
F5	PT2B	0	C	-	PT6B	0	C	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
C5	PT2A	0	T	-	PT6A	0	T	-
C4	CFG0	0	-	-	CFG0	0	-	-
B4	CFG1	0	-	-	CFG1	0	-	-
C3	DONE	0	-	-	DONE	0	-	-
A1	GND	-	-	-	GND	-	-	-
A16	GND	-	-	-	GND	-	-	-
F11	GND	-	-	-	GND	-	-	-
F6	GND	-	-	-	GND	-	-	-
G10	GND	-	-	-	GND	-	-	-
G7	GND	-	-	-	GND	-	-	-
G8	GND	-	-	-	GND	-	-	-
G9	GND	-	-	-	GND	-	-	-
H10	GND	-	-	-	GND	-	-	-
H7	GND	-	-	-	GND	-	-	-
H8	GND	-	-	-	GND	-	-	-
H9	GND	-	-	-	GND	-	-	-
J10	GND	-	-	-	GND	-	-	-
J7	GND	-	-	-	GND	-	-	-
J8	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
A9	PT27A	1	T	-	PT31A	1	T	-
C9	PT26B	1	C	D7	PT30B	1	C	D7
C8	PT26A	1	T	-	PT30A	1	T	-
E9	PT25B	0	C	BUSY	PT29B	0	C	BUSY
-	GNDIO0	0	-	-	GNDIO0	0	-	-
B8	PT25A	0	T	CS1N	PT29A	0	T	CS1N
A8	PT24B	0	C	PCLKC0_0	PT28B	0	C	PCLKC0_0
A7	PT24A	0	T	PCLKT0_0	PT28A	0	T	PCLKT0_0
B7	PT23B	0	C	-	PT27B	0	C	-
C7	PT23A	0	T	DQS	PT27A	0	T	DQS
E8	PT22B	0	-	-	PT26B	0	-	-
D8	PT21A	0	-	DOUT	PT25A	0	-	DOUT
A6	PT20B	0	C	-	PT24B	0	C	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
C6	PT20A	0	T	WRITEN	PT24A	0	T	WRITEN
E7	PT19B	0	C	-	PT23B	0	C	-
D7	PT19A	0	T	VREF1_0	PT23A	0	T	VREF1_0
A5	PT18B	0	C	-	PT22B	0	C	-
B5	PT18A	0	T	DI	PT22A	0	T	DI
A4	PT17B	0	C	-	PT21B	0	C	-
B6	PT17A	0	T	CSN	PT21A	0	T	CSN
E6	PT16B	0	C	-	PT20B	0	C	-
D6	PT16A	0	T	-	PT20A	0	T	-
D5	PT15B	0	C	VREF2_0	PT19B	0	C	VREF2_0
A3	PT15A	0	T	DQS	PT19A	0	T	DQS
B3	PT14B	0	-	-	PT18B	0	-	-
B2	PT13A	0	-	-	PT17A	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
A2	PT12B	0	C	-	PT16B	0	C	-
B1	PT12A	0	T	-	PT16A	0	T	-
F5	PT11B	0	C	-	PT15B	0	C	-
C5	PT11A	0	T	-	PT15A	0	T	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
C4	CFG0	0	-	-	CFG0	0	-	-
B4	CFG1	0	-	-	CFG1	0	-	-
C3	DONE	0	-	-	DONE	0	-	-
A1	GND	-	-	-	GND	-	-	-
A16	GND	-	-	-	GND	-	-	-
F11	GND	-	-	-	GND	-	-	-
F6	GND	-	-	-	GND	-	-	-

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
G10	GND	-	-	-	GND	-	-	-
G7	GND	-	-	-	GND	-	-	-
G8	GND	-	-	-	GND	-	-	-
G9	GND	-	-	-	GND	-	-	-
H10	GND	-	-	-	GND	-	-	-
H7	GND	-	-	-	GND	-	-	-
H8	GND	-	-	-	GND	-	-	-
H9	GND	-	-	-	GND	-	-	-
J10	GND	-	-	-	GND	-	-	-
J7	GND	-	-	-	GND	-	-	-
J8	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-
K10	GND	-	-	-	GND	-	-	-
K7	GND	-	-	-	GND	-	-	-
K8	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-
L6	GND	-	-	-	GND	-	-	-
T1	GND	-	-	-	GND	-	-	-
T16	GND	-	-	-	GND	-	-	-
D13	VCC	-	-	-	VCC	-	-	-
D4	VCC	-	-	-	VCC	-	-	-
E12	VCC	-	-	-	VCC	-	-	-
E5	VCC	-	-	-	VCC	-	-	-
M12	VCC	-	-	-	VCC	-	-	-
M5	VCC	-	-	-	VCC	-	-	-
N13	VCC	-	-	-	VCC	-	-	-
N4	VCC	-	-	-	VCC	-	-	-
E13	VCCAUX	-	-	-	VCCAUX	-	-	-
E4	VCCAUX	-	-	-	VCCAUX	-	-	-
M13	VCCAUX	-	-	-	VCCAUX	-	-	-
M4	VCCAUX	-	-	-	VCCAUX	-	-	-
F7	VCCIO0	0	-	-	VCCIO0	0	-	-
F8	VCCIO0	0	-	-	VCCIO0	0	-	-
F10	VCCIO1	1	-	-	VCCIO1	1	-	-
F9	VCCIO1	1	-	-	VCCIO1	1	-	-
G11	VCCIO2	2	-	-	VCCIO2	2	-	-
H11	VCCIO2	2	-	-	VCCIO2	2	-	-
J11	VCCIO3	3	-	-	VCCIO3	3	-	-
K11	VCCIO3	3	-	-	VCCIO3	3	-	-
L10	VCCIO4	4	-	-	VCCIO4	4	-	-
L9	VCCIO4	4	-	-	VCCIO4	4	-	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
C20	PT38A	1	T	-	PT43A	1	T	-	PT47A	1	T	-
C21	PT37B	1	C	-	PT42B	1	C	-	PT46B	1	C	-
C22	PT37A	1	T	-	PT42A	1	T	-	PT46A	1	T	-
B22	PT36B	1	C	-	PT41B	1	C	-	PT45B	1	C	-
A21	PT36A	1	T	-	PT41A	1	T	-	PT45A	1	T	-
D15	PT35B	1	C	-	PT40B	1	C	-	PT44B	1	C	-
D14	PT35A	1	T	-	PT40A	1	T	-	PT44A	1	T	-
B21	PT34B	1	C	VREF1_1	PT39B	1	C	VREF1_1	PT43B	1	C	VREF1_1
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
A20	PT34A	1	T	DQS	PT39A	1	T	DQS	PT43A	1	T	DQS
B20	PT33B	1	-	-	PT38B	1	-	-	PT42B	1	-	-
A19	PT32A	1	-	-	PT37A	1	-	-	PT41A	1	-	-
B19	PT31B	1	C	-	PT36B	1	C	-	PT40B	1	C	-
A18	PT31A	1	T	-	PT36A	1	T	-	PT40A	1	T	-
C14	PT30B	1	C	-	PT35B	1	C	-	PT39B	1	C	-
C13	PT30A	1	T	D0	PT35A	1	T	D0	PT39A	1	T	D0
B18	PT29B	1	C	D1	PT34B	1	C	D1	PT38B	1	C	D1
A17	PT29A	1	T	VREF2_1	PT34A	1	T	VREF2_1	PT38A	1	T	VREF2_1
B17	PT28B	1	C	-	PT33B	1	C	-	PT37B	1	C	-
A16	PT28A	1	T	D2	PT33A	1	T	D2	PT37A	1	T	D2
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
B16	PT27B	1	C	D3	PT32B	1	C	D3	PT36B	1	C	D3
A15	PT27A	1	T	-	PT32A	1	T	-	PT36A	1	T	-
B15	PT26B	1	C	-	PT31B	1	C	-	PT35B	1	C	-
A14	PT26A	1	T	DQS	PT31A	1	T	DQS	PT35A	1	T	DQS
D13	PT25B	1	-	-	PT30B	1	-	-	PT34B	1	-	-
D12	PT24A	1	-	D4	PT29A	1	-	D4	PT33A	1	-	D4
B14	PT23B	1	C	-	PT28B	1	C	-	PT32B	1	C	-
A13	PT23A	1	T	D5	PT28A	1	T	D5	PT32A	1	T	D5
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
B13	PT22B	1	C	D6	PT27B	1	C	D6	PT31B	1	C	D6
A12	PT22A	1	T	-	PT27A	1	T	-	PT31A	1	T	-
B12	PT21B	1	C	D7	PT26B	1	C	D7	PT30B	1	C	D7
C12	PT21A	1	T	-	PT26A	1	T	-	PT30A	1	T	-
C11	PT20B	0	C	BUSY	PT25B	0	C	BUSY	PT29B	0	C	BUSY
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
B11	PT20A	0	T	CS1N	PT25A	0	T	CS1N	PT29A	0	T	CS1N
A11	PT19B	0	C	PCLKC0_0	PT24B	0	C	PCLKC0_0	PT28B	0	C	PCLKC0_0
A10	PT19A	0	T	PCLKT0_0	PT24A	0	T	PCLKT0_0	PT28A	0	T	PCLKT0_0
B10	PT18B	0	C	-	PT23B	0	C	-	PT27B	0	C	-
B9	PT18A	0	T	DQS	PT23A	0	T	DQS	PT27A	0	T	DQS
D11	PT17B	0	-	-	PT22B	0	-	-	PT26B	0	-	-
D10	PT16A	0	-	DOUT	PT21A	0	-	DOUT	PT25A	0	-	DOUT
A9	PT15B	0	C	-	PT20B	0	C	-	PT24B	0	C	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C8	PT15A	0	T	WRITEN	PT20A	0	T	WRITEN	PT24A	0	T	WRITEN
B8	PT14B	0	C	-	PT19B	0	C	-	PT23B	0	C	-
A8	PT14A	0	T	VREF1_0	PT19A	0	T	VREF1_0	PT23A	0	T	VREF1_0
C7	PT13B	0	C	-	PT18B	0	C	-	PT22B	0	C	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
F5	PROGRAMN	7	-	-	PROGRAMN	7	-	-
E3	CCLK	7	-	-	CCLK	7	-	-
C1	PL2B	7	-	-	PL2B	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
G5	PL3A	7	T ³	-	PL3A	7	T ³	-
G6	PL3B	7	C ³	-	PL3B	7	C ³	-
F4	PL4A	7	T	-	PL4A	7	T	-
F3	PL4B	7	C	-	PL4B	7	C	-
G4	PL5A	7	T ³	-	PL5A	7	T ³	-
G3	PL5B	7	C ³	-	PL5B	7	C ³	-
D1	PL6A	7	T ³	-	PL6A	7	T ³	-
D2	PL6B	7	C ³	-	PL6B	7	C ³	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
E1	PL7A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A
E2	PL7B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A
H5	PL8A	7	T ³	-	PL8A	7	T ³	-
H6	PL8B	7	C ³	-	PL8B	7	C ³	-
H4	PL9A	7	-	-	PL9A	7	-	-
H3	PL10B	7	-	VREF1_7	PL10B	7	-	VREF1_7
F1	PL11A	7	T ³	DQS	PL11A	7	T ³	DQS
F2	PL11B	7	C ³	-	PL11B	7	C ³	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
J5	PL12A	7	T	-	PL12A	7	T	-
J6	PL12B	7	C	-	PL12B	7	C	-
G1	PL13A	7	T ³	-	PL13A	7	T ³	-
G2	PL13B	7	C ³	-	PL13B	7	C ³	-
J4	PL15A	7	T ³	-	PL15A	7	T ³	-
J3	PL15B	7	C ³	-	PL15B	7	C ³	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
H1	PL16A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A
H2	PL16B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A
J1	PL17A	7	T ³	-	PL17A	7	T ³	-
J2	PL17B	7	C ³	-	PL17B	7	C ³	-
K3	PL18A	7	-	VREF2_7	PL18A	7	-	VREF2_7
K2	PL19B	7	-	-	PL19B	7	-	-
K4	PL20A	7	T ³	DQS	PL20A	7	T ³	DQS
-	GNDIO7	7	-	-	GNDIO7	7	-	-
K5	PL20B	7	C ³	-	PL20B	7	C ³	-
K1	PL21A	7	T	-	PL21A	7	T	-
L2	PL21B	7	C	-	PL21B	7	C	-
L4	PL22A	7	T ³	-	PL22A	7	T ³	-
L3	PL22B	7	C ³	-	PL22B	7	C ³	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
AB5	PB16A	5	T	-	PB20A	5	T	-
AB6	PB16B	5	C	-	PB20B	5	C	-
AA8	PB17A	5	T	-	PB21A	5	T	-
AA9	PB17B	5	C	VREF2_5	PB21B	5	C	VREF2_5
W10	PB18A	5	T	-	PB22A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
V10	PB18B	5	C	-	PB22B	5	C	-
AB7	PB19A	5	T	-	PB23A	5	T	-
AB8	PB19B	5	C	-	PB23B	5	C	-
AB9	PB20A	5	T	-	PB24A	5	T	-
AB10	PB20B	5	C	-	PB24B	5	C	-
Y10	PB21A	5	-	-	PB25A	5	-	-
AA10	PB22B	5	-	-	PB26B	5	-	-
W11	PB23A	5	T	DQS	PB27A	5	T	DQS
V11	PB23B	5	C	-	PB27B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y11	PB24A	5	T	-	PB28A	5	T	-
AA11	PB24B	5	C	-	PB28B	5	C	-
AB11	PB25A	5	T	-	PB29A	5	T	-
AB12	PB25B	5	C	-	PB29B	5	C	-
Y12	PB26A	4	T	-	PB30A	4	T	-
AA12	PB26B	4	C	-	PB30B	4	C	-
W12	PB27A	4	T	PCLKT4_0	PB31A	4	T	PCLKT4_0
V12	PB27B	4	C	PCLKC4_0	PB31B	4	C	PCLKC4_0
-	GNDIO4	4	-	-	GNDIO4	4	-	-
AB13	PB28A	4	T	-	PB32A	4	T	-
AB14	PB28B	4	C	-	PB32B	4	C	-
AA13	PB29A	4	-	-	PB33A	4	-	-
Y13	PB30B	4	-	-	PB34B	4	-	-
AB15	PB31A	4	T	DQS	PB35A	4	T	DQS
AB16	PB31B	4	C	VREF1_4	PB35B	4	C	VREF1_4
V13	PB32A	4	T	-	PB36A	4	T	-
W13	PB32B	4	C	-	PB36B	4	C	-
AA14	PB33A	4	T	-	PB37A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA15	PB33B	4	C	-	PB37B	4	C	-
AB17	PB34A	4	T	-	PB38A	4	T	-
AB18	PB34B	4	C	-	PB38B	4	C	-
W14	PB35A	4	T	-	PB39A	4	T	-
Y14	PB35B	4	C	-	PB39B	4	C	-
U14	PB36A	4	T	VREF2_4	PB40A	4	T	VREF2_4
V14	PB36B	4	C	-	PB40B	4	C	-

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following located on the Lattice website at www.latticesemi.com.

- Thermal Management document
- Technical Note TN1052 - Power Estimation and Management for LatticeECP/EC and LatticeXP Devices
- Power Calculator tool included with Lattice's ispLEVER design tool, or as a standalone download from www.latticesemi.com/software

Industrial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15C-3F484I	300	1.8/2.5/3.3V	-3	fpBGA	484	IND	15.5K
LFXP15C-4F484I	300	1.8/2.5/3.3V	-4	fpBGA	484	IND	15.5K
LFXP15C-3F388I	268	1.8/2.5/3.3V	-3	fpBGA	388	IND	15.5K
LFXP15C-4F388I	268	1.8/2.5/3.3V	-4	fpBGA	388	IND	15.5K
LFXP15C-3F256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	15.5K
LFXP15C-4F256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	15.5K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20C-3F484I	340	1.8/2.5/3.3V	-3	fpBGA	484	IND	19.7K
LFXP20C-4F484I	340	1.8/2.5/3.3V	-4	fpBGA	484	IND	19.7K
LFXP20C-3F388I	268	1.8/2.5/3.3V	-3	fpBGA	388	IND	19.7K
LFXP20C-4F388I	268	1.8/2.5/3.3V	-4	fpBGA	388	IND	19.7K
LFXP20C-3F256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	19.7K
LFXP20C-4F256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	19.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3E-3Q208I	136	1.2V	-3	PQFP	208	IND	3.1K
LFXP3E-4Q208I	136	1.2V	-4	PQFP	208	IND	3.1K
LFXP3E-3T144I	100	1.2V	-3	TQFP	144	IND	3.1K
LFXP3E-4T144I	100	1.2V	-4	TQFP	144	IND	3.1K
LFXP3E-3T100I	62	1.2V	-3	TQFP	100	IND	3.1K
LFXP3E-4T100I	62	1.2V	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6E-3F256I	188	1.2V	-3	fpBGA	256	IND	5.8K
LFXP6E-4F256I	188	1.2V	-4	fpBGA	256	IND	5.8K
LFXP6E-3Q208I	142	1.2V	-3	PQFP	208	IND	5.8K
LFXP6E-4Q208I	142	1.2V	-4	PQFP	208	IND	5.8K
LFXP6E-3T144I	100	1.2V	-3	TQFP	144	IND	5.8K
LFXP6E-4T144I	100	1.2V	-4	TQFP	144	IND	5.8K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10E-3F388I	244	1.2V	-3	fpBGA	388	IND	9.7K
LFXP10E-4F388I	244	1.2V	-4	fpBGA	388	IND	9.7K
LFXP10E-3F256I	188	1.2V	-3	fpBGA	256	IND	9.7K
LFXP10E-4F256I	188	1.2V	-4	fpBGA	256	IND	9.7K

Industrial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10E-3FN388I	244	1.2V	-3	fpBGA	388	IND	9.7K
LFXP10E-4FN388I	244	1.2V	-4	fpBGA	388	IND	9.7K
LFXP10E-3FN256I	188	1.2V	-3	fpBGA	256	IND	9.7K
LFXP10E-4FN256I	188	1.2V	-4	fpBGA	256	IND	9.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15E-3FN484I	300	1.2V	-3	fpBGA	484	IND	15.5K
LFXP15E-4FN484I	300	1.2V	-4	fpBGA	484	IND	15.5K
LFXP15E-3FN388I	268	1.2V	-3	fpBGA	388	IND	15.5K
LFXP15E-4FN388I	268	1.2V	-4	fpBGA	388	IND	15.5K
LFXP15E-3FN256I	188	1.2V	-3	fpBGA	256	IND	15.5K
LFXP15E-4FN256I	188	1.2V	-4	fpBGA	256	IND	15.5K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20E-3FN484I	340	1.2V	-3	fpBGA	484	IND	19.7K
LFXP20E-4FN484I	340	1.2V	-4	fpBGA	484	IND	19.7K
LFXP20E-3FN388I	268	1.2V	-3	fpBGA	388	IND	19.7K
LFXP20E-4FN388I	268	1.2V	-4	fpBGA	388	IND	19.7K
LFXP20E-3FN256I	188	1.2V	-3	fpBGA	256	IND	19.7K
LFXP20E-4FN256I	188	1.2V	-4	fpBGA	256	IND	19.7K