Lattice Semiconductor Corporation - LFXP20E-4FN484C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	20000
Total RAM Bits	405504
Number of I/O	340
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp20e-4fn484c

Introduction

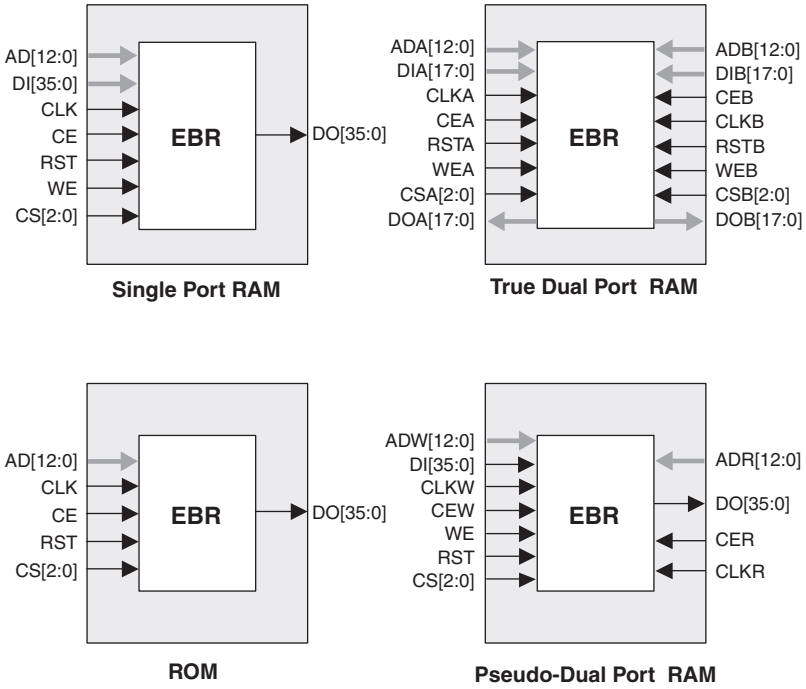
The LatticeXP family of FPGA devices combine logic gates, embedded memory and high performance I/Os in a single architecture that is both non-volatile and infinitely reconfigurable to support cost-effective system designs.

The re-programmable non-volatile technology used in the LatticeXP family is the next generation ispXP™ technology. With this technology, expensive external configuration memories are not required and designs are secured from unauthorized read-back. In addition, instant-on capability allows for easy interfacing in many applications.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeXP family of FPGA devices. Synthesis library support for LatticeXP is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeXP device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeXP family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Figure 2-14. sysMEM Memory Primitives



The EBR memory supports three forms of write behavior for single port or dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** -þa copy of the input data appears at the output of the same port during a write cycle.þThis mode is supported for all data widths.

3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-15.

master serial clock is 2.5MHz. Table 2-10 lists all the available Master Serial Clock frequencies. When a different Master Serial Clock is selected during the design process, the following sequence takes place:

1. User selects a different Master Serial Clock frequency for configuration.
2. During configuration the device starts with the default (2.5MHz) Master Serial Clock frequency.
3. The clock configuration settings are contained in the early configuration bit stream.
4. The Master Serial Clock frequency changes to the selected frequency once the clock configuration bits are received.

For further information on the use of this oscillator for configuration, please see details of additional technical documentation at the end of this data sheet.

Table 2-10. Selectable Master Serial Clock (CCLK) Frequencies During Configuration

CCLK (MHz)	CCLK (MHz)	CCLK (MHz)
2.5[1]	13	45
4.3	15	51
5.4	20	55
6.9	26	60
8.1	30	130
9.2	34	—
10.0	41	—

1. Default

Density Shifting

The LatticeXP family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

Supply Current (Standby)[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LFXP3E	15	mA
		LFXP6E	20	mA
		LFXP10E	35	mA
		LFXP15E	45	mA
		LFXP20E	55	mA
		LFXP3C	35	mA
		LFXP6C	40	mA
		LFXP10C	70	mA
		LFXP15C	80	mA
		LFXP20C	90	mA
I_{CCP}	PLL Power Supply (per PLL)	All	8	mA
I_{CCAUX}	Auxiliary Power Supply V_{CCAUX} = 3.3V	LFXP3E/C	22	mA
		LFXP6E/C	22	mA
		LFXP10E/C	30	mA
		LFXP15E/C	30	mA
		LFXP20E/C	30	mA
I_{CCIO}	Bank Power Supply[6]	All	2	mA
I_{CCJ}	V_{CCJ} Power Supply	All	1	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the VCCIO or GND.
3. Frequency 0MHz.
4. User pattern: blank.
5. T_A=25°C, power supplies at nominal voltage.
6. Per bank.

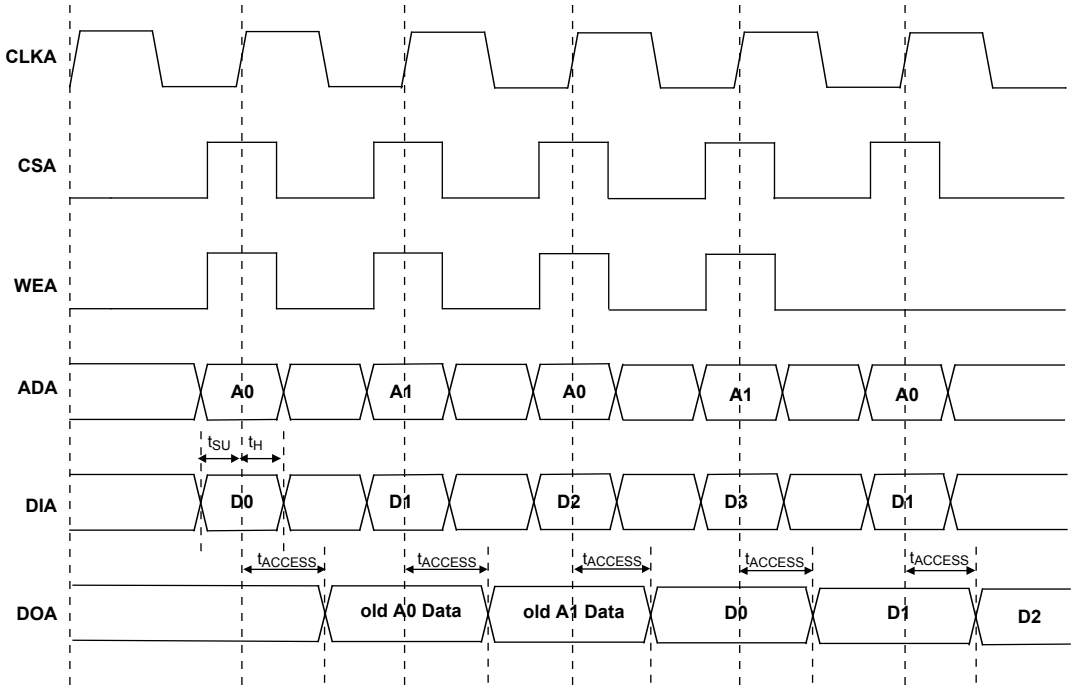
Initialization Supply Current[1, 2, 3, 4, 5, 6]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[7]	Units
I_{CC}	Core Power Supply	LFXP3E	40	mA
		LFXP6E	50	mA
		LFXP10E	110	mA
		LFXP15E	140	mA
		LFXP20E	250	mA
		LFXP3C	60	mA
		LFXP6C	70	mA
		LFXP10C	150	mA
		LFXP15C	180	mA
		LFXP20C	290	mA
I_{CCAUX}	Auxiliary Power Supply V_{CCAUX} = 3.3V	LFXP3E/C	50	mA
		LFXP6E/C	60	mA
		LFXP10E/C	90	mA
		LFXP15 /C	110	mA
		LFXP20E/C	130	mA
I_{CCJ}	V_{CCJ} Power Supply	All	2	mA

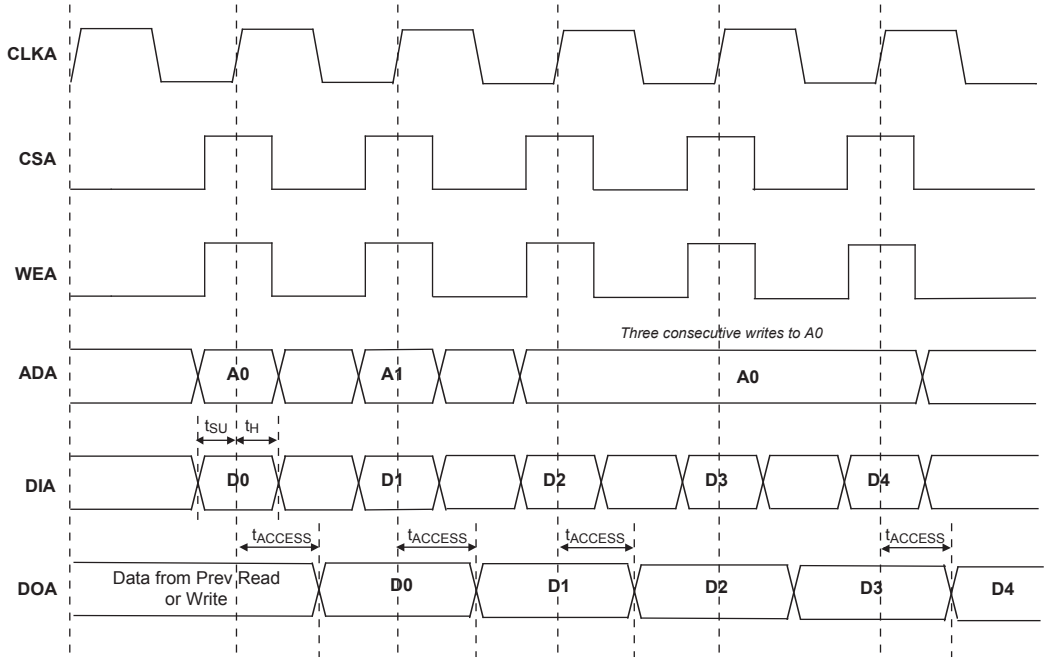
1. Until DONE signal is active.
2. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
4. Frequency 0MHz.
5. Typical user pattern.
6. Assume normal bypass capacitor/decoupling capacitor across the supply.
7. T_A=25°C, power supplies at nominal voltage.

Figure 3-10. Read Before Write (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

Figure 3-11. Write Through (SP Read/Write On Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

LatticeXP sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
sysCONFIG Byte Data Flow				
t_{SUCBDI}	Byte D[0:7] Setup Time to CCLK	7	—	ns
t_{HCBDI}	Byte D[0:7] Hold Time to CCLK	3	—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	—	12	ns
t_{SUCS}	CS[0:1] Setup Time to CCLK	7	—	ns
t_{HCS}	CS[0:1] Hold Time to CCLK	2	—	ns
t_{SUWD}	Write Signal Setup Time to CCLK	7	—	ns
t_{HWD}	Write Signal Hold Time to CCLK	2	—	ns
t_{DCB}	CCLK to BUSY Delay Time	—	12	ns
t_{CORD}	Clock to Out for Read Data	—	12	ns
sysCONFIG Byte Slave Clocking				
t_{BSCH}	Byte Slave Clock Minimum High Pulse	6	—	ns
t_{BSCL}	Byte Slave Clock Minimum Low Pulse	8	—	ns
t_{BSCYC}	Byte Slave Clock Cycle Time	15	—	ns
sysCONFIG Serial (Bit) Data Flow				
t_{SUSCDI}	DI (Data In) Setup Time to CCLK	7	—	ns
t_{HSCDI}	DI (Data In) Hold Time to CCLK	2	—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	—	12	ns
sysCONFIG Serial Slave Clocking				
t_{SSCH}	Serial Slave Clock Minimum High Pulse	6	—	ns
t_{SSCL}	Serial Slave Clock Minimum Low Pulse	6	—	ns
sysCONFIG POR, Initialization and Wake Up				
t_{ICFG}	Minimum Vcc to INIT High	—	50	ms
t_{VMC}	Time from t_{ICFG} to Valid Master Clock	—	2	us
t_{PRGMRJ}	Program Pin Pulse Rejection	—	7	ns
t_{PRGM}[2]	PROGRAMN Low Time to Start Configuration	25	—	ns
t_{DINIT}	INIT Low Time	—	1	ms
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INIT Low	—	37	ns
t_{DINITD}	Delay Time from PROGRAMN Low to DONE Low	—	37	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low	—	25	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence	—	25	ns
t_{MWC}	Additional Wake Master Clock Signals after Done Pin High	120	—	cycles
Configuration Master Clock (CCLK)				
Frequency[1]		Selected Value - 30%	Selected Value + 30%	MHz
Duty Cycle		40	60	%

1. See Table 2-10 for available CCLK frequencies.
2. The threshold level for PROGRAMN, as well as for CFG[1] and CFG[0], is determined by V_{CC}, such that the threshold = $V_{CC}/2$.

Timing v.F0.11

Switching Test Conditions

Figure 3-13 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Figure 3-5.

Figure 3-13. Output Test Load, LVTTL and LVCMOS Standards

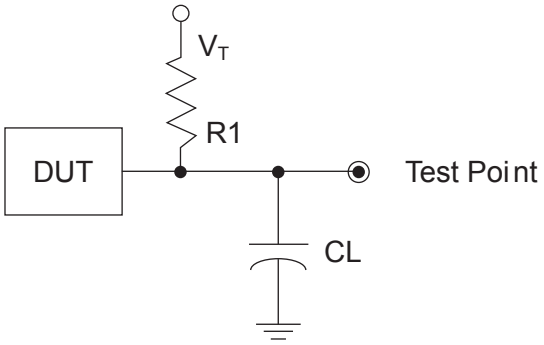


Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	0pF	LVCMOS 3.3 = 1.5V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	188	0pF	$V_{CCIO}/2$	V_{OL}
LVCMOS 2.5 I/O (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVCMOS 2.5 I/O (H -> Z)			V_{OH} - 0.15	V_{OL}
LVCMOS 2.5 I/O (L -> Z)			V_{OL} + 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions
Test and Programming (Dedicated pins. Pull-up is enabled on input pins during configuration.)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data in pin, used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence).
TDO	O	Output pin -Test Data out pin used to shift data out of device using 1149.1.
V_{CCJ}	—	V_{CCJ} - The power supply pin for JTAG Test Access Port.
Configuration Pads (used during sysCONFIG)		
CFG[1:0]	I	Mode pins used to specify configuration modes values latched on rising edge of INITN. During configuration, a pull-up is enabled.
INITN	I/O	Open Drain pin - Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. If CFG1 and CFG0 are high (SDM) then this pin is pulled low.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
DONE	I/O	Open Drain pin - Indicates that the configuration sequence is complete, and the startup sequence is in progress.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
BUSY	I/O	Generally not used. After configuration it is a user-programmable I/O pin.
CSN	I	sysCONFIG chip select (Active low). During configuration, a pull-up is enabled. After configuration it is user a programmable I/O pin.
CS1N	I	sysCONFIG chip select (Active Low). During configuration, a pull-up is enabled. After configuration it is user programmable I/O pin
WRITEN	I	Write Data on Parallel port (Active low). After configuration it is a user programmable I/O pin
D[7:0]	I/O	sysCONFIG Port Data I/O. After configuration these are user programmable I/O pins.
DOUT, CSON	O	Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port. After configuration, it is a user-programmable I/O pin.
DI	I	Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. After configuration it is a user-programmable I/O pin.
SLEEPN[2]	I	Sleep Mode pin - Active low sleep pin.þ When this pin is held high, the device operates normally.þ When driven low, the device moves into Sleep Mode after a specified time.This pin has a weak internal pull-up, but when not used an external pull-up to V_{CC} is recommended.
TOE[3]	I	Test Output Enable tri-states all I/O pins when driven low. This pin has a weak internal pull-up, but when not used an external pull-up to V_{CC} is recommended.

1. Applies toþ LFXP10, LFXP15 and LFXP20 only.
2. Applies to LFXP “C” devices only.
3. Applies to LFXP “E” devices only.

Pin Information Summary[1] (Cont.)

Pin Type		XP10		XP15			XP20		
		256 fpBGA	388 fpBGA	256 fpBGA	388 fpBGA	484 fpBGA	256 fpBGA	388 fpBGA	484 fpBGA
Single Ended User I/O		188	244	188	268	300	188	268	340
Differential Pair User I/O[2]		76	104	76	112	128	76	112	144
Configuration	Dedicated	11	11	11	11	11	11	11	11
	Muxed	14	14	14	14	14	14	14	14
TAP		5	5	5	5	5	5	5	5
Dedicated (total without supplies)		6	6	6	6	6	6	6	6
V_{CC}		8	14	8	14	28	8	14	28
V_{CCAUX}		4	4	4	4	12	4	4	12
V_{CCPLL}		2	2	2	2	2	2	2	2
V_{CCIO}	Bank0	2	5	2	5	4	2	5	4
	Bank1	2	5	2	5	4	2	5	4
	Bank2	2	4	2	4	4	2	4	4
	Bank3	2	4	2	4	4	2	4	4
	Bank4	2	5	2	5	4	2	5	4
	Bank5	2	5	2	5	4	2	5	4
	Bank6	2	4	2	4	4	2	4	4
	Bank7	2	4	2	4	4	2	4	4
GND		24	50	24	50	56	24	50	56
GND_{PLL}		2	2	2	2	2	2	2	2
NC		0	24	0	0	40	0	0	0
Single Ended/ Differential I/O per Bank[2]	Bank0	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank1	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank2	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank3	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank4	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank5	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank6	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank7	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
V_{CCJ}		1	1	1	1	1	1	1	1

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
2. The differential I/O per bank includes both dedicated LVDS and emulated LVDS pin pairs. Please see the Logic Signal Connections table for more information.

LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
139	PT6A	0	-	DI	PT9A	0	-	DI
140	PT5A	0	-	CSN	PT8A	0	-	CSN
141	PT3B	0	-	VREF2_0	PT6B	0	-	VREF2_0
142	CFG0	0	-	-	CFG0	0	-	-
143	CFG1	0	-	-	CFG1	0	-	-
144	DONE	0	-	-	DONE	0	-	-

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
1	CFG1	0	-	-	CFG1	0	-	-
2	DONE	0	-	-	DONE	0	-	-
3	PROGRAMN	7	-	-	PROGRAMN	7	-	-
4	CCLK	7	-	-	CCLK	7	-	-
5	GND	-	-	-	GND	-	-	-
6	PL2A	7	T[3]	-	PL2A	7	T[3]	-
7	GNDIO7	7	-	-	GNDIO7	7	-	-
8	PL2B	7	C[3]	-	PL2B	7	C[3]	-
9	PL3A	7	T	LUM0_PLLT_FB_A	PL3A	7	T	LUM0_PLLT_FB_A
10	PL3B	7	C	LUM0_PLLC_FB_A	PL3B	7	C	LUM0_PLLC_FB_A
11	PL4A	7	T[3]	-	PL4A	7	T[3]	-
12	PL4B	7	C[3]	-	PL4B	7	C[3]	-
13	VCCIO7	7	-	-	VCCIO7	7	-	-
14	PL5A	7	-	VREF1_7	PL5A	7	-	VREF1_7
15	PL6B	7	-	VREF2_7	PL6B	7	-	VREF2_7
16	GNDIO7	7	-	-	GNDIO7	7	-	-
17	PL7A	7	T[3]	DQS	PL7A	7	T[3]	DQS
18	PL7B	7	C[3]	-	PL7B	7	C[3]	-
19	VCC	-	-	-	VCC	-	-	-
20	PL8A	7	T	LUM0_PLLT_IN_A	PL8A	7	T	LUM0_PLLT_IN_A
21	PL8B	7	C	LUM0_PLLC_IN_A	PL8B	7	C	LUM0_PLLC_IN_A
22	PL9A	7	T[3]	-	PL9A	7	T[3]	-
23	VCCIO7	7	-	-	VCCIO7	7	-	-
24	PL9B	7	C[3]	-	PL9B	7	C[3]	-
25	VCCP0	-	-	-	VCCP0	-	-	-
26	GNDP0	-	-	-	GNDP0	-	-	-
27	NC	-	-	-	PL15B	6	-	-
28	VCCIO6	6	-	-	VCCIO6	6	-	-
29	PL11A	6	T[3]	-	PL16A	6	T[3]	-
30	PL11B	6	C[3]	-	PL16B	6	C[3]	-
31	PL12A	6	T	PCLKT6_0	PL17A	6	T	PCLKT6_0
32	PL12B	6	C	PCLKC6_0	PL17B	6	C	PCLKC6_0
33	NC	-	-	-	PL18A	6	T[3]	-
34	NC	-	-	-	PL18B	6	C[3]	-
35	VCC	-	-	-	VCC	-	-	-
36	PL13A	6	T[3]	-	PL21A	6	T[3]	-
37	PL13B	6	C[3]	-	PL21B	6	C[3]	-
38	GNDIO6	6	-	-	GNDIO6	6	-	-
39	PL14A	6	-	VREF1_6	PL22A	6	-	VREF1_6
40	PL15B	6	-	VREF2_6	PL23B	6	-	VREF2_6
41	VCCIO6	6	-	-	VCCIO6	6	-	-
42	PL16A	6	T[3]	DQS	PL24A	6	T[3]	DQS
43	PL16B	6	C[3]	-	PL24B	6	C[3]	-
44	PL17A	6	T	-	PL25A	6	T	-
45	PL17B	6	C	-	PL25B	6	C	-
46	PL18A	6	T[3]	-	PL26A	6	T[3]	-

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
139	PR7A	2	T[3]	DQS	PR7A	2	T[3]	DQS
140	VCCIO2	2	-	-	VCCIO2	2	-	-
141	PR6B	2	-	VREF1_2	PR6B	2	-	VREF1_2
142	PR5A	2	-	VREF2_2	PR5A	2	-	VREF2_2
143	GNDIO2	2	-	-	GNDIO2	2	-	-
144	PR4B	2	C[3]	-	PR4B	2	C[3]	-
145	PR4A	2	T[3]	-	PR4A	2	T[3]	-
146	PR3B	2	C	RUM0_PLLC_FB_A	PR3B	2	C	RUM0_PLLC_FB_A
147	PR3A	2	T	RUM0_PLLT_FB_A	PR3A	2	T	RUM0_PLLT_FB_A
148	PR2B	2	C[3]	-	PR2B	2	C[3]	-
149	VCCIO2	2	-	-	VCCIO2	2	-	-
150	PR2A	2	T[3]	-	PR2A	2	T[3]	-
151	VCC	-	-	-	VCC	-	-	-
152	VCCAUX	-	-	-	VCCAUX	-	-	-
153	TDO	-	-	-	TDO	-	-	-
154	VCCJ	-	-	-	VCCJ	-	-	-
155	TDI	-	-	-	TDI	-	-	-
156	TMS	-	-	-	TMS	-	-	-
157	TCK	-	-	-	TCK	-	-	-
158	VCC	-	-	-	VCC	-	-	-
159	PT25A	1	-	VREF1_1	PT28A	1	-	VREF1_1
160	PT24B	1	C	-	PT27B	1	C	-
161	PT24A	1	T	-	PT27A	1	T	-
162	PT23A	1	-	D0	PT26A	1	-	D0
163	GNDIO1	1	-	-	GNDIO1	1	-	-
164	PT22B	1	C	D1	PT25B	1	C	D1
165	PT22A	1	T	VREF2_1	PT25A	1	T	VREF2_1
166	PT21A	1	-	D2	PT24A	1	-	D2
167	VCCIO1	1	-	-	VCCIO1	1	-	-
168	PT20B	1	C	D3	PT23B	1	C	D3
169	PT20A	1	T	-	PT23A	1	T	-
170	PT19B	1	C	-	PT22B	1	C	-
171	PT19A	1	T	DQS	PT22A	1	T	DQS
172	GNDIO1	1	-	-	GNDIO1	1	-	-
173	PT18B	1	-	-	PT21B	1	-	-
174	PT17A	1	-	D4	PT20A	1	-	D4
175	PT16B	1	C	-	PT19B	1	C	-
176	PT16A	1	T	D5	PT19A	1	T	D5
177	VCCIO1	1	-	-	VCCIO1	1	-	-
178	PT15B	1	C	D6	PT18B	1	C	D6
179	PT15A	1	T	-	PT18A	1	T	-
180	PT14B	1	-	D7	PT17B	1	-	D7
181	GND	-	-	-	GND	-	-	-
182	VCC	-	-	-	VCC	-	-	-
183	PT13B	0	C	BUSY	PT16B	0	C	BUSY
184	GNDIO0	0	-	-	GNDIO0	0	-	-

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP6				LFXP10			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
K10	GND	-	-	-	GND	-	-	-
K7	GND	-	-	-	GND	-	-	-
K8	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-
L6	GND	-	-	-	GND	-	-	-
T1	GND	-	-	-	GND	-	-	-
T16	GND	-	-	-	GND	-	-	-
D13	VCC	-	-	-	VCC	-	-	-
D4	VCC	-	-	-	VCC	-	-	-
E12	VCC	-	-	-	VCC	-	-	-
E5	VCC	-	-	-	VCC	-	-	-
M12	VCC	-	-	-	VCC	-	-	-
M5	VCC	-	-	-	VCC	-	-	-
N13	VCC	-	-	-	VCC	-	-	-
N4	VCC	-	-	-	VCC	-	-	-
E13	VCCAUX	-	-	-	VCCAUX	-	-	-
E4	VCCAUX	-	-	-	VCCAUX	-	-	-
M13	VCCAUX	-	-	-	VCCAUX	-	-	-
M4	VCCAUX	-	-	-	VCCAUX	-	-	-
F7	VCCIO0	0	-	-	VCCIO0	0	-	-
F8	VCCIO0	0	-	-	VCCIO0	0	-	-
F10	VCCIO1	1	-	-	VCCIO1	1	-	-
F9	VCCIO1	1	-	-	VCCIO1	1	-	-
G11	VCCIO2	2	-	-	VCCIO2	2	-	-
H11	VCCIO2	2	-	-	VCCIO2	2	-	-
J11	VCCIO3	3	-	-	VCCIO3	3	-	-
K11	VCCIO3	3	-	-	VCCIO3	3	-	-
L10	VCCIO4	4	-	-	VCCIO4	4	-	-
L9	VCCIO4	4	-	-	VCCIO4	4	-	-
L7	VCCIO5	5	-	-	VCCIO5	5	-	-
L8	VCCIO5	5	-	-	VCCIO5	5	-	-
J6	VCCIO6	6	-	-	VCCIO6	6	-	-
K6	VCCIO6	6	-	-	VCCIO6	6	-	-
G6	VCCIO7	7	-	-	VCCIO7	7	-	-
H6	VCCIO7	7	-	-	VCCIO7	7	-	-

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
F4	PROGRAMN	7	-	-	PROGRAMN	7	-	-	PROGRAMN	7	-	-
G4	CCLK	7	-	-	CCLK	7	-	-	CCLK	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
D2	PL2A	7	T[3]	-	PL6A	7	T[3]	-	PL6A	7	T[3]	-
D1	PL2B	7	C[3]	-	PL6B	7	C[3]	-	PL6B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
E2	PL3A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A
E3	PL3B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A
F3	PL4A	7	T[3]	-	PL8A	7	T[3]	-	PL8A	7	T[3]	-
F2	PL4B	7	C[3]	-	PL8B	7	C[3]	-	PL8B	7	C[3]	-
H4	PL5A	7	-	-	PL9A	7	-	-	PL9A	7	-	-
H3	PL6B	7	-	VREF1_7	PL10B	7	-	VREF1_7	PL10B	7	-	VREF1_7
G3	PL7A	7	T[3]	DQS	PL11A	7	T[3]	DQS	PL11A	7	T[3]	DQS
G2	PL7B	7	C[3]	-	PL11B	7	C[3]	-	PL11B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
F1	PL8A	7	T	-	PL12A	7	T	-	PL12A	7	T	-
E1	PL8B	7	C	-	PL12B	7	C	-	PL12B	7	C	-
J4	PL9A	7	T[3]	-	PL13A	7	T[3]	-	PL13A	7	T[3]	-
K4	PL9B	7	C[3]	-	PL13B	7	C[3]	-	PL13B	7	C[3]	-
G1	PL11A	7	T[3]	-	PL15A	7	T[3]	-	PL15A	7	T[3]	-
H2	PL11B	7	C[3]	-	PL15B	7	C[3]	-	PL15B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
J2	PL12A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A
H1	PL12B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A
J1	PL13A	7	T[3]	-	PL17A	7	T[3]	-	PL17A	7	T[3]	-
K2	PL13B	7	C[3]	-	PL17B	7	C[3]	-	PL17B	7	C[3]	-
K3	PL14A	7	-	VREF2_7	PL18A	7	-	VREF2_7	PL18A	7	-	VREF2_7
J3	PL15B	7	-	-	PL19B	7	-	-	PL19B	7	-	-
K1	PL16A	7	T[3]	DQS	PL20A	7	T[3]	DQS	PL20A	7	T[3]	DQS
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
L2	PL16B	7	C[3]	-	PL20B	7	C[3]	-	PL20B	7	C[3]	-
L3	PL17A	7	T	-	PL21A	7	T	-	PL21A	7	T	-
L4	PL17B	7	C	-	PL21B	7	C	-	PL21B	7	C	-
L1	PL18A	7	T[3]	-	PL22A	7	T[3]	-	PL22A	7	T[3]	-
M1	PL18B	7	C[3]	-	PL22B	7	C[3]	-	PL22B	7	C[3]	-
M2	VCCP0	-	-	-	VCCP0	-	-	-	VCCP0	-	-	-
N1	GNDP0	-	-	-	GNDP0	-	-	-	GNDP0	-	-	-
M3	PL19A	6	T[3]	-	PL23A	6	T[3]	-	PL27A	6	T[3]	-
M4	PL19B	6	C[3]	-	PL23B	6	C[3]	-	PL27B	6	C[3]	-
P1	PL20A	6	T	PCLKT6_0	PL24A	6	T	PCLKT6_0	PL28A	6	T	PCLKT6_0
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
N2	PL20B	6	C	PCLKC6_0	PL24B	6	C	PCLKC6_0	PL28B	6	C	PCLKC6_0
R1	PL21A	6	T[3]	-	PL25A	6	T[3]	-	PL29A	6	T[3]	-
P2	PL21B	6	C[3]	-	PL25B	6	C[3]	-	PL29B	6	C[3]	-
N3	PL22A	6	-	-	PL26A	6	-	-	PL30A	6	-	-
N4	PL23B	6	-	VREF1_6	PL27B	6	-	VREF1_6	PL31B	6	-	VREF1_6
T1	PL24A	6	T[3]	DQS	PL28A	6	T[3]	DQS	PL32A	6	T[3]	DQS
R2	PL24B	6	C[3]	-	PL28B	6	C[3]	-	PL32B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
U1	PL25A	6	T	LLM0_PLLT_IN_A	PL29A	6	T	LLM0_PLLT_IN_A	PL33A	6	T	LLM0_PLLT_IN_A
T2	PL25B	6	C	LLM0_PLLC_IN_A	PL29B	6	C	LLM0_PLLC_IN_A	PL33B	6	C	LLM0_PLLC_IN_A
V1	PL26A	6	T[3]	-	PL30A	6	T[3]	-	PL34A	6	T[3]	-
U2	PL26B	6	C[3]	-	PL30B	6	C[3]	-	PL34B	6	C[3]	-
W1	PL28A	6	T[3]	-	PL32A	6	T[3]	-	PL36A	6	T[3]	-
V2	PL28B	6	C[3]	-	PL32B	6	C[3]	-	PL36B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	-	-	-	GNDIO6	6	-	-
P3	PL29A	6	T	-	PL33A	6	T	-	PL37A	6	T	-
P4	PL29B	6	C	-	PL33B	6	C	-	PL37B	6	C	-
Y1	PL30A	6	T[3]	-	PL34A	6	T[3]	-	PL38A	6	T[3]	-
W2	PL30B	6	C[3]	-	PL34B	6	C[3]	-	PL38B	6	C[3]	-
R3	PL31A	6	-	VREF2_6	PL35A	6	-	VREF2_6	PL39A	6	-	VREF2_6
R4	PL32B	6	-	-	PL36B	6	-	-	PL40B	6	-	-
T3	PL33A	6	T[3]	DQS	PL37A	6	T[3]	DQS	PL41A	6	T[3]	DQS
T4	PL33B	6	C[3]	-	PL37B	6	C[3]	-	PL41B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
V4	PL34A	6	T	LLM0_PLLT_FB_A	PL38A	6	T	LLM0_PLLT_FB_A	PL42A	6	T	LLM0_PLLT_FB_A
V3	PL34B	6	C	LLM0_PLLC_FB_A	PL38B	6	C	LLM0_PLLC_FB_A	PL42B	6	C	LLM0_PLLC_FB_A
U4	PL35A	6	T[3]	-	PL39A	6	T[3]	-	PL43A	6	T[3]	-
U3	PL35B	6	C[3]	-	PL39B	6	C[3]	-	PL43B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
W5	SLEEPN[1]/ TOE[2]	-	-	-	SLEEPN[1]/ TOE[2]	-	-	-	SLEEPN[1]/ TOE[2]	-	-	-
Y2	INITN	5	-	-	INITN	5	-	-	INITN	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y3	-	-	-	-	PB3B	5	-	-	PB7B	5	-	-
W3	-	-	-	-	PB4A	5	T	-	PB8A	5	T	-
W4	-	-	-	-	PB4B	5	C	-	PB8B	5	C	-
AA2	-	-	-	-	PB5A	5	-	-	PB9A	5	-	-
AA1	-	-	-	-	PB6B	5	-	-	PB10B	5	-	-
W6	PB2A	5	-	-	PB7A	5	T	DQS	PB11A	5	T	DQS
W7	-	-	-	-	PB7B	5	C	-	PB11B	5	C	-
Y4	PB3A	5	T	-	PB8A	5	T	-	PB12A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y5	PB3B	5	C	-	PB8B	5	C	-	PB12B	5	C	-
AB2	PB4A	5	T	-	PB9A	5	T	-	PB13A	5	T	-
AA3	PB4B	5	C	-	PB9B	5	C	-	PB13B	5	C	-
AB3	PB5A	5	T	-	PB10A	5	T	-	PB14A	5	T	-
AA4	PB5B	5	C	-	PB10B	5	C	-	PB14B	5	C	-
W8	PB6A	5	T	-	PB11A	5	T	-	PB15A	5	T	-
W9	PB6B	5	C	-	PB11B	5	C	-	PB15B	5	C	-
AB4	PB7A	5	T	VREF1_5	PB12A	5	T	VREF1_5	PB16A	5	T	VREF1_5
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
AA5	PB7B	5	C	-	PB12B	5	C	-	PB16B	5	C	-
AB5	PB8A	5	-	-	PB13A	5	-	-	PB17A	5	-	-
Y6	PB9B	5	-	-	PB14B	5	-	-	PB18B	5	-	-
AA6	PB10A	5	T	DQS	PB15A	5	T	DQS	PB19A	5	T	DQS
AB6	PB10B	5	C	-	PB15B	5	C	-	PB19B	5	C	-
Y9	PB11A	5	T	-	PB16A	5	T	-	PB20A	5	T	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
AA20	PB36B	4	C	-	PB41B	4	C	-	PB45B	4	C	-
AB21	PB37A	4	T	-	PB42A	4	T	-	PB46A	4	T	-
AA21	PB37B	4	C	-	PB42B	4	C	-	PB46B	4	C	-
AA22	PB38A	4	T	-	PB43A	4	T	-	PB47A	4	T	-
Y21	PB38B	4	C	-	PB43B	4	C	-	PB47B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
W16	PB39A	4	-	-	PB44A	4	T	-	PB48A	4	T	-
W17	-	-	-	-	PB44B	4	C	-	PB48B	4	C	-
Y15	-	-	-	-	PB45A	4	-	-	PB49A	4	-	-
Y16	-	-	-	-	PB46B	4	-	-	PB50B	4	-	-
W19	-	-	-	-	PB47A	4	T	DQS	PB51A	4	T	DQS
W18	-	-	-	-	PB47B	4	C	-	PB51B	4	C	-
W20	-	-	-	-	PB48A	4	-	-	PB52A	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
T20	PR35B	3	C[3]	-	PR39B	3	C[3]	-	PR43B	3	C[3]	-
T19	PR35A	3	T[3]	-	PR39A	3	T[3]	-	PR43A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
U19	PR34B	3	C	RLM0_PLLC_FB_A	PR38B	3	C	RLM0_PLLC_FB_A	PR42B	3	C	RLM0_PLLC_FB_A
U20	PR34A	3	T	RLM0_PLLT_FB_A	PR38A	3	T	RLM0_PLLT_FB_A	PR42A	3	T	RLM0_PLLT_FB_A
V19	PR33B	3	C[3]	-	PR37B	3	C[3]	-	PR41B	3	C[3]	-
V20	PR33A	3	T[3]	DQS	PR37A	3	T[3]	DQS	PR41A	3	T[3]	DQS
R19	PR32B	3	-	-	PR36B	3	-	-	PR40B	3	-	-
R20	PR31A	3	-	VREF1_3	PR35A	3	-	VREF1_3	PR39A	3	-	VREF1_3
W21	PR30B	3	C[3]	-	PR34B	3	C[3]	-	PR38B	3	C[3]	-
Y22	PR30A	3	T[3]	-	PR34A	3	T[3]	-	PR38A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
P19	PR29B	3	C	-	PR33B	3	C	-	PR37B	3	C	-
P20	PR29A	3	T	-	PR33A	3	T	-	PR37A	3	T	-
V21	PR28B	3	C[3]	-	PR32B	3	C[3]	-	PR36B	3	C[3]	-
W22	PR28A	3	T[3]	-	PR32A	3	T[3]	-	PR36A	3	T[3]	-
U21	PR26B	3	C[3]	-	PR30B	3	C[3]	-	PR34B	3	C[3]	-
V22	PR26A	3	T[3]	-	PR30A	3	T[3]	-	PR34A	3	T[3]	-
T21	PR25B	3	C	RLM0_PLLC_IN_A	PR29B	3	C	RLM0_PLLC_IN_A	PR33B	3	C	RLM0_PLLC_IN_A
U22	PR25A	3	T	RLM0_PLLT_IN_A	PR29A	3	T	RLM0_PLLT_IN_A	PR33A	3	T	RLM0_PLLT_IN_A
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
R21	PR24B	3	C[3]	-	PR28B	3	C[3]	-	PR32B	3	C[3]	-
T22	PR24A	3	T[3]	DQS	PR28A	3	T[3]	DQS	PR32A	3	T[3]	DQS
N19	PR23B	3	-	-	PR27B	3	-	-	PR31B	3	-	-
N20	PR22A	3	-	VREF2_3	PR26A	3	-	VREF2_3	PR30A	3	-	VREF2_3
R22	PR21B	3	C[3]	-	PR25B	3	C[3]	-	PR29B	3	C[3]	-
P22	PR21A	3	T[3]	-	PR25A	3	T[3]	-	PR29A	3	T[3]	-
P21	PR20B	3	C	-	PR24B	3	C	-	PR28B	3	C	-
N21	PR20A	3	T	-	PR24A	3	T	-	PR28A	3	T	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
M20	PR19B	3	C[3]	-	PR23B	3	C[3]	-	PR27B	3	C[3]	-
M19	PR19A	3	T[3]	-	PR23A	3	T[3]	-	PR27A	3	T[3]	-
N22	GNDP1	-	-	-	GNDP1	-	-	-	GNDP1	-	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
G9	VCC	-	-	-	VCC	-	-	-
H15	VCC	-	-	-	VCC	-	-	-
H8	VCC	-	-	-	VCC	-	-	-
J16	VCC	-	-	-	VCC	-	-	-
J7	VCC	-	-	-	VCC	-	-	-
K16	VCC	-	-	-	VCC	-	-	-
K17	VCC	-	-	-	VCC	-	-	-
K6	VCC	-	-	-	VCC	-	-	-
K7	VCC	-	-	-	VCC	-	-	-
N16	VCC	-	-	-	VCC	-	-	-
N17	VCC	-	-	-	VCC	-	-	-
N6	VCC	-	-	-	VCC	-	-	-
N7	VCC	-	-	-	VCC	-	-	-
P16	VCC	-	-	-	VCC	-	-	-
P7	VCC	-	-	-	VCC	-	-	-
R15	VCC	-	-	-	VCC	-	-	-
R8	VCC	-	-	-	VCC	-	-	-
T10	VCC	-	-	-	VCC	-	-	-
T13	VCC	-	-	-	VCC	-	-	-
T14	VCC	-	-	-	VCC	-	-	-
T9	VCC	-	-	-	VCC	-	-	-
U10	VCC	-	-	-	VCC	-	-	-
U13	VCC	-	-	-	VCC	-	-	-
G15	VCCAUX	-	-	-	VCCAUX	-	-	-
G16	VCCAUX	-	-	-	VCCAUX	-	-	-
G7	VCCAUX	-	-	-	VCCAUX	-	-	-
G8	VCCAUX	-	-	-	VCCAUX	-	-	-
H16	VCCAUX	-	-	-	VCCAUX	-	-	-
H7	VCCAUX	-	-	-	VCCAUX	-	-	-
R16	VCCAUX	-	-	-	VCCAUX	-	-	-
R7	VCCAUX	-	-	-	VCCAUX	-	-	-
T15	VCCAUX	-	-	-	VCCAUX	-	-	-
T16	VCCAUX	-	-	-	VCCAUX	-	-	-
T7	VCCAUX	-	-	-	VCCAUX	-	-	-
T8	VCCAUX	-	-	-	VCCAUX	-	-	-
F11	VCCIO0	0	-	-	VCCIO0	0	-	-
G11	VCCIO0	0	-	-	VCCIO0	0	-	-
H10	VCCIO0	0	-	-	VCCIO0	0	-	-
H11	VCCIO0	0	-	-	VCCIO0	0	-	-
F12	VCCIO1	1	-	-	VCCIO1	1	-	-
G12	VCCIO1	1	-	-	VCCIO1	1	-	-
H12	VCCIO1	1	-	-	VCCIO1	1	-	-

Commercial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15C-3F484C	300	1.8/2.5/3.3V	-3	fpBGA	484	COM	15.5K
LFXP15C-4F484C	300	1.8/2.5/3.3V	-4	fpBGA	484	COM	15.5K
LFXP15C-5F484C	300	1.8/2.5/3.3V	-5	fpBGA	484	COM	15.5K
LFXP15C-3F388C	268	1.8/2.5/3.3V	-3	fpBGA	388	COM	15.5K
LFXP15C-4F388C	268	1.8/2.5/3.3V	-4	fpBGA	388	COM	15.5K
LFXP15C-5F388C	268	1.8/2.5/3.3V	-5	fpBGA	388	COM	15.5K
LFXP15C-3F256C	188	1.8/2.5/3.3V	-3	fpBGA	256	COM	15.5K
LFXP15C-4F256C	188	1.8/2.5/3.3V	-4	fpBGA	256	COM	15.5K
LFXP15C-5F256C	188	1.8/2.5/3.3V	-5	fpBGA	256	COM	15.5K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20C-3F484C	340	1.8/2.5/3.3V	-3	fpBGA	484	COM	19.7K
LFXP20C-4F484C	340	1.8/2.5/3.3V	-4	fpBGA	484	COM	19.7K
LFXP20C-5F484C	340	1.8/2.5/3.3V	-5	fpBGA	484	COM	19.7K
LFXP20C-3F388C	268	1.8/2.5/3.3V	-3	fpBGA	388	COM	19.7K
LFXP20C-4F388C	268	1.8/2.5/3.3V	-4	fpBGA	388	COM	19.7K
LFXP20C-5F388C	268	1.8/2.5/3.3V	-5	fpBGA	388	COM	19.7K
LFXP20C-3F256C	188	1.8/2.5/3.3V	-3	fpBGA	256	COM	19.7K
LFXP20C-4F256C	188	1.8/2.5/3.3V	-4	fpBGA	256	COM	19.7K
LFXP20C-5F256C	188	1.8/2.5/3.3V	-5	fpBGA	256	COM	19.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3E-3Q208C	136	1.2V	-3	PQFP	208	COM	3.1K
LFXP3E-4Q208C	136	1.2V	-4	PQFP	208	COM	3.1K
LFXP3E-5Q208C	136	1.2V	-5	PQFP	208	COM	3.1K
LFXP3E-3T144C	100	1.2V	-3	TQFP	144	COM	3.1K
LFXP3E-4T144C	100	1.2V	-4	TQFP	144	COM	3.1K
LFXP3E-5T144C	100	1.2V	-5	TQFP	144	COM	3.1K
LFXP3E-3T100C	62	1.2V	-3	TQFP	100	COM	3.1K
LFXP3E-4T100C	62	1.2V	-4	TQFP	100	COM	3.1K
LFXP3E-5T100C	62	1.2V	-5	TQFP	100	COM	3.1K

Industrial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15C-3F484I	300	1.8/2.5/3.3V	-3	fpBGA	484	IND	15.5K
LFXP15C-4F484I	300	1.8/2.5/3.3V	-4	fpBGA	484	IND	15.5K
LFXP15C-3F388I	268	1.8/2.5/3.3V	-3	fpBGA	388	IND	15.5K
LFXP15C-4F388I	268	1.8/2.5/3.3V	-4	fpBGA	388	IND	15.5K
LFXP15C-3F256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	15.5K
LFXP15C-4F256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	15.5K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20C-3F484I	340	1.8/2.5/3.3V	-3	fpBGA	484	IND	19.7K
LFXP20C-4F484I	340	1.8/2.5/3.3V	-4	fpBGA	484	IND	19.7K
LFXP20C-3F388I	268	1.8/2.5/3.3V	-3	fpBGA	388	IND	19.7K
LFXP20C-4F388I	268	1.8/2.5/3.3V	-4	fpBGA	388	IND	19.7K
LFXP20C-3F256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	19.7K
LFXP20C-4F256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	19.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3E-3Q208I	136	1.2V	-3	PQFP	208	IND	3.1K
LFXP3E-4Q208I	136	1.2V	-4	PQFP	208	IND	3.1K
LFXP3E-3T144I	100	1.2V	-3	TQFP	144	IND	3.1K
LFXP3E-4T144I	100	1.2V	-4	TQFP	144	IND	3.1K
LFXP3E-3T100I	62	1.2V	-3	TQFP	100	IND	3.1K
LFXP3E-4T100I	62	1.2V	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6E-3F256I	188	1.2V	-3	fpBGA	256	IND	5.8K
LFXP6E-4F256I	188	1.2V	-4	fpBGA	256	IND	5.8K
LFXP6E-3Q208I	142	1.2V	-3	PQFP	208	IND	5.8K
LFXP6E-4Q208I	142	1.2V	-4	PQFP	208	IND	5.8K
LFXP6E-3T144I	100	1.2V	-3	TQFP	144	IND	5.8K
LFXP6E-4T144I	100	1.2V	-4	TQFP	144	IND	5.8K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10E-3F388I	244	1.2V	-3	fpBGA	388	IND	9.7K
LFXP10E-4F388I	244	1.2V	-4	fpBGA	388	IND	9.7K
LFXP10E-3F256I	188	1.2V	-3	fpBGA	256	IND	9.7K
LFXP10E-4F256I	188	1.2V	-4	fpBGA	256	IND	9.7K