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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	20000
Total RAM Bits	405504
Number of I/O	268
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	388-BBGA
Supplier Device Package	388-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp20e-5fn388c

Table 2-4. PFU Modes of Operation

Logic	Ripple	RAM[1]	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR16x2 x 4 DPR16x2 x 2	ROM16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR16x4 x 2 DPR16x4 x 1	ROM16x2 x 4
LUT 6x 2 or MUX 8x1 x 2	2-bit Counter x 4	SPR16x8 x 1	ROM16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM16x8 x 1

1. These modes are not available in PFF blocks

Routing

There are many resources provided in the LatticeXP devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal, vertical and diagonal directions. The x2 and x6 resources are buffered allowing both short and long connections routing between PFUs.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

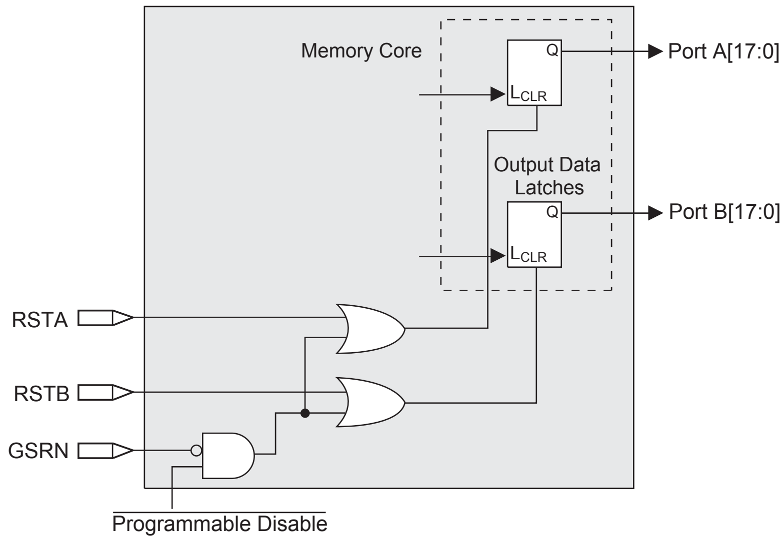
Clock Distribution Network

The clock inputs are selected from external I/O, the sysCLOCK™ PLLs or routing. These clock inputs are fed through the chip via a clock distribution system.

Primary Clock Sources

LatticeXP devices derive clocks from three primary sources: PLL outputs, dedicated clock inputs and routing. LatticeXP devices have two to four sysCLOCK PLLs, located on the left and right sides of the device. There are four dedicated clock inputs, one on each side of the device. Figure 2-5 shows the 20 primary clock sources.

Figure 2-15. Memory Core Reset

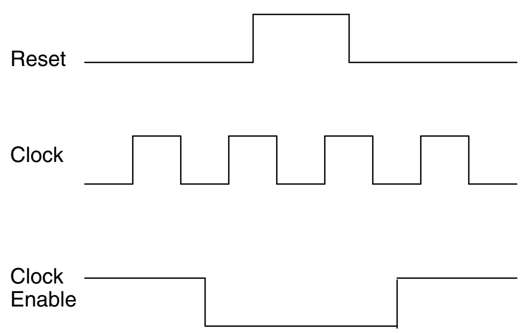


For further information on sysMEM EBR block, see the details of additional technical documentation at the end of this data sheet.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-16. The GSR input to the EBR is always asynchronous.

Figure 2-16. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

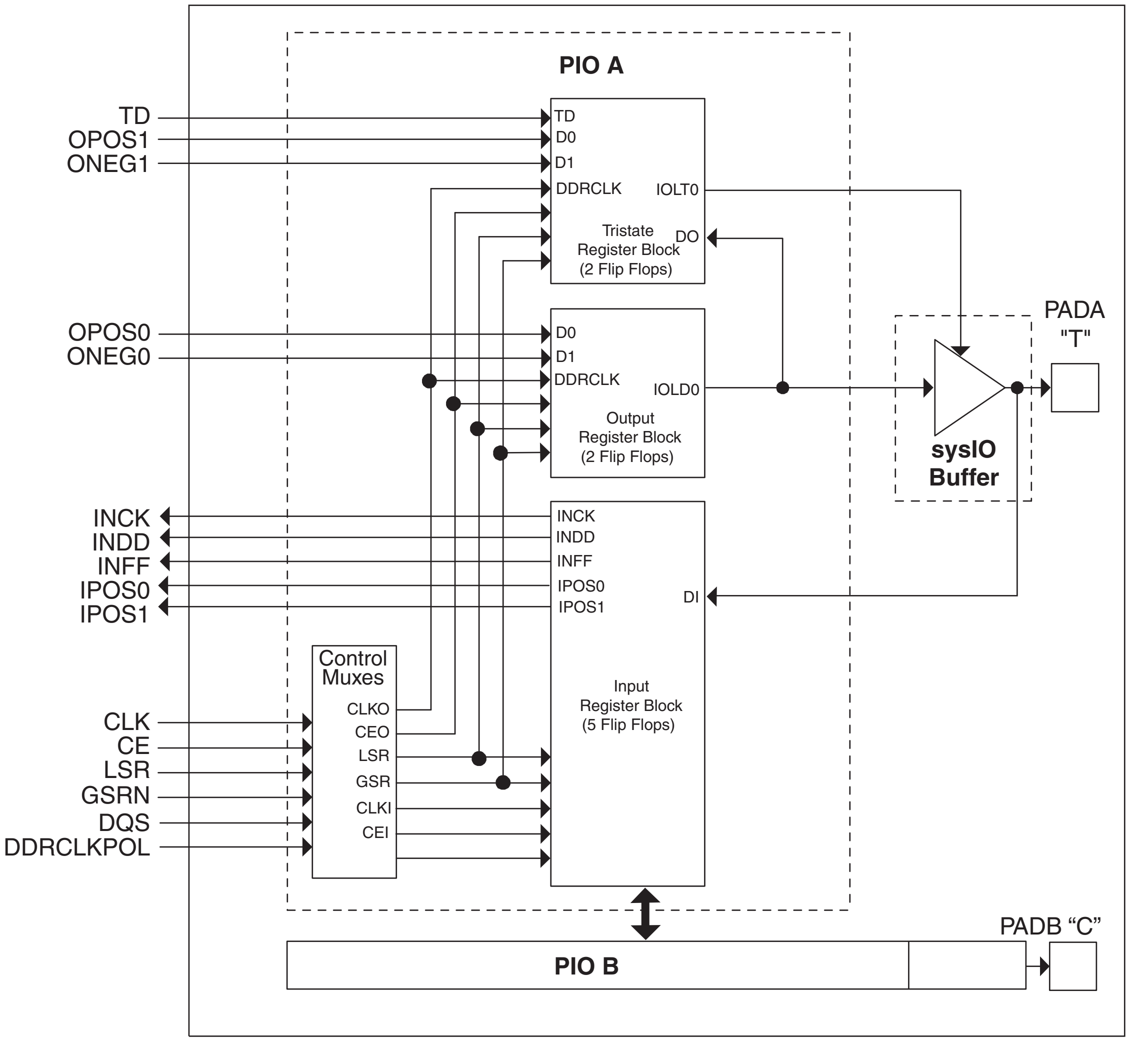
These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

Programmable I/O Cells (PICs)

Each PIC contains two PIOs connected to their respective sysIO Buffers which are then connected to the PADs as shown in Figure 2-17. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to sysIO buffer, and receives input from the buffer.

Figure 2-17. PIC Diagram



In the LatticeXP family, seven PIOs or four (3.5) PICs are grouped together to provide two LVDS differential pairs, one PIC pair and one single I/O, as shown in Figure 2-18.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as "T" and "C"). The PAD Labels "T" and "C" distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 14 PIOs (a group of 8 PICs) contains a delay element to facilitate the generation of DQS signals as shown in Figure 2-19. The DQS signal feeds the DQS bus which spans the set of 13 PIOs (8 PICs). The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table in this data sheet.

Table 2-9. Characteristics of Normal, Off and Sleep Modes

Characteristic	Normal	Off	Sleep
SLEEPN Pin	High	—	Low
Static Icc	Typical <100mA	0	Typical <100uA
I/O Leakage	<10µA	<1mA	<10µA
Power Supplies VCC/VCCIO/VCCAUX	Normal Range	Off	Normal Range
Logic Operation	User Defined	Non Operational	Non operational
I/O Operation	User Defined	Tri-state	Tri-state
JTAG and Programming circuitry	Operational	Non-operational	Non-operational
EBR Contents and Registers	Maintained	Non-maintained	Non-maintained

SLEEPN Pin Characteristics

The SLEEPN pin behaves as an LVCMOS input with the voltage standard appropriate to the VCC supply for the device. This pin also has a weak pull-up typically in the order of 10µA along with a Schmidt trigger and glitch filter to prevent false triggering. An external pull-up to V_{CC} is recommended when Sleep Mode is not used to ensure the device stays in normal operation mode. Typically the device enters Sleep Mode several hundred ns after SLEEPN is held at a valid low and restarts normal operation as specified in the Sleep Mode Timing table. The AC and DC specifications portion of this data sheet show a detailed timing diagram.

Configuration and Testing

The following section describes the configuration and testing features of the LatticeXP family of devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeXP devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

Device Configuration

All LatticeXP devices contain two possible ports that can be used for device configuration and programming. The test access port (TAP), which supports serial configuration, and the sysCONFIG port that supports both byte-wide and serial configuration.

The non-volatile memory in the LatticeXP can be configured in three different modes:

- In sysCONFIG mode via the sysCONFIG port. Note this can also be done in background mode.
- In 1532 mode via the 1149.1 port.
- In background mode via the 1149.1 port. This allows the device to be operated while reprogramming takes place.

The SRAM configuration memory can be configured in three different ways:

- At power-up via the on-chip non-volatile memory.
- In 1532 mode via the 1149.1 port SRAM direct configuration.
- In sysCONFIG mode via the sysCONFIG port SRAM direct configuration.

Figure 2-29 provides a pictorial representation of the different programming ports and modes available in the LatticeXP devices.

On power-up, the FPGA SRAM is ready to be configured with the sysCONFIG port active. The IEEE 1149.1 serial mode can be activated any time after power-up by sending the appropriate command through the TAP port.

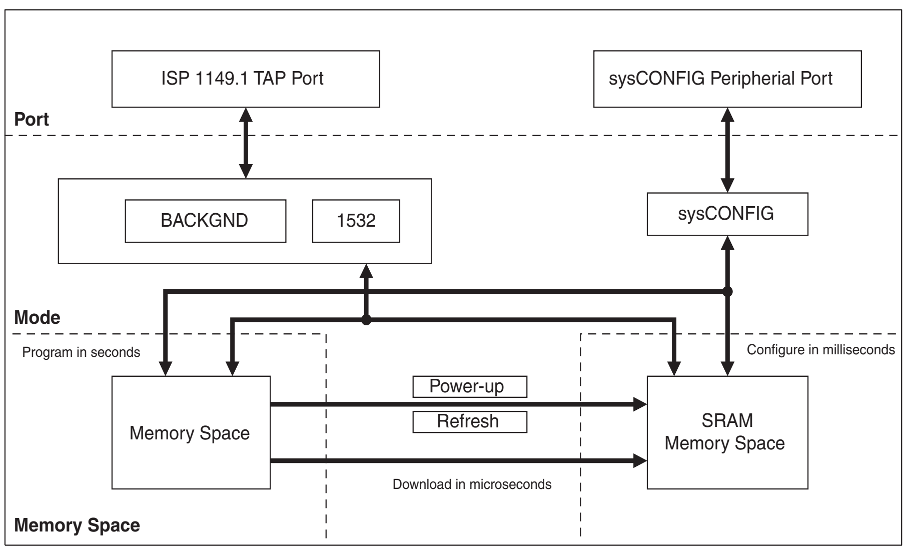
Leave Alone I/O
When using 1532 mode for non-volatile memory programming, users may specify I/Os as high, low, tristated or held at current value. This provides excellent flexibility for implementing systems where reprogramming occurs on-the-fly.

TransFR (Transparent Field Reconfiguration)
TransFR (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. See Lattice technical note #TN1087, *Minimizing System Interruption During Configuration Using TransFR Technology,* for details.

Security
The LatticeXP devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile memory spaces. Once set, the only way to clear security bits is to erase the memory space.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

Figure 2-29. ispXP Block Diagram



Internal Logic Analyzer Capability (ispTRACY)

All LatticeXP devices support an internal logic analyzer diagnostic feature. The diagnostic features provide capabilities similar to an external logic analyzer, such as programmable event and trigger condition and deep trace memory. This feature is enabled by Lattice's ispTRACY. The ispTRACY utility is added into the user design at compile time.

For more information on ispTRACY, please see information regarding additional technical documentation at the end of this data sheet.

Oscillator

Every LatticeXP device has an internal CMOS oscillator which is used to derive a master serial clock for configuration. The oscillator and the master serial clock run continuously in the configuration mode. The default value of the

Typical Building Block Function Performance[1]

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	-5 Timing	Units
Basic Functions		
16-bit decoder	6.1	ns
32-bit decoder	7.3	ns
64-bit decoder	8.2	ns
4:1 MUX	4.9	ns
8:1 MUX	5.3	ns
16:1 MUX	5.7	ns
32:1 MUX	6.3	ns

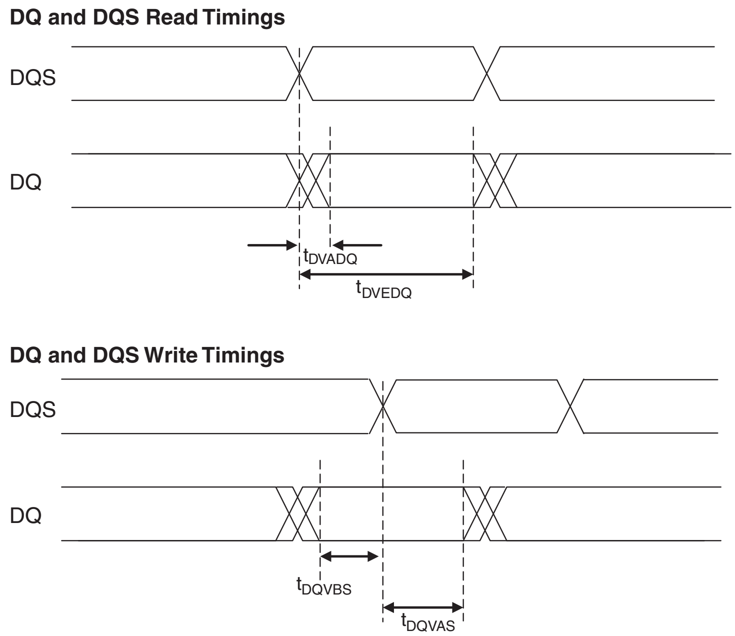
Register to Register Performance

Function	-5 Timing	Units
Basic Functions		
16-bit decoder	351	MHz
32-bit decoder	248	MHz
64-bit decoder	237	MHz
4:1 MUX	590	MHz
8:1 MUX	523	MHz
16:1 MUX	434	MHz
32:1 MUX	355	MHz
8-bit adder	343	MHz
16-bit adder	292	MHz
64-bit adder	130	MHz
16-bit counter	388	MHz
32-bit counter	295	MHz
64-bit counter	200	MHz
64-bit accumulator	164	MHz
Embedded Memory Functions		
Single Port RAM 256x36 bits	254	MHz
True-Dual Port RAM 512x18 bits	254	MHz
Distributed Memory Functions		
16x2 SP RAM	434	MHz
64x2 SP RAM	332	MHz
128x4 SP RAM	235	MHz
32x2 PDP RAM	322	MHz
64x4 PDP RAM	291	MHz

1. These timing numbers were generated using the ispLEVER design tool. Exact performance may vary with design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Timing v.F0.11

Figure 3-5. DDR Timings



LatticeXP Internal Timing Parameters[1] (Continued)

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register	—	1.61	—	1.94	—	2.32	ns
PLL Parameters								
t_{RSTREC}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
t_{RSTSU}	Reset Signal Setup Time	1.00	—	1.00	—	1.00	—	ns

1. Internal parameters are characterized but not tested on every device.

Timing v.F0.11

Switching Test Conditions

Figure 3-13 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Figure 3-5.

Figure 3-13. Output Test Load, LVTTL and LVCMOS Standards

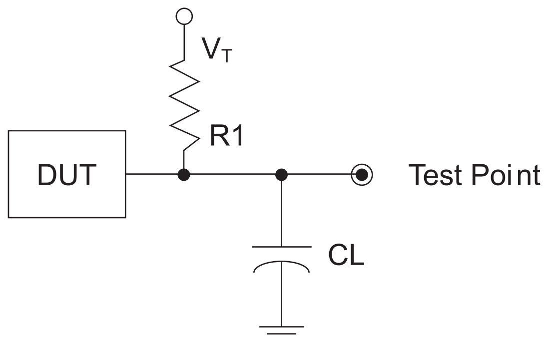


Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces

<table>
<tr><th>Test Condition</th><th>R_1</th><th>C_L</th><th>Timing Ref.</th><th>V_T</th></tr>
<tr><td rowspan="5">LVTTL and other LVCMOS settings (L -> H, H -> L)</td><td rowspan="5">∞</td><td rowspan="5">0pF</td><td>LVCMOS 3.3 = 1.5V</td><td>—</td></tr>
<tr><td>LVCMOS 2.5 = $V_{CCIO}/2$</td><td>—</td></tr>
<tr><td>LVCMOS 1.8 = $V_{CCIO}/2$</td><td>—</td></tr>
<tr><td>LVCMOS 1.5 = $V_{CCIO}/2$</td><td>—</td></tr>
<tr><td>LVCMOS 1.2 = $V_{CCIO}/2$</td><td>—</td></tr>
<tr><td>LVCMOS 2.5 I/O (Z -> H)</td><td rowspan="4">188</td><td rowspan="4">0pF</td><td>$V_{CCIO}/2$</td><td>V_{OL}</td></tr>
<tr><td>LVCMOS 2.5 I/O (Z -> L)</td><td>$V_{CCIO}/2$</td><td>V_{OH}</td></tr>
<tr><td>LVCMOS 2.5 I/O (H -> Z)</td><td>V_{OH} - 0.15</td><td>V_{OL}</td></tr>
<tr><td>LVCMOS 2.5 I/O (L -> Z)</td><td>V_{OL} + 0.15</td><td>V_{OH}</td></tr>
</table>

Note: Output test conditions for all other interfaces are determined by the respective standards.

LatticeXP Family Data Sheet Pinout Information

Lattice Semiconductor Corporation

November 2007 | Data Sheet DS1001

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
P[Edge] [Row/Column Number*]_[A/B]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic. During configuration, the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
GSRN	I	Global RESET signal. (Active low). Any I/O pin can be configured to be GSRN.
NC	—	No connect.
GND	—	GND - Ground. Dedicated Pins.
V_{CC}	—	VCC - The power supply pins for core logic. Dedicated Pins.
V_{CCAUX}	—	V_{CCAUX} - The Auxiliary power supply pin. It powers all the differential and referenced input buffers. Dedicated Pins.
V_{CCP0}	—	Voltage supply pins for ULM0PLL (and LLM1PLL[1]).
V_{CCP1}	—	Voltage supply pins for URM0PLL (and LRM1PLL[1]).
GNDP0	—	Ground pins for ULM0PLL (and LLM1PLL[1]).
GNDP1	—	Ground pins for URM0PLL (and LRM1PLL[1]).
V_{CCIOx}	—	V_{CCIO} - The power supply pins for I/O bank x. Dedicated Pins.
$V_{REF1(x)}$, $V_{REF2(x)}$	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V_{REF} inputs. When not used, they may be used as I/O pins.
PLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_PLL[T, C]_IN_A	—	Reference clock (PLL) input Pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A, B, C...at each side.
[LOC][num]_PLL[T, C]_FB_A	—	Optional feedback (PLL) input Pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A, B, C...at each side.
PCLK[T, C]_[n:0]_[3:0]	—	Primary Clock Pads, T = true and C = complement, n per side, indexed by bank and 0,1, 2, 3 within bank.
[LOC]DQS[num]	—	DQS input Pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = Ball function number. Any pad can be configured to be DQS output.

LFXP3 Logic Signal Connections: 100 TQFP

Pin Number	Pin Function	Bank	Differential	Dual Function
1	CFG1	0	-	-
2	DONE	0	-	-
3	PROGRAMN	7	-	-
4	CCLK	7	-	-
5	PL3A	7	T	LUM0_PLLT_FB_A
6	PL3B	7	C	LUM0_PLLC_FB_A
7	VCCIO7	7	-	-
8	PL5A	7	-	VREF1_7
9	PL6B	7	-	VREF2_7
10	GNDIO7	7	-	-
11	PL7A	7	T[3]	DQS
12	PL7B	7	C[3]	-
13	PL8A	7	T	LUM0_PLLT_IN_A
14	PL8B	7	C	LUM0_PLLC_IN_A
15	PL9A	7	T[3]	-
16	PL9B	7	C[3]	-
17	VCCP0	-	-	-
18	GNDP0	-	-	-
19	PL12A	6	T	PCLKT6_0
20	PL12B	6	C	PCLKC6_0
21	GNDIO6	6	-	-
22	VCCIO6	6	-	-
23	PL18A	6	T[3]	-
24	PL18B	6	C[3]	-
25	VCCAUX	-	-	-
26	SLEEPN[1]/TOE[2]	-	-	-
27	INITN	5	-	-
28	VCC	-	-	-
29	PB2B	5	-	VREF1_5
30	PB5B	5	-	VREF2_5
31	PB8A	5	T	-
32	PB8B	5	C	-
33	GNDIO5	5	-	-
34	PB9A	5	-	-
35	PB10B	5	-	-
36	PB11A	5	T	DQS
37	PB11B	5	C	-
38	VCCIO5	5	-	-
39	PB12A	5	T	-
40	PB12B	5	C	-
41	PB13A	5	T	-
42	PB13B	5	C	-
43	GND	-	-	-

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
93	PB19B	4	C	VREF1_4	PB22B	4	C	VREF1_4
94	PB20A	4	T	-	PB23A	4	T	-
95	PB20B	4	C	-	PB23B	4	C	-
96	PB21A	4	T	-	PB24A	4	T	-
97	VCCIO4	4	-	-	VCCIO4	4	-	-
98	PB21B	4	C	-	PB24B	4	C	-
99	PB22A	4	T	-	PB25A	4	T	-
100	PB22B	4	C	-	PB25B	4	C	-
101	PB23A	4	T	-	PB26A	4	T	-
102	PB23B	4	C	-	PB26B	4	C	-
103	PB24A	4	T	VREF2_4	PB27A	4	-	VREF2_4
104	PB24B	4	C	-	PB30A	4	T	DQS
105	PB25A	4	-	-	PB30B	4	C	-
106	GND	-	-	-	GND	-	-	-
107	VCC	-	-	-	VCC	-	-	-
108	PR18B	3	C[3]	-	PR26B	3	C[3]	-
109	GNDIO3	3	-	-	GNDIO3	3	-	-
110	PR18A	3	T[3]	-	PR26A	3	T[3]	-
111	PR17B	3	C	-	PR25B	3	C	-
112	PR17A	3	T	-	PR25A	3	T	-
113	PR16B	3	C[3]	-	PR24B	3	C[3]	-
114	PR16A	3	T[3]	DQS	PR24A	3	T[3]	DQS
115	VCCIO3	3	-	-	VCCIO3	3	-	-
116	PR15B	3	-	VREF1_3	PR23B	3	-	VREF1_3
117	PR14A	3	-	VREF2_3	PR22A	3	-	VREF2_3
118	GNDIO3	3	-	-	GNDIO3	3	-	-
119	PR13B	3	C	-	PR21B	3	C[3]	-
120	PR13A	3	T	-	PR21A	3	T[3]	-
121	GND	-	-	-	GND	-	-	-
122	PR12B	3	C	-	PR20B	3	C	-
123	PR12A	3	T	-	PR20A	3	T	-
124	PR11B	3	C	-	PR19B	3	C[3]	-
125	VCCIO3	3	-	-	VCCIO3	3	-	-
126	PR11A	3	T	-	PR19A	3	T[3]	-
127	GNDP1	-	-	-	GNDP1	-	-	-
128	VCCP1	-	-	-	VCCP1	-	-	-
129	NC	-	-	-	PR13A	2	-	-
130	GND	-	-	-	GND	-	-	-
131	PR9B	2	C	PCLKC2_0	PR12B	2	C	PCLKC2_0
132	PR9A	2	T	PCLKT2_0	PR12A	2	T	PCLKT2_0
133	NC	-	-	-	PR11B	2	C[3]	-
134	NC	-	-	-	PR11A	2	T[3]	-
135	GNDIO2	2	-	-	GNDIO2	2	-	-
136	PR8B	2	C	RUM0_PLLC_IN_A	PR8B	2	C	RUM0_PLLC_IN_A
137	PR8A	2	T	RUM0_PLLT_IN_A	PR8A	2	T	RUM0_PLLT_IN_A
138	PR7B	2	C[3]	-	PR7B	2	C[3]	-

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

	LFXP6				LFXP10			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
K4	PL20A	6	T	-	PL29A	6	T	-
K5	PL20B	6	C	-	PL29B	6	C	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
N1	PL23B	6	-	VREF2_6	PL31A	6	-	VREF2_6
N2	PL21B	6	C[3]	-	PL32B	6	-	-
P1	PL24A	6	T[3]	DQS	PL33A	6	T[3]	DQS
P2	PL24B	6	C[3]	-	PL33B	6	C[3]	-
L5	PL25A	6	T	-	PL34A	6	T	LLM0_PLLT_FB_A
M6	PL25B	6	C	-	PL34B	6	C	LLM0_PLLC_FB_A
M3	PL26A	6	T[3]	-	PL35A	6	T[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
N3	PL26B	6	C[3]	-	PL35B	6	C[3]	-
P4	SLEEPN[1]/TOE[2]	-	-	-	SLEEPN[1]/TOE[2]	-	-	-
P3	INITN	5	-	-	INITN	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
R4	PB2A	5	T	-	PB6A	5	T	-
N5	PB2B	5	C	-	PB6B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
P5	PB5B	5	-	VREF1_5	PB7A	5	T	VREF1_5
R1	PB3B	5	C	-	PB7B	5	C	-
N6	PB4A	5	-	-	PB8A	5	-	-
M7	PB3A	5	T	-	PB9B	5	-	-
R2	PB6A	5	T	DQS	PB10A	5	T	DQS
T2	PB6B	5	C	-	PB10B	5	C	-
R3	PB7A	5	T	-	PB11A	5	T	-
T3	PB7B	5	C	-	PB11B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
T4	PB8A	5	T	-	PB12A	5	T	-
R5	PB8B	5	C	VREF2_5	PB12B	5	C	VREF2_5
N7	PB9A	5	T	-	PB13A	5	T	-
M8	PB9B	5	C	-	PB13B	5	C	-
T5	PB10A	5	T	-	PB14A	5	T	-
P6	PB10B	5	C	-	PB14B	5	C	-
T6	PB11A	5	T	-	PB15A	5	T	-
R6	PB11B	5	C	-	PB15B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
P7	PB12A	5	-	-	PB16A	5	-	-
N8	PB13B	5	-	-	PB17B	5	-	-
R7	PB14A	5	T	DQS	PB18A	5	T	DQS
T7	PB14B	5	C	-	PB18B	5	C	-
P8	PB15A	5	T	-	PB19A	5	T	-
T8	PB15B	5	C	-	PB19B	5	C	-

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

	LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L4	PL32A	6	-	-	PL36A	6	-	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
K4	PL33A	6	T	-	PL37A	6	T	-
K5	PL33B	6	C	-	PL37B	6	C	-
N1	PL35A	6	-	VREF2_6	PL39A	6	-	VREF2_6
N2	PL36B	6	-	-	PL40B	6	-	-
P1	PL37A	6	T[3]	DQS	PL41A	6	T[3]	DQS
P2	PL37B	6	C[3]	-	PL41B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
L5	PL38A	6	T	LLM0_PLLT_FB_A	PL42A	6	T	LLM0_PLLT_FB_A
M6	PL38B	6	C	LLM0_PLLC_FB_A	PL42B	6	C	LLM0_PLLC_FB_A
M3	PL39A	6	T[3]	-	PL43A	6	T[3]	-
N3	PL39B	6	C[3]	-	PL43B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
P4	SLEEPN[1]/TOE[2]	-	-	-	SLEEPN[1]/TOE[2]	-	-	-
P3	INITN	5	-	-	INITN	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
R4	PB11A	5	T	-	PB15A	5	T	-
N5	PB11B	5	C	-	PB15B	5	C	-
P5	PB12A	5	T	VREF1_5	PB16A	5	T	VREF1_5
-	GNDIO5	5	-	-	GNDIO5	5	-	-
R1	PB12B	5	C	-	PB16B	5	C	-
N6	PB13A	5	-	-	PB17A	5	-	-
M7	PB14B	5	-	-	PB18B	5	-	-
R2	PB15A	5	T	DQS	PB19A	5	T	DQS
T2	PB15B	5	C	-	PB19B	5	C	-
R3	PB16A	5	T	-	PB20A	5	T	-
T3	PB16B	5	C	-	PB20B	5	C	-
T4	PB17A	5	T	-	PB21A	5	T	-
R5	PB17B	5	C	VREF2_5	PB21B	5	C	VREF2_5
N7	PB18A	5	T	-	PB22A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
M8	PB18B	5	C	-	PB22B	5	C	-
T5	PB19A	5	T	-	PB23A	5	T	-
P6	PB19B	5	C	-	PB23B	5	C	-
T6	PB20A	5	T	-	PB24A	5	T	-
R6	PB20B	5	C	-	PB24B	5	C	-
P7	PB21A	5	-	-	PB25A	5	-	-
N8	PB22B	5	-	-	PB26B	5	-	-
R7	PB23A	5	T	DQS	PB27A	5	T	DQS

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

	LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
G10	GND	-	-	-	GND	-	-	-
G7	GND	-	-	-	GND	-	-	-
G8	GND	-	-	-	GND	-	-	-
G9	GND	-	-	-	GND	-	-	-
H10	GND	-	-	-	GND	-	-	-
H7	GND	-	-	-	GND	-	-	-
H8	GND	-	-	-	GND	-	-	-
H9	GND	-	-	-	GND	-	-	-
J10	GND	-	-	-	GND	-	-	-
J7	GND	-	-	-	GND	-	-	-
J8	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-
K10	GND	-	-	-	GND	-	-	-
K7	GND	-	-	-	GND	-	-	-
K8	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-
L6	GND	-	-	-	GND	-	-	-
T1	GND	-	-	-	GND	-	-	-
T16	GND	-	-	-	GND	-	-	-
D13	VCC	-	-	-	VCC	-	-	-
D4	VCC	-	-	-	VCC	-	-	-
E12	VCC	-	-	-	VCC	-	-	-
E5	VCC	-	-	-	VCC	-	-	-
M12	VCC	-	-	-	VCC	-	-	-
M5	VCC	-	-	-	VCC	-	-	-
N13	VCC	-	-	-	VCC	-	-	-
N4	VCC	-	-	-	VCC	-	-	-
E13	VCCAUX	-	-	-	VCCAUX	-	-	-
E4	VCCAUX	-	-	-	VCCAUX	-	-	-
M13	VCCAUX	-	-	-	VCCAUX	-	-	-
M4	VCCAUX	-	-	-	VCCAUX	-	-	-
F7	VCCIO0	0	-	-	VCCIO0	0	-	-
F8	VCCIO0	0	-	-	VCCIO0	0	-	-
F10	VCCIO1	1	-	-	VCCIO1	1	-	-
F9	VCCIO1	1	-	-	VCCIO1	1	-	-
G11	VCCIO2	2	-	-	VCCIO2	2	-	-
H11	VCCIO2	2	-	-	VCCIO2	2	-	-
J11	VCCIO3	3	-	-	VCCIO3	3	-	-
K11	VCCIO3	3	-	-	VCCIO3	3	-	-
L10	VCCIO4	4	-	-	VCCIO4	4	-	-
L9	VCCIO4	4	-	-	VCCIO4	4	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA

	LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
F5	PROGRAMN	7	-	-	PROGRAMN	7	-	-
E3	CCLK	7	-	-	CCLK	7	-	-
C1	PL2B	7	-	-	PL2B	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
G5	PL3A	7	T[3]	-	PL3A	7	T[3]	-
G6	PL3B	7	C[3]	-	PL3B	7	C[3]	-
F4	PL4A	7	T	-	PL4A	7	T	-
F3	PL4B	7	C	-	PL4B	7	C	-
G4	PL5A	7	T[3]	-	PL5A	7	T[3]	-
G3	PL5B	7	C[3]	-	PL5B	7	C[3]	-
D1	PL6A	7	T[3]	-	PL6A	7	T[3]	-
D2	PL6B	7	C[3]	-	PL6B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
E1	PL7A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A
E2	PL7B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A
H5	PL8A	7	T[3]	-	PL8A	7	T[3]	-
H6	PL8B	7	C[3]	-	PL8B	7	C[3]	-
H4	PL9A	7	-	-	PL9A	7	-	-
H3	PL10B	7	-	VREF1_7	PL10B	7	-	VREF1_7
F1	PL11A	7	T[3]	DQS	PL11A	7	T[3]	DQS
F2	PL11B	7	C[3]	-	PL11B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
J5	PL12A	7	T	-	PL12A	7	T	-
J6	PL12B	7	C	-	PL12B	7	C	-
G1	PL13A	7	T[3]	-	PL13A	7	T[3]	-
G2	PL13B	7	C[3]	-	PL13B	7	C[3]	-
J4	PL15A	7	T[3]	-	PL15A	7	T[3]	-
J3	PL15B	7	C[3]	-	PL15B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
H1	PL16A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A
H2	PL16B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A
J1	PL17A	7	T[3]	-	PL17A	7	T[3]	-
J2	PL17B	7	C[3]	-	PL17B	7	C[3]	-
K3	PL18A	7	-	VREF2_7	PL18A	7	-	VREF2_7
K2	PL19B	7	-	-	PL19B	7	-	-
K4	PL20A	7	T[3]	DQS	PL20A	7	T[3]	DQS
-	GNDIO7	7	-	-	GNDIO7	7	-	-
K5	PL20B	7	C[3]	-	PL20B	7	C[3]	-
K1	PL21A	7	T	-	PL21A	7	T	-
L2	PL21B	7	C	-	PL21B	7	C	-
L4	PL22A	7	T[3]	-	PL22A	7	T[3]	-
L3	PL22B	7	C[3]	-	PL22B	7	C[3]	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

	LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
R18	PR38B	3	C	RLM0_PLLC_FB_A	PR42B	3	C	RLM0_PLLC_FB_A
R17	PR38A	3	T	RLM0_PLLT_FB_A	PR42A	3	T	RLM0_PLLT_FB_A
Y22	PR37B	3	C[3]	-	PR41B	3	C[3]	-
Y21	PR37A	3	T[3]	DQS	PR41A	3	T[3]	DQS
W22	PR36B	3	-	-	PR40B	3	-	-
W21	PR35A	3	-	VREF1_3	PR39A	3	-	VREF1_3
P17	PR34B	3	C[3]	-	PR38B	3	C[3]	-
P18	PR34A	3	T[3]	-	PR38A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
R19	PR33B	3	C	-	PR37B	3	C	-
R20	PR33A	3	T	-	PR37A	3	T	-
V22	PR32B	3	C[3]	-	PR36B	3	C[3]	-
V21	PR32A	3	T[3]	-	PR36A	3	T[3]	-
U22	PR30B	3	C[3]	-	PR34B	3	C[3]	-
U21	PR30A	3	T[3]	-	PR34A	3	T[3]	-
P19	PR29B	3	C	RLM0_PLLC_IN_A	PR33B	3	C	RLM0_PLLC_IN_A
P20	PR29A	3	T	RLM0_PLLT_IN_A	PR33A	3	T	RLM0_PLLT_IN_A
-	GNDIO3	3	-	-	GNDIO3	3	-	-
T22	PR28B	3	C[3]	-	PR32B	3	C[3]	-
T21	PR28A	3	T[3]	DQS	PR32A	3	T[3]	DQS
R22	PR27B	3	-	-	PR31B	3	-	-
R21	PR26A	3	-	VREF2_3	PR30A	3	-	VREF2_3
N19	PR25B	3	C[3]	-	PR29B	3	C[3]	-
N20	PR25A	3	T[3]	-	PR29A	3	T[3]	-
N18	PR24B	3	C	-	PR28B	3	C	-
M18	PR24A	3	T	-	PR28A	3	T	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
P22	PR23B	3	C[3]	-	PR27B	3	C[3]	-
P21	PR23A	3	T[3]	-	PR27A	3	T[3]	-
N22	-	-	-	-	PR26B	3	C[3]	-
N21	-	-	-	-	PR26A	3	T[3]	-
M19	-	-	-	-	PR25B	3	-	-
M20	GNDP1	-	-	-	GNDP1	-	-	-
L18	VCCP1	-	-	-	VCCP1	-	-	-
M21	-	-	-	-	PR24A	2	-	-
M22	PR22B	2	C[3]	-	PR23B	2	C[3]	-
L22	PR22A	2	T[3]	-	PR23A	2	T[3]	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
L19	-	-	-	-	PR22B	2	C[3]	-
L20	-	-	-	-	PR22A	2	T[3]	-
L21	PR21B	2	C	PCLKC2_0	PR21B	2	C	PCLKC2_0
K22	PR21A	2	T	PCLKT2_0	PR21A	2	T	PCLKT2_0

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

	LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
J15	GND	-	-	-	GND	-	-	-
J8	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-
K10	GND	-	-	-	GND	-	-	-
K11	GND	-	-	-	GND	-	-	-
K12	GND	-	-	-	GND	-	-	-
K13	GND	-	-	-	GND	-	-	-
K14	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-
L10	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-
L12	GND	-	-	-	GND	-	-	-
L13	GND	-	-	-	GND	-	-	-
L14	GND	-	-	-	GND	-	-	-
L9	GND	-	-	-	GND	-	-	-
M10	GND	-	-	-	GND	-	-	-
M11	GND	-	-	-	GND	-	-	-
M12	GND	-	-	-	GND	-	-	-
M13	GND	-	-	-	GND	-	-	-
M14	GND	-	-	-	GND	-	-	-
M9	GND	-	-	-	GND	-	-	-
N10	GND	-	-	-	GND	-	-	-
N11	GND	-	-	-	GND	-	-	-
N12	GND	-	-	-	GND	-	-	-
N13	GND	-	-	-	GND	-	-	-
N14	GND	-	-	-	GND	-	-	-
N9	GND	-	-	-	GND	-	-	-
P10	GND	-	-	-	GND	-	-	-
P11	GND	-	-	-	GND	-	-	-
P12	GND	-	-	-	GND	-	-	-
P13	GND	-	-	-	GND	-	-	-
P14	GND	-	-	-	GND	-	-	-
P15	GND	-	-	-	GND	-	-	-
P8	GND	-	-	-	GND	-	-	-
P9	GND	-	-	-	GND	-	-	-
R14	GND	-	-	-	GND	-	-	-
R9	GND	-	-	-	GND	-	-	-
F10	VCC	-	-	-	VCC	-	-	-
F13	VCC	-	-	-	VCC	-	-	-
G10	VCC	-	-	-	VCC	-	-	-
G13	VCC	-	-	-	VCC	-	-	-
G14	VCC	-	-	-	VCC	-	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

	LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
G9	VCC	-	-	-	VCC	-	-	-
H15	VCC	-	-	-	VCC	-	-	-
H8	VCC	-	-	-	VCC	-	-	-
J16	VCC	-	-	-	VCC	-	-	-
J7	VCC	-	-	-	VCC	-	-	-
K16	VCC	-	-	-	VCC	-	-	-
K17	VCC	-	-	-	VCC	-	-	-
K6	VCC	-	-	-	VCC	-	-	-
K7	VCC	-	-	-	VCC	-	-	-
N16	VCC	-	-	-	VCC	-	-	-
N17	VCC	-	-	-	VCC	-	-	-
N6	VCC	-	-	-	VCC	-	-	-
N7	VCC	-	-	-	VCC	-	-	-
P16	VCC	-	-	-	VCC	-	-	-
P7	VCC	-	-	-	VCC	-	-	-
R15	VCC	-	-	-	VCC	-	-	-
R8	VCC	-	-	-	VCC	-	-	-
T10	VCC	-	-	-	VCC	-	-	-
T13	VCC	-	-	-	VCC	-	-	-
T14	VCC	-	-	-	VCC	-	-	-
T9	VCC	-	-	-	VCC	-	-	-
U10	VCC	-	-	-	VCC	-	-	-
U13	VCC	-	-	-	VCC	-	-	-
G15	VCCAUX	-	-	-	VCCAUX	-	-	-
G16	VCCAUX	-	-	-	VCCAUX	-	-	-
G7	VCCAUX	-	-	-	VCCAUX	-	-	-
G8	VCCAUX	-	-	-	VCCAUX	-	-	-
H16	VCCAUX	-	-	-	VCCAUX	-	-	-
H7	VCCAUX	-	-	-	VCCAUX	-	-	-
R16	VCCAUX	-	-	-	VCCAUX	-	-	-
R7	VCCAUX	-	-	-	VCCAUX	-	-	-
T15	VCCAUX	-	-	-	VCCAUX	-	-	-
T16	VCCAUX	-	-	-	VCCAUX	-	-	-
T7	VCCAUX	-	-	-	VCCAUX	-	-	-
T8	VCCAUX	-	-	-	VCCAUX	-	-	-
F11	VCCIO0	0	-	-	VCCIO0	0	-	-
G11	VCCIO0	0	-	-	VCCIO0	0	-	-
H10	VCCIO0	0	-	-	VCCIO0	0	-	-
H11	VCCIO0	0	-	-	VCCIO0	0	-	-
F12	VCCIO1	1	-	-	VCCIO1	1	-	-
G12	VCCIO1	1	-	-	VCCIO1	1	-	-
H12	VCCIO1	1	-	-	VCCIO1	1	-	-

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following located on the Lattice website at www.latticesemi.com.

- Thermal Management document
- Technical Note TN1052 - Power Estimation and Management for LatticeECP/EC and LatticeXP Devices
- Power Calculator tool included with Lattice's ispLEVER design tool, or as a standalone download from www.latticesemi.com/software