Lattice Semiconductor Corporation - LFXP3C-3TN100C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	3000
Total RAM Bits	55296
Number of I/O	62
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp3c-3tn100c

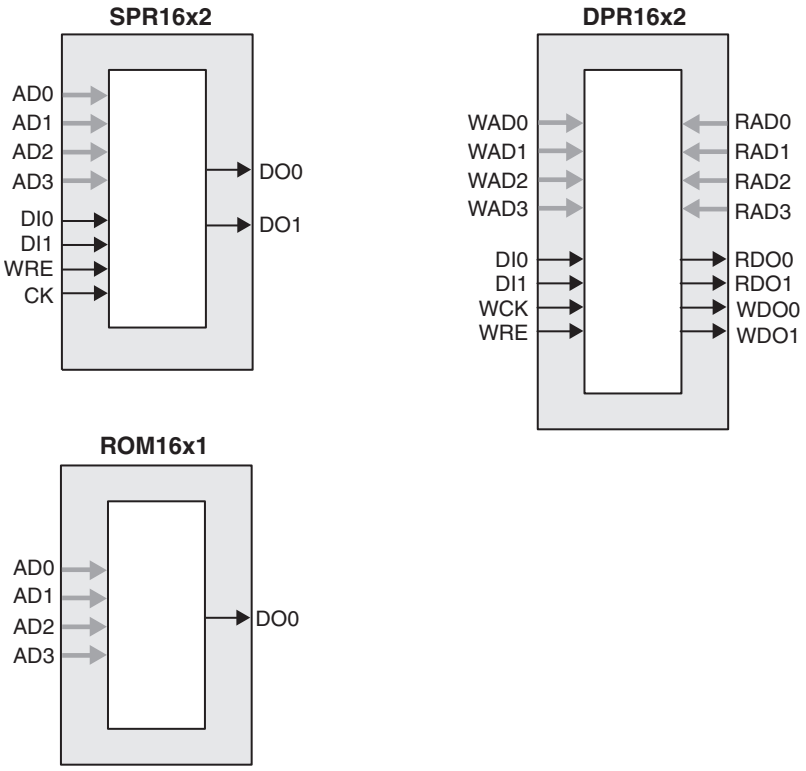
The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-4 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices, one Slice functions as the read-write port. The other companion Slice supports the read-only port. For more information on RAM mode in LatticeXP devices, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required for Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of Slices	1	2

Note: SPR = Single Port RAM, DPR = Dual Port RAM

Figure 2-4. Distributed Memory Primitives

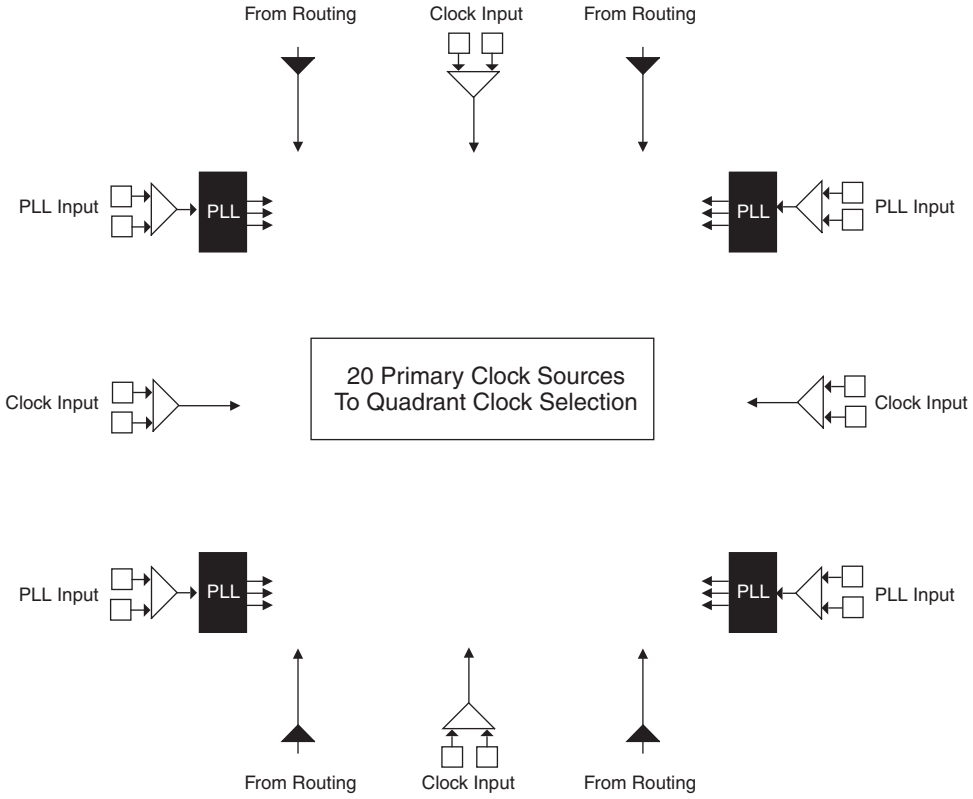


ROM Mode: The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

Figure 2-5. Primary Clock Sources



Note: Smaller devices have two PLLs.

Secondary Clock Sources

LatticeXP devices have four secondary clock resources per quadrant. The secondary clock branches are tapped at every PFU. These secondary clock networks can also be used for controls and high fanout data. These secondary clocks are derived from four clock input pads and 16 routing signals as shown in Figure 2-6.

Initialization Supply Current[1, 2, 3, 4, 5, 6]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[7]	Units
I_{CC}	Core Power Supply	LFXP3E	40	mA
		LFXP6E	50	mA
		LFXP10E	110	mA
		LFXP15E	140	mA
		LFXP20E	250	mA
		LFXP3C	60	mA
		LFXP6C	70	mA
		LFXP10C	150	mA
		LFXP15C	180	mA
		LFXP20C	290	mA
I_{CCAUX}	Auxiliary Power Supply V_{CCAUX} = 3.3V	LFXP3E/C	50	mA
		LFXP6E/C	60	mA
		LFXP10E/C	90	mA
		LFXP15 /C	110	mA
		LFXP20E/C	130	mA
I_{CCJ}	V_{CCJ} Power Supply	All	2	mA

1. Until DONE signal is active.
2. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
4. Frequency 0MHz.
5. Typical user pattern.
6. Assume normal bypass capacitor/decoupling capacitor across the supply.
7. T_A=25°C, power supplies at nominal voltage.

sysIO Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.5	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	8, 4	-8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2 (“C” Version)	-0.3	0.42	0.78	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2 (“E” Version)	-0.3	$0.35V_{CC}$	$0.65V_{CC}$	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
PCI	-0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	-0.5
SSTL3 class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCIO} - 1.1	8	-8
SSTL3 class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCIO} - 0.9	16	-16
SSTL2 class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	7.6	-7.6
SSTL2 class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCIO} - 0.43	15.2	-15.2
SSTL18 class I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.4	V_{CCIO} - 0.4	6.7	-6.7
HSTL15 class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	8	-8
HSTL15 class III	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	24	-8
HSTL18 class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	9.6	-9.6
HSTL18 class II	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	16	-16
HSTL18 class III	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	24	-8

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions
Test and Programming (Dedicated pins. Pull-up is enabled on input pins during configuration.)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data in pin, used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence).
TDO	O	Output pin -Test Data out pin used to shift data out of device using 1149.1.
V_{CCJ}	—	V_{CCJ} - The power supply pin for JTAG Test Access Port.
Configuration Pads (used during sysCONFIG)		
CFG[1:0]	I	Mode pins used to specify configuration modes values latched on rising edge of INITN. During configuration, a pull-up is enabled.
INITN	I/O	Open Drain pin - Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. If CFG1 and CFG0 are high (SDM) then this pin is pulled low.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
DONE	I/O	Open Drain pin - Indicates that the configuration sequence is complete, and the startup sequence is in progress.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
BUSY	I/O	Generally not used. After configuration it is a user-programmable I/O pin.
CSN	I	sysCONFIG chip select (Active low). During configuration, a pull-up is enabled. After configuration it is user a programmable I/O pin.
CS1N	I	sysCONFIG chip select (Active Low). During configuration, a pull-up is enabled. After configuration it is user programmable I/O pin
WRITEN	I	Write Data on Parallel port (Active low). After configuration it is a user programmable I/O pin
D[7:0]	I/O	sysCONFIG Port Data I/O. After configuration these are user programmable I/O pins.
DOUT, CSON	O	Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port. After configuration, it is a user-programmable I/O pin.
DI	I	Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. After configuration it is a user-programmable I/O pin.
SLEEPN[2]	I	Sleep Mode pin - Active low sleep pin.þ When this pin is held high, the device operates normally.þ When driven low, the device moves into Sleep Mode after a specified time.This pin has a weak internal pull-up, but when not used an external pull-up to V_{CC} is recommended.
TOE[3]	I	Test Output Enable tri-states all I/O pins when driven low. This pin has a weak internal pull-up, but when not used an external pull-up to V_{CC} is recommended.

1. Applies toþ LFXP10, LFXP15 and LFXP20 only.
2. Applies to LFXP “C” devices only.
3. Applies to LFXP “E” devices only.

Pin Information Summary[1]

Pin Type		XP3			XP6		
		100 TQFP	144 TQFP	208 PQFP	144 TQFP	208 PQFP	256 fpBGA
Single Ended User I/O		62	100	136	100	142	188
Differential Pair User I/O[2]		19	35	56	35	58	80
Configuration	Dedicated	11	11	11	11	11	11
	Muxed	14	14	14	14	14	14
TAP		5	5	5	5	5	5
Dedicated (total without supplies)		6	6	6	6	6	6
V_{CC}		2	4	8	4	8	8
V_{CCAUX}		2	2	2	2	2	4
V_{CCPLL}		2	2	2	2	2	2
V_{CCIO}	Bank0	1	1	2	1	2	2
	Bank1	1	1	2	1	2	2
	Bank2	1	1	2	1	2	2
	Bank3	1	1	2	1	2	2
	Bank4	1	2	2	2	2	2
	Bank5	1	1	2	1	2	2
	Bank6	1	1	2	1	2	2
	Bank7	1	1	2	1	2	2
GND		10	13	24	13	24	24
GND_{PLL}		2	2	2	2	2	2
NC		0	0	6	0	0	0
Single Ended/Differential I/O per Bank[2]	Bank0	8/2	12/3	20/8	12/3	20/8	26/11
	Bank1	9/0	12/2	18/6	12/2	18/6	26/11
	Bank2	8/3	12/5	14/6	12/5	17/7	21/9
	Bank3	6/2	13/5	14/6	13/5	14/6	21/9
	Bank4	5/2	14/6	21/9	14/6	21/9	26/11
	Bank5	12/4	12/4	21/9	12/4	21/9	26/11
	Bank6	4/2	13/5	14/6	13/5	17/7	21/9
	Bank7	10/4	12/5	14/6	12/5	14/6	21/9
V_{CCJ}		1	1	1	1	1	1

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
2. The differential I/O per bank includes both dedicated LVDS and emulated LVDS pin pairs. Please see the Logic Signal Connections table for more information.

LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
1	PROGRAMN	7	-	-	PROGRAMN	7	-	-
2	CCLK	7	-	-	CCLK	7	-	-
3	GND	-	-	-	GND	-	-	-
4	PL2A	7	T[3]	-	PL2A	7	T[3]	-
5	PL2B	7	C[3]	-	PL2B	7	C[3]	-
6	PL3A	7	T	LUM0_PLLT_FB_A	PL3A	7	T	LUM0_PLLT_FB_A
7	PL3B	7	C	LUM0_PLLC_FB_A	PL3B	7	C	LUM0_PLLC_FB_A
8	VCCIO7	7	-	-	VCCIO7	7	-	-
9	PL5A	7	-	VREF1_7	PL5A	7	-	VREF1_7
10	PL6B	7	-	VREF2_7	PL6B	7	-	VREF2_7
11	GNDIO7	7	-	-	GNDIO7	7	-	-
12	PL7A	7	T[3]	DQS	PL7A	7	T[3]	DQS
13	PL7B	7	C[3]	-	PL7B	7	C[3]	-
14	VCC	-	-	-	VCC	-	-	-
15	PL8A	7	T	LUM0_PLLT_IN_A	PL8A	7	T	LUM0_PLLT_IN_A
16	PL8B	7	C	LUM0_PLLC_IN_A	PL8B	7	C	LUM0_PLLC_IN_A
17	PL9A	7	T[3]	-	PL9A	7	T[3]	-
18	PL9B	7	C[3]	-	PL9B	7	C[3]	-
19	VCCP0	-	-	-	VCCP0	-	-	-
20	GNDP0	-	-	-	GNDP0	-	-	-
21	VCCIO6	6	-	-	VCCIO6	6	-	-
22	PL11A	6	T[3]	-	PL16A	6	T[3]	-
23	PL11B	6	C[3]	-	PL16B	6	C[3]	-
24	PL12A	6	T	PCLKT6_0	PL17A	6	T	PCLKT6_0
25	PL12B	6	C	PCLKC6_0	PL17B	6	C	PCLKC6_0
26	PL13A	6	T[3]	-	PL18A	6	T[3]	-
27	PL13B	6	C[3]	-	PL18B	6	C[3]	-
28	GNDIO6	6	-	-	GNDIO6	6	-	-
29	PL14A	6	-	VREF1_6	PL22A	6	-	VREF1_6
30	PL15B	6	-	VREF2_6	PL23B	6	-	VREF2_6
31	PL16A	6	T[3]	DQS	PL24A	6	T[3]	DQS
32	PL16B	6	C[3]	-	PL24B	6	C[3]	-
33	PL17A	6	-	-	PL25A	6	-	-
34	PL18A	6	T[3]	-	PL26A	6	T[3]	-
35	PL18B	6	C[3]	-	PL26B	6	C[3]	-
36	VCCAUX	-	-	-	VCCAUX	-	-	-
37	SLEEPN[1]/TOE[2]	-	-	-	SLEEPN[1]/TOE[2]	-	-	-
38	INITN	5	-	-	INITN	5	-	-
39	VCC	-	-	-	VCC	-	-	-
40	PB2B	5	-	VREF1_5	PB5B	5	-	VREF1_5
41	PB5B	5	-	VREF2_5	PB8B	5	-	VREF2_5
42	PB7A	5	T	-	PB10A	5	T	-
43	PB7B	5	C	-	PB10B	5	C	-
44	GNDIO5	5	-	-	GNDIO5	5	-	-
45	PB9A	5	-	-	PB12A	5	-	-
46	PB10B	5	-	-	PB13B	5	-	-

LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
47	PB11A	5	T	DQS	PB14A	5	T	DQS
48	PB11B	5	C	-	PB14B	5	C	-
49	VCCIO5	5	-	-	VCCIO5	5	-	-
50	PB12A	5	T	-	PB15A	5	T	-
51	PB12B	5	C	-	PB15B	5	C	-
52	PB13A	5	T	-	PB16A	5	T	-
53	PB13B	5	C	-	PB16B	5	C	-
54	GND	-	-	-	GND	-	-	-
55	PB14A	4	T	-	PB17A	4	T	-
56	GNDIO4	4	-	-	GNDIO4	4	-	-
57	PB14B	4	C	-	PB17B	4	C	-
58	PB15A	4	T	PCLKT4_0	PB18A	4	T	PCLKT4_0
59	PB15B	4	C	PCLKC4_0	PB18B	4	C	PCLKC4_0
60	PB16A	4	T	-	PB19A	4	T	-
61	VCCIO4	4	-	-	VCCIO4	4	-	-
62	PB16B	4	C	-	PB19B	4	C	-
63	PB19A	4	T	DQS	PB22A	4	T	DQS
64	GNDIO4	4	-	-	GNDIO4	4	-	-
65	PB19B	4	C	VREF1_4	PB22B	4	C	VREF1_4
66	PB20A	4	T	-	PB23A	4	T	-
67	PB20B	4	C	-	PB23B	4	C	-
68	VCCIO4	4	-	-	VCCIO4	4	-	-
69	PB22A	4	-	-	PB25A	4	-	-
70	PB24A	4	T	VREF2_4	PB27A	4	T	VREF2_4
71	PB24B	4	C	-	PB27B	4	C	-
72	PB25A	4	-	-	PB28A	4	-	-
73	VCC	-	-	-	VCC	-	-	-
74	PR18B	3	C[3]	-	PR26B	3	C[3]	-
75	GNDIO3	3	-	-	GNDIO3	3	-	-
76	PR18A	3	T[3]	-	PR26A	3	T[3]	-
77	PR17B	3	C	-	PR25B	3	C	-
78	PR17A	3	T	-	PR25A	3	T	-
79	PR16B	3	C[3]	-	PR24B	3	C[3]	-
80	PR16A	3	T[3]	DQS	PR24A	3	T[3]	DQS
81	PR15B	3	-	VREF1_3	PR23B	3	-	VREF1_3
82	PR14A	3	-	VREF2_3	PR22A	3	-	VREF2_3
83	PR13B	3	C	-	PR21B	3	C[3]	-
84	PR13A	3	T	-	PR21A	3	T[3]	-
85	GND	-	-	-	GND	-	-	-
86	PR12A	3	-	-	PR20A	3	-	-
87	PR11B	3	C	-	PR19B	3	C[3]	-
88	VCCIO3	3	-	-	VCCIO3	3	-	-
89	PR11A	3	T	-	PR19A	3	T[3]	-
90	GNDP1	-	-	-	GNDP1	-	-	-
91	VCCP1	-	-	-	VCCP1	-	-	-
92	PR9B	2	C	PCLKC2_0	PR12B	2	C	PCLKC2_0

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
185	PT13A	0	T	CS1N	PT16A	0	T	CS1N
186	PT12B	0	C	PCLKC0_0	PT15B	0	C	PCLKC0_0
187	PT12A	0	T	PCLKT0_0	PT15A	0	T	PCLKT0_0
188	PT11B	0	C	-	PT14B	0	C	-
189	VCCIO0	0	-	-	VCCIO0	0	-	-
190	PT11A	0	T	DQS	PT14A	0	T	DQS
191	PT10B	0	-	-	PT13B	0	-	-
192	PT9A	0	-	DOUT	PT12A	0	-	DOUT
193	PT8B	0	C	-	PT11B	0	C	-
194	GNDIO0	0	-	-	GNDIO0	0	-	-
195	PT8A	0	T	WRITEN	PT11A	0	T	WRITEN
196	PT7B	0	C	-	PT10B	0	C	-
197	PT7A	0	T	VREF1_0	PT10A	0	T	VREF1_0
198	PT6B	0	C	-	PT9B	0	C	-
199	VCCIO0	0	-	-	VCCIO0	0	-	-
200	PT6A	0	T	DI	PT9A	0	T	DI
201	PT5B	0	C	-	PT8B	0	C	-
202	PT5A	0	T	CSN	PT8A	0	T	CSN
203	PT4B	0	C	-	PT7B	0	C	-
204	PT4A	0	T	-	PT7A	0	T	-
205	PT3B	0	-	VREF2_0	PT6B	0	-	VREF2_0
206	PT2B	0	-	-	PT5B	0	-	-
207	GND	-	-	-	GND	-	-	-
208	CFG0	0	-	-	CFG0	0	-	-

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L4	PL32A	6	-	-	PL36A	6	-	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
K4	PL33A	6	T	-	PL37A	6	T	-
K5	PL33B	6	C	-	PL37B	6	C	-
N1	PL35A	6	-	VREF2_6	PL39A	6	-	VREF2_6
N2	PL36B	6	-	-	PL40B	6	-	-
P1	PL37A	6	T[3]	DQS	PL41A	6	T[3]	DQS
P2	PL37B	6	C[3]	-	PL41B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
L5	PL38A	6	T	LLM0_PLLT_FB_A	PL42A	6	T	LLM0_PLLT_FB_A
M6	PL38B	6	C	LLM0_PLLC_FB_A	PL42B	6	C	LLM0_PLLC_FB_A
M3	PL39A	6	T[3]	-	PL43A	6	T[3]	-
N3	PL39B	6	C[3]	-	PL43B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
P4	SLEEPN[1]/TOE[2]	-	-	-	SLEEPN[1]/TOE[2]	-	-	-
P3	INITN	5	-	-	INITN	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
R4	PB11A	5	T	-	PB15A	5	T	-
N5	PB11B	5	C	-	PB15B	5	C	-
P5	PB12A	5	T	VREF1_5	PB16A	5	T	VREF1_5
-	GNDIO5	5	-	-	GNDIO5	5	-	-
R1	PB12B	5	C	-	PB16B	5	C	-
N6	PB13A	5	-	-	PB17A	5	-	-
M7	PB14B	5	-	-	PB18B	5	-	-
R2	PB15A	5	T	DQS	PB19A	5	T	DQS
T2	PB15B	5	C	-	PB19B	5	C	-
R3	PB16A	5	T	-	PB20A	5	T	-
T3	PB16B	5	C	-	PB20B	5	C	-
T4	PB17A	5	T	-	PB21A	5	T	-
R5	PB17B	5	C	VREF2_5	PB21B	5	C	VREF2_5
N7	PB18A	5	T	-	PB22A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
M8	PB18B	5	C	-	PB22B	5	C	-
T5	PB19A	5	T	-	PB23A	5	T	-
P6	PB19B	5	C	-	PB23B	5	C	-
T6	PB20A	5	T	-	PB24A	5	T	-
R6	PB20B	5	C	-	PB24B	5	C	-
P7	PB21A	5	-	-	PB25A	5	-	-
N8	PB22B	5	-	-	PB26B	5	-	-
R7	PB23A	5	T	DQS	PB27A	5	T	DQS

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
P16	PR37B	3	C[3]	-	PR41B	3	C[3]	-
R16	PR37A	3	T[3]	DQS	PR41A	3	T[3]	DQS
M15	PR36B	3	-	-	PR40B	3	-	-
N14	PR35A	3	-	VREF1_3	PR39A	3	-	VREF1_3
-	GNDIO3	3	-	-	GNDIO3	3	-	-
M14	PR33B	3	C	-	PR37B	3	C	-
L13	PR33A	3	T	-	PR37A	3	T	-
L15	PR32B	3	C[3]	-	PR36B	3	C[3]	-
L14	PR32A	3	T[3]	-	PR36A	3	T[3]	-
L12	PR30A	3	-	-	PR34A	3	-	-
M16	PR29B	3	C	RLM0_PLLC_IN_A	PR33B	3	C	RLM0_PLLC_IN_A
N16	PR29A	3	T	RLM0_PLLT_IN_A	PR33A	3	T	RLM0_PLLT_IN_A
-	GNDIO3	3	-	-	GNDIO3	3	-	-
K14	PR28B	3	C[3]	-	PR32B	3	C[3]	-
K15	PR28A	3	T[3]	DQS	PR32A	3	T[3]	DQS
K12	PR27B	3	-	-	PR31B	3	-	-
K13	PR26A	3	-	VREF2_3	PR30A	3	-	VREF2_3
L16	PR25B	3	C[3]	-	PR29B	3	C[3]	-
K16	PR25A	3	T[3]	-	PR29A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
J15	PR23B	3	C[3]	-	PR27B	3	C[3]	-
J14	PR23A	3	T[3]	-	PR27A	3	T[3]	-
J13	GNDP1	-	-	-	GNDP1	-	-	-
J12	VCCP1	-	-	-	VCCP1	-	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
J16	PR21B	2	C	PCLKC2_0	PR21B	2	C	PCLKC2_0
H16	PR21A	2	T	PCLKT2_0	PR21A	2	T	PCLKT2_0
H13	PR20B	2	C[3]	-	PR20B	2	C[3]	-
H12	PR20A	2	T[3]	DQS	PR20A	2	T[3]	DQS
H15	PR19B	2	-	-	PR19B	2	-	-
H14	PR18A	2	-	VREF1_2	PR18A	2	-	VREF1_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G15	PR17B	2	C[3]	-	PR17B	2	C[3]	-
G14	PR17A	2	T[3]	-	PR17A	2	T[3]	-
G16	PR16B	2	C	RUM0_PLLC_IN_A	PR16B	2	C	RUM0_PLLC_IN_A
F16	PR16A	2	T	RUM0_PLLT_IN_A	PR16A	2	T	RUM0_PLLT_IN_A
G13	PR15B	2	-	-	PR15B	2	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G12	PR12B	2	C	-	PR12B	2	C	-
F13	PR12A	2	T	-	PR12A	2	T	-
B16	PR11B	2	C[3]	-	PR11B	2	C[3]	-
C16	PR11A	2	T[3]	DQS	PR11A	2	T[3]	DQS

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
F4	PROGRAMN	7	-	-	PROGRAMN	7	-	-	PROGRAMN	7	-	-
G4	CCLK	7	-	-	CCLK	7	-	-	CCLK	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
D2	PL2A	7	T[3]	-	PL6A	7	T[3]	-	PL6A	7	T[3]	-
D1	PL2B	7	C[3]	-	PL6B	7	C[3]	-	PL6B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
E2	PL3A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A
E3	PL3B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A
F3	PL4A	7	T[3]	-	PL8A	7	T[3]	-	PL8A	7	T[3]	-
F2	PL4B	7	C[3]	-	PL8B	7	C[3]	-	PL8B	7	C[3]	-
H4	PL5A	7	-	-	PL9A	7	-	-	PL9A	7	-	-
H3	PL6B	7	-	VREF1_7	PL10B	7	-	VREF1_7	PL10B	7	-	VREF1_7
G3	PL7A	7	T[3]	DQS	PL11A	7	T[3]	DQS	PL11A	7	T[3]	DQS
G2	PL7B	7	C[3]	-	PL11B	7	C[3]	-	PL11B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
F1	PL8A	7	T	-	PL12A	7	T	-	PL12A	7	T	-
E1	PL8B	7	C	-	PL12B	7	C	-	PL12B	7	C	-
J4	PL9A	7	T[3]	-	PL13A	7	T[3]	-	PL13A	7	T[3]	-
K4	PL9B	7	C[3]	-	PL13B	7	C[3]	-	PL13B	7	C[3]	-
G1	PL11A	7	T[3]	-	PL15A	7	T[3]	-	PL15A	7	T[3]	-
H2	PL11B	7	C[3]	-	PL15B	7	C[3]	-	PL15B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
J2	PL12A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A
H1	PL12B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A
J1	PL13A	7	T[3]	-	PL17A	7	T[3]	-	PL17A	7	T[3]	-
K2	PL13B	7	C[3]	-	PL17B	7	C[3]	-	PL17B	7	C[3]	-
K3	PL14A	7	-	VREF2_7	PL18A	7	-	VREF2_7	PL18A	7	-	VREF2_7
J3	PL15B	7	-	-	PL19B	7	-	-	PL19B	7	-	-
K1	PL16A	7	T[3]	DQS	PL20A	7	T[3]	DQS	PL20A	7	T[3]	DQS
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
L2	PL16B	7	C[3]	-	PL20B	7	C[3]	-	PL20B	7	C[3]	-
L3	PL17A	7	T	-	PL21A	7	T	-	PL21A	7	T	-
L4	PL17B	7	C	-	PL21B	7	C	-	PL21B	7	C	-
L1	PL18A	7	T[3]	-	PL22A	7	T[3]	-	PL22A	7	T[3]	-
M1	PL18B	7	C[3]	-	PL22B	7	C[3]	-	PL22B	7	C[3]	-
M2	VCCP0	-	-	-	VCCP0	-	-	-	VCCP0	-	-	-
N1	GNDP0	-	-	-	GNDP0	-	-	-	GNDP0	-	-	-
M3	PL19A	6	T[3]	-	PL23A	6	T[3]	-	PL27A	6	T[3]	-
M4	PL19B	6	C[3]	-	PL23B	6	C[3]	-	PL27B	6	C[3]	-
P1	PL20A	6	T	PCLKT6_0	PL24A	6	T	PCLKT6_0	PL28A	6	T	PCLKT6_0
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
N2	PL20B	6	C	PCLKC6_0	PL24B	6	C	PCLKC6_0	PL28B	6	C	PCLKC6_0
R1	PL21A	6	T[3]	-	PL25A	6	T[3]	-	PL29A	6	T[3]	-
P2	PL21B	6	C[3]	-	PL25B	6	C[3]	-	PL29B	6	C[3]	-
N3	PL22A	6	-	-	PL26A	6	-	-	PL30A	6	-	-
N4	PL23B	6	-	VREF1_6	PL27B	6	-	VREF1_6	PL31B	6	-	VREF1_6
T1	PL24A	6	T[3]	DQS	PL28A	6	T[3]	DQS	PL32A	6	T[3]	DQS
R2	PL24B	6	C[3]	-	PL28B	6	C[3]	-	PL32B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
U1	PL25A	6	T	LLM0_PLLT_IN_A	PL29A	6	T	LLM0_PLLT_IN_A	PL33A	6	T	LLM0_PLLT_IN_A
T2	PL25B	6	C	LLM0_PLLC_IN_A	PL29B	6	C	LLM0_PLLC_IN_A	PL33B	6	C	LLM0_PLLC_IN_A
V1	PL26A	6	T[3]	-	PL30A	6	T[3]	-	PL34A	6	T[3]	-
U2	PL26B	6	C[3]	-	PL30B	6	C[3]	-	PL34B	6	C[3]	-
W1	PL28A	6	T[3]	-	PL32A	6	T[3]	-	PL36A	6	T[3]	-
V2	PL28B	6	C[3]	-	PL32B	6	C[3]	-	PL36B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	-	-	-	GNDIO6	6	-	-
P3	PL29A	6	T	-	PL33A	6	T	-	PL37A	6	T	-
P4	PL29B	6	C	-	PL33B	6	C	-	PL37B	6	C	-
Y1	PL30A	6	T[3]	-	PL34A	6	T[3]	-	PL38A	6	T[3]	-
W2	PL30B	6	C[3]	-	PL34B	6	C[3]	-	PL38B	6	C[3]	-
R3	PL31A	6	-	VREF2_6	PL35A	6	-	VREF2_6	PL39A	6	-	VREF2_6
R4	PL32B	6	-	-	PL36B	6	-	-	PL40B	6	-	-
T3	PL33A	6	T[3]	DQS	PL37A	6	T[3]	DQS	PL41A	6	T[3]	DQS
T4	PL33B	6	C[3]	-	PL37B	6	C[3]	-	PL41B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
V4	PL34A	6	T	LLM0_PLLT_FB_A	PL38A	6	T	LLM0_PLLT_FB_A	PL42A	6	T	LLM0_PLLT_FB_A
V3	PL34B	6	C	LLM0_PLLC_FB_A	PL38B	6	C	LLM0_PLLC_FB_A	PL42B	6	C	LLM0_PLLC_FB_A
U4	PL35A	6	T[3]	-	PL39A	6	T[3]	-	PL43A	6	T[3]	-
U3	PL35B	6	C[3]	-	PL39B	6	C[3]	-	PL43B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
W5	SLEEPN[1]/ TOE[2]	-	-	-	SLEEPN[1]/ TOE[2]	-	-	-	SLEEPN[1]/ TOE[2]	-	-	-
Y2	INITN	5	-	-	INITN	5	-	-	INITN	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y3	-	-	-	-	PB3B	5	-	-	PB7B	5	-	-
W3	-	-	-	-	PB4A	5	T	-	PB8A	5	T	-
W4	-	-	-	-	PB4B	5	C	-	PB8B	5	C	-
AA2	-	-	-	-	PB5A	5	-	-	PB9A	5	-	-
AA1	-	-	-	-	PB6B	5	-	-	PB10B	5	-	-
W6	PB2A	5	-	-	PB7A	5	T	DQS	PB11A	5	T	DQS
W7	-	-	-	-	PB7B	5	C	-	PB11B	5	C	-
Y4	PB3A	5	T	-	PB8A	5	T	-	PB12A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y5	PB3B	5	C	-	PB8B	5	C	-	PB12B	5	C	-
AB2	PB4A	5	T	-	PB9A	5	T	-	PB13A	5	T	-
AA3	PB4B	5	C	-	PB9B	5	C	-	PB13B	5	C	-
AB3	PB5A	5	T	-	PB10A	5	T	-	PB14A	5	T	-
AA4	PB5B	5	C	-	PB10B	5	C	-	PB14B	5	C	-
W8	PB6A	5	T	-	PB11A	5	T	-	PB15A	5	T	-
W9	PB6B	5	C	-	PB11B	5	C	-	PB15B	5	C	-
AB4	PB7A	5	T	VREF1_5	PB12A	5	T	VREF1_5	PB16A	5	T	VREF1_5
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
AA5	PB7B	5	C	-	PB12B	5	C	-	PB16B	5	C	-
AB5	PB8A	5	-	-	PB13A	5	-	-	PB17A	5	-	-
Y6	PB9B	5	-	-	PB14B	5	-	-	PB18B	5	-	-
AA6	PB10A	5	T	DQS	PB15A	5	T	DQS	PB19A	5	T	DQS
AB6	PB10B	5	C	-	PB15B	5	C	-	PB19B	5	C	-
Y9	PB11A	5	T	-	PB16A	5	T	-	PB20A	5	T	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
M21	VCCP1	-	-	-	VCCP1	-	-	-	VCCP1	-	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
M22	PR18B	2	C[3]	-	PR22B	2	C[3]	-	PR22B	2	C[3]	-
L22	PR18A	2	T[3]	-	PR22A	2	T[3]	-	PR22A	2	T[3]	-
K22	PR17B	2	C	PCLKC2_0	PR21B	2	C	PCLKC2_0	PR21B	2	C	PCLKC2_0
K21	PR17A	2	T	PCLKT2_0	PR21A	2	T	PCLKT2_0	PR21A	2	T	PCLKT2_0
L19	PR16B	2	C[3]	-	PR20B	2	C[3]	-	PR20B	2	C[3]	-
K20	PR16A	2	T[3]	DQS	PR20A	2	T[3]	DQS	PR20A	2	T[3]	DQS
L20	PR15B	2	-	-	PR19B	2	-	-	PR19B	2	-	-
L21	PR14A	2	-	VREF1_2	PR18A	2	-	VREF1_2	PR18A	2	-	VREF1_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
J22	PR13B	2	C[3]	-	PR17B	2	C[3]	-	PR17B	2	C[3]	-
J21	PR13A	2	T[3]	-	PR17A	2	T[3]	-	PR17A	2	T[3]	-
H22	PR12B	2	C	RUM0_PLLC_IN_A	PR16B	2	C	RUM0_PLLC_IN_A	PR16B	2	C	RUM0_PLLC_IN_A
H21	PR12A	2	T	RUM0_PLLT_IN_A	PR16A	2	T	RUM0_PLLT_IN_A	PR16A	2	T	RUM0_PLLT_IN_A
K19	PR11B	2	C[3]	-	PR15B	2	C[3]	-	PR15B	2	C[3]	-
J19	PR11A	2	T[3]	-	PR15A	2	T[3]	-	PR15A	2	T[3]	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
J20	PR9B	2	C[3]	-	PR13B	2	C[3]	-	PR13B	2	C[3]	-
H20	PR9A	2	T[3]	-	PR13A	2	T[3]	-	PR13A	2	T[3]	-
H19	PR8B	2	C	-	PR12B	2	C	-	PR12B	2	C	-
G19	PR8A	2	T	-	PR12A	2	T	-	PR12A	2	T	-
G22	PR7B	2	C[3]	-	PR11B	2	C[3]	-	PR11B	2	C[3]	-
G21	PR7A	2	T[3]	DQS	PR11A	2	T[3]	DQS	PR11A	2	T[3]	DQS
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
F20	PR6B	2	-	-	PR10B	2	-	-	PR10B	2	-	-
G20	PR5A	2	-	VREF2_2	PR9A	2	-	VREF2_2	PR9A	2	-	VREF2_2
F22	PR4B	2	C[3]	-	PR8B	2	C[3]	-	PR8B	2	C[3]	-
F21	PR4A	2	T[3]	-	PR8A	2	T[3]	-	PR8A	2	T[3]	-
E22	PR3B	2	C	RUM0_PLLC_FB_A	PR7B	2	C	RUM0_PLLC_FB_A	PR7B	2	C	RUM0_PLLC_FB_A
E21	PR3A	2	T	RUM0_PLLT_FB_A	PR7A	2	T	RUM0_PLLT_FB_A	PR7A	2	T	RUM0_PLLT_FB_A
D22	PR2B	2	C[3]	-	PR6B	2	C[3]	-	PR6B	2	C[3]	-
D21	PR2A	2	T[3]	-	PR6A	2	T[3]	-	PR6A	2	T[3]	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
F19	TDO	-	-	-	TDO	-	-	-	TDO	-	-	-
E20	VCCJ	-	-	-	VCCJ	-	-	-	VCCJ	-	-	-
D20	TDI	-	-	-	TDI	-	-	-	TDI	-	-	-
D19	TMS	-	-	-	TMS	-	-	-	TMS	-	-	-
D18	TCK	-	-	-	TCK	-	-	-	TCK	-	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
E19	-	-	-	-	PT48A	1	-	-	PT52A	1	-	-
D17	-	-	-	-	PT47B	1	C	-	PT51B	1	C	-
D16	-	-	-	-	PT47A	1	T	DQS	PT51A	1	T	DQS
C16	-	-	-	-	PT46B	1	-	-	PT50B	1	-	-
C15	-	-	-	-	PT45A	1	-	-	PT49A	1	-	-
C17	-	-	-	-	PT44B	1	C	-	PT48B	1	C	-
C18	PT39A	1	-	-	PT44A	1	T	-	PT48A	1	T	-
C19	PT38B	1	C	-	PT43B	1	C	-	PT47B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
K11	GND	-	-	-	GND	-	-	-	GND	-	-	-
K12	GND	-	-	-	GND	-	-	-	GND	-	-	-
K13	GND	-	-	-	GND	-	-	-	GND	-	-	-
K14	GND	-	-	-	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-	GND	-	-	-
L10	GND	-	-	-	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-	GND	-	-	-
L12	GND	-	-	-	GND	-	-	-	GND	-	-	-
L13	GND	-	-	-	GND	-	-	-	GND	-	-	-
L14	GND	-	-	-	GND	-	-	-	GND	-	-	-
L9	GND	-	-	-	GND	-	-	-	GND	-	-	-
M10	GND	-	-	-	GND	-	-	-	GND	-	-	-
M11	GND	-	-	-	GND	-	-	-	GND	-	-	-
M12	GND	-	-	-	GND	-	-	-	GND	-	-	-
M13	GND	-	-	-	GND	-	-	-	GND	-	-	-
M14	GND	-	-	-	GND	-	-	-	GND	-	-	-
M9	GND	-	-	-	GND	-	-	-	GND	-	-	-
N10	GND	-	-	-	GND	-	-	-	GND	-	-	-
N11	GND	-	-	-	GND	-	-	-	GND	-	-	-
N12	GND	-	-	-	GND	-	-	-	GND	-	-	-
N13	GND	-	-	-	GND	-	-	-	GND	-	-	-
N14	GND	-	-	-	GND	-	-	-	GND	-	-	-
N9	GND	-	-	-	GND	-	-	-	GND	-	-	-
P10	GND	-	-	-	GND	-	-	-	GND	-	-	-
P11	GND	-	-	-	GND	-	-	-	GND	-	-	-
P12	GND	-	-	-	GND	-	-	-	GND	-	-	-
P13	GND	-	-	-	GND	-	-	-	GND	-	-	-
P14	GND	-	-	-	GND	-	-	-	GND	-	-	-
P9	GND	-	-	-	GND	-	-	-	GND	-	-	-
R10	GND	-	-	-	GND	-	-	-	GND	-	-	-
R11	GND	-	-	-	GND	-	-	-	GND	-	-	-
R12	GND	-	-	-	GND	-	-	-	GND	-	-	-
R13	GND	-	-	-	GND	-	-	-	GND	-	-	-
R14	GND	-	-	-	GND	-	-	-	GND	-	-	-
H9	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
J15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
J8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
K15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
K8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
L15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
L8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
M15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
M8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
N15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
N8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
P15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
P8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
R9	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
G16	VCCAUX	-	-	-	VCCAUX	-	-	-	VCCAUX	-	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
D18	-	-	-	-	PT55B	1	C	-
E18	-	-	-	-	PT55A	1	T	-
C19	-	-	-	-	PT54B	1	C	-
C18	-	-	-	-	PT54A	1	T	-
C21	-	-	-	-	PT53B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B21	-	-	-	-	PT53A	1	T	-
E17	PT48B	1	C	-	PT52B	1	C	-
E16	PT48A	1	T	-	PT52A	1	T	-
C17	PT47B	1	C	-	PT51B	1	C	-
D17	PT47A	1	T	DQS	PT51A	1	T	DQS
F17	PT46B	1	-	-	PT50B	1	-	-
F16	PT45A	1	-	-	PT49A	1	-	-
C16	PT44B	1	C	-	PT48B	1	C	-
D16	PT44A	1	T	-	PT48A	1	T	-
A20	PT43B	1	C	-	PT47B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B20	PT43A	1	T	-	PT47A	1	T	-
A19	PT42B	1	C	-	PT46B	1	C	-
B19	PT42A	1	T	-	PT46A	1	T	-
C15	PT41B	1	C	-	PT45B	1	C	-
D15	PT41A	1	T	-	PT45A	1	T	-
A18	PT40B	1	C	-	PT44B	1	C	-
B18	PT40A	1	T	-	PT44A	1	T	-
F15	PT39B	1	C	VREF1_1	PT43B	1	C	VREF1_1
-	GNDIO1	1	-	-	GNDIO1	1	-	-
E15	PT39A	1	T	DQS	PT43A	1	T	DQS
A17	PT38B	1	-	-	PT42B	1	-	-
B17	PT37A	1	-	-	PT41A	1	-	-
E14	PT36B	1	C	-	PT40B	1	C	-
F14	PT36A	1	T	-	PT40A	1	T	-
D14	PT35B	1	C	-	PT39B	1	C	-
C14	PT35A	1	T	D0	PT39A	1	T	D0
A16	PT34B	1	C	D1	PT38B	1	C	D1
B16	PT34A	1	T	VREF2_1	PT38A	1	T	VREF2_1
A15	PT33B	1	C	-	PT37B	1	C	-
B15	PT33A	1	T	D2	PT37A	1	T	D2
-	GNDIO1	1	-	-	GNDIO1	1	-	-
E13	PT32B	1	C	D3	PT36B	1	C	D3
D13	PT32A	1	T	-	PT36A	1	T	-
C13	PT31B	1	C	-	PT35B	1	C	-
B13	PT31A	1	T	DQS	PT35A	1	T	DQS

Commercial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20E-3F484C	340	1.2V	-3	fpBGA	484	COM	19.7K
LFXP20E-4F484C	340	1.2V	-4	fpBGA	484	COM	19.7K
LFXP20E-5F484C	340	1.2V	-5	fpBGA	484	COM	19.7K
LFXP20E-3F388C	268	1.2V	-3	fpBGA	388	COM	19.7K
LFXP20E-4F388C	268	1.2V	-4	fpBGA	388	COM	19.7K
LFXP20E-5F388C	268	1.2V	-5	fpBGA	388	COM	19.7K
LFXP20E-3F256C	188	1.2V	-3	fpBGA	256	COM	19.7K
LFXP20E-4F256C	188	1.2V	-4	fpBGA	256	COM	19.7K
LFXP20E-5F256C	188	1.2V	-5	fpBGA	256	COM	19.7K

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3C-3Q208I	136	1.8/2.5/3.3V	-3	PQFP	208	IND	3.1K
LFXP3C-4Q208I	136	1.8/2.5/3.3V	-4	PQFP	208	IND	3.1K
LFXP3C-3T144I	100	1.8/2.5/3.3V	-3	TQFP	144	IND	3.1K
LFXP3C-4T144I	100	1.8/2.5/3.3V	-4	TQFP	144	IND	3.1K
LFXP3C-3T100I	62	1.8/2.5/3.3V	-3	TQFP	100	IND	3.1K
LFXP3C-4T100I	62	1.8/2.5/3.3V	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6C-3F256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	5.8K
LFXP6C-4F256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	5.8K
LFXP6C-3Q208I	142	1.8/2.5/3.3V	-3	PQFP	208	IND	5.8K
LFXP6C-4Q208I	142	1.8/2.5/3.3V	-4	PQFP	208	IND	5.8K
LFXP6C-3T144I	100	1.8/2.5/3.3V	-3	TQFP	144	IND	5.8K
LFXP6C-4T144I	100	1.8/2.5/3.3V	-4	TQFP	144	IND	5.8K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10C-3F388I	244	1.8/2.5/3.3V	-3	fpBGA	388	IND	9.7K
LFXP10C-4F388I	244	1.8/2.5/3.3V	-4	fpBGA	388	IND	9.7K
LFXP10C-3F256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	9.7K
LFXP10C-4F256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	9.7K

Commercial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20C-3FN484C	340	1.8/2.5/3.3V	-3	fpBGA	484	COM	19.7K
LFXP20C-4FN484C	340	1.8/2.5/3.3V	-4	fpBGA	484	COM	19.7K
LFXP20C-5FN484C	340	1.8/2.5/3.3V	-5	fpBGA	484	COM	19.7K
LFXP20C-3FN388C	268	1.8/2.5/3.3V	-3	fpBGA	388	COM	19.7K
LFXP20C-4FN388C	268	1.8/2.5/3.3V	-4	fpBGA	388	COM	19.7K
LFXP20C-5FN388C	268	1.8/2.5/3.3V	-5	fpBGA	388	COM	19.7K
LFXP20C-3FN256C	188	1.8/2.5/3.3V	-3	fpBGA	256	COM	19.7K
LFXP20C-4FN256C	188	1.8/2.5/3.3V	-4	fpBGA	256	COM	19.7K
LFXP20C-5FN256C	188	1.8/2.5/3.3V	-5	fpBGA	256	COM	19.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3E-3QN208C	136	1.2V	-3	PQFP	208	COM	3.1K
LFXP3E-4QN208C	136	1.2V	-4	PQFP	208	COM	3.1K
LFXP3E-5QN208C	136	1.2V	-5	PQFP	208	COM	3.1K
LFXP3E-3TN144C	100	1.2V	-3	TQFP	144	COM	3.1K
LFXP3E-4TN144C	100	1.2V	-4	TQFP	144	COM	3.1K
LFXP3E-5TN144C	100	1.2V	-5	TQFP	144	COM	3.1K
LFXP3E-3TN100C	62	1.2V	-3	TQFP	100	COM	3.1K
LFXP3E-4TN100C	62	1.2V	-4	TQFP	100	COM	3.1K
LFXP3E-5TN100C	62	1.2V	-5	TQFP	100	COM	3.1K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6E-3FN256C	188	1.2V	-3	fpBGA	256	COM	5.8K
LFXP6E-4FN256C	188	1.2V	-4	fpBGA	256	COM	5.8K
LFXP6E-5FN256C	188	1.2V	-5	fpBGA	256	COM	5.8K
LFXP6E-3QN208C	142	1.2V	-3	PQFP	208	COM	5.8K
LFXP6E-4QN208C	142	1.2V	-4	PQFP	208	COM	5.8K
LFXP6E-5QN208C	142	1.2V	-5	PQFP	208	COM	5.8K
LFXP6E-3TN144C	100	1.2V	-3	TQFP	144	COM	5.8K
LFXP6E-4TN144C	100	1.2V	-4	TQFP	144	COM	5.8K
LFXP6E-5TN144C	100	1.2V	-5	TQFP	144	COM	5.8K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10E-3FN388C	244	1.2V	-3	fpBGA	388	COM	9.7K
LFXP10E-4FN388C	244	1.2V	-4	fpBGA	388	COM	9.7K
LFXP10E-5FN388C	244	1.2V	-5	fpBGA	388	COM	9.7K
LFXP10E-3FN256C	188	1.2V	-3	fpBGA	256	COM	9.7K
LFXP10E-4FN256C	188	1.2V	-4	fpBGA	256	COM	9.7K
LFXP10E-5FN256C	188	1.2V	-5	fpBGA	256	COM	9.7K

Commercial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15E-3FN484C	300	1.2V	-3	fpBGA	484	COM	15.5K
LFXP15E-4FN484C	300	1.2V	-4	fpBGA	484	COM	15.5K
LFXP15E-5FN484C	300	1.2V	-5	fpBGA	484	COM	15.5K
LFXP15E-3FN388C	268	1.2V	-3	fpBGA	388	COM	15.5K
LFXP15E-4FN388C	268	1.2V	-4	fpBGA	388	COM	15.5K
LFXP15E-5FN388C	268	1.2V	-5	fpBGA	388	COM	15.5K
LFXP15E-3FN256C	188	1.2V	-3	fpBGA	256	COM	15.5K
LFXP15E-4FN256C	188	1.2V	-4	fpBGA	256	COM	15.5K
LFXP15E-5FN256C	188	1.2V	-5	fpBGA	256	COM	15.5K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20E-3FN484C	340	1.2V	-3	fpBGA	484	COM	19.7K
LFXP20E-4FN484C	340	1.2V	-4	fpBGA	484	COM	19.7K
LFXP20E-5FN484C	340	1.2V	-5	fpBGA	484	COM	19.7K
LFXP20E-3FN388C	268	1.2V	-3	fpBGA	388	COM	19.7K
LFXP20E-4FN388C	268	1.2V	-4	fpBGA	388	COM	19.7K
LFXP20E-5FN388C	268	1.2V	-5	fpBGA	388	COM	19.7K
LFXP20E-3FN256C	188	1.2V	-3	fpBGA	256	COM	19.7K
LFXP20E-4FN256C	188	1.2V	-4	fpBGA	256	COM	19.7K
LFXP20E-5FN256C	188	1.2V	-5	fpBGA	256	COM	19.7K

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3C-3QN208I	136	1.8/2.5/3.3V	-3	PQFP	208	IND	3.1K
LFXP3C-4QN208I	136	1.8/2.5/3.3V	-4	PQFP	208	IND	3.1K
LFXP3C-3TN144I	100	1.8/2.5/3.3V	-3	TQFP	144	IND	3.1K
LFXP3C-4TN144I	100	1.8/2.5/3.3V	-4	TQFP	144	IND	3.1K
LFXP3C-3TN100I	62	1.8/2.5/3.3V	-3	TQFP	100	IND	3.1K
LFXP3C-4TN100I	62	1.8/2.5/3.3V	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6C-3FN256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	5.8K
LFXP6C-4FN256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	5.8K
LFXP6C-3QN208I	142	1.8/2.5/3.3V	-3	PQFP	208	IND	5.8K
LFXP6C-4QN208I	142	1.8/2.5/3.3V	-4	PQFP	208	IND	5.8K
LFXP6C-3TN144I	100	1.8/2.5/3.3V	-3	TQFP	144	IND	5.8K
LFXP6C-4TN144I	100	1.8/2.5/3.3V	-4	TQFP	144	IND	5.8K

LatticeXP Family Data Sheet Supplemental Information

November 2007 Data Sheet DS1001

For Further Information

A variety of technical notes for the LatticeXP family are available on the Lattice website at www.latticesemi.com.

- LatticeECP/EC and LatticeXP sysIO Usage Guide (TN1056)
- Lattice ispTRACY Usage Guide (TN1054)
- LatticeECP/EC and LatticeXP sysCLOCK PLL Design and Usage Guide (TN1049)
- Memory Usage Guide for LatticeECP/EC and LatticeXP Devices (TN1051)
- LatticeECP/EC and XP DDR Usage Guide (TN1050)
- Power Estimation and Management for LatticeECP/EC and LatticeXP Devices (TN1052)
- LatticeXP sysCONFIG Usage Guide (TN1082)

For further information on interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com