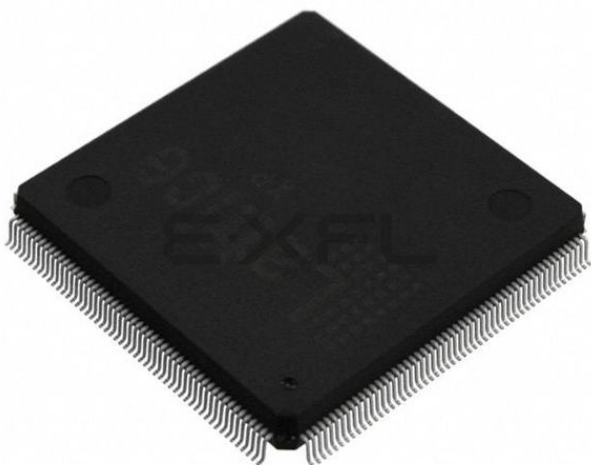




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

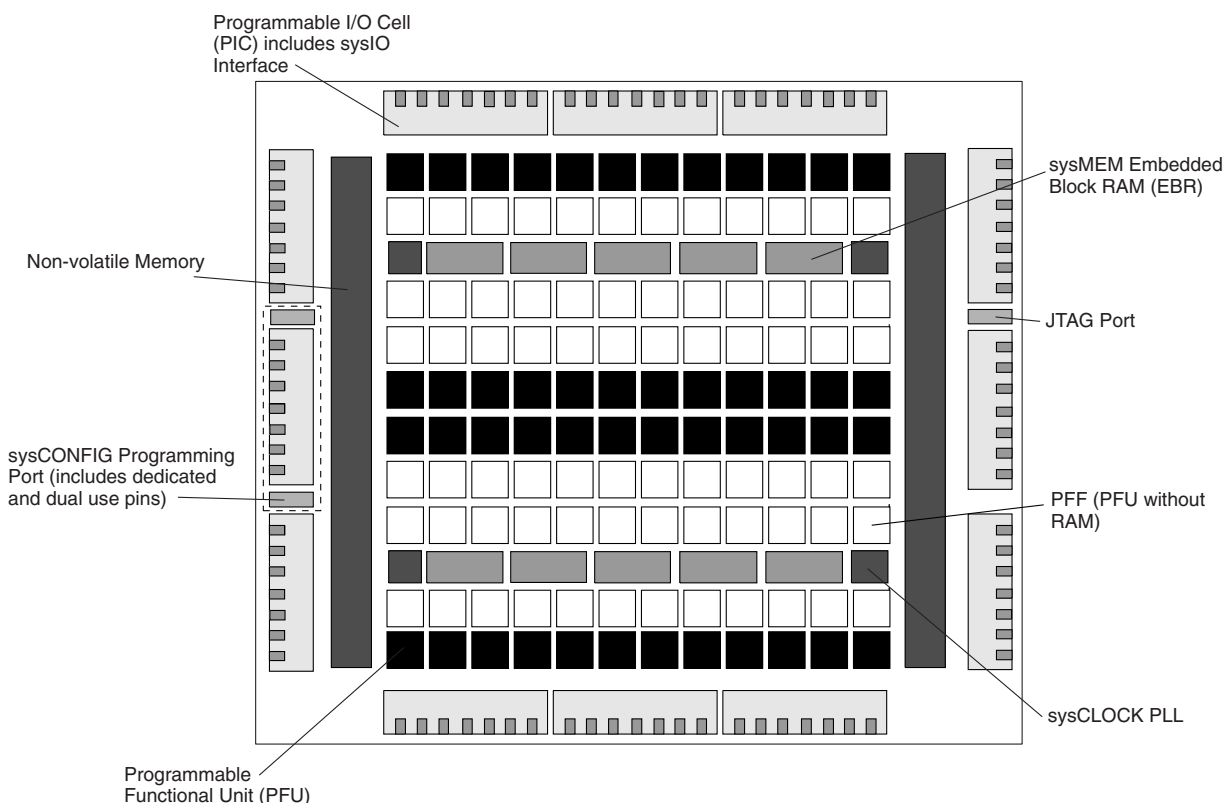
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	3000
Total RAM Bits	55296
Number of I/O	136
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp3c-4qn208c

Figure 2-1. LatticeXP Top Level Block Diagram

PFU and PFF Blocks

The core of the LatticeXP devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of the data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-2. All the interconnections to and from PFU blocks are from routing. There are 53 inputs and 25 outputs associated with each PFU block.

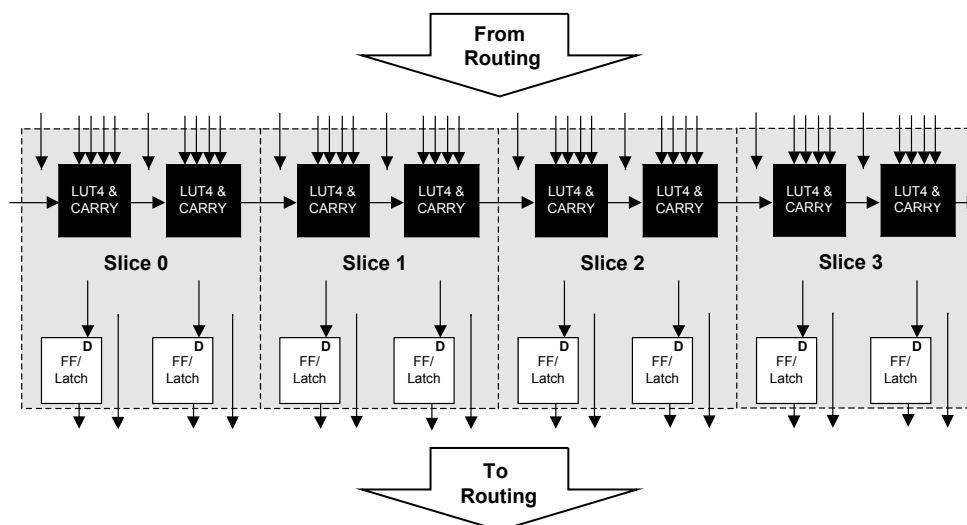
Figure 2-2. PFU Diagram

Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In ¹
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output ¹

1. See Figure 2-2 for connection details.

2. Requires two PFUs.

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SP 16x2	ROM 16x1 x 2
PFF Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	N/A	ROM 16x1 x 2

Logic Mode: In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other Slices.

Ripple Mode: Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Two additional signals: Carry Generate and Carry Propagate are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode: In this mode, distributed RAM can be constructed using each LUT block as a 16x1-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

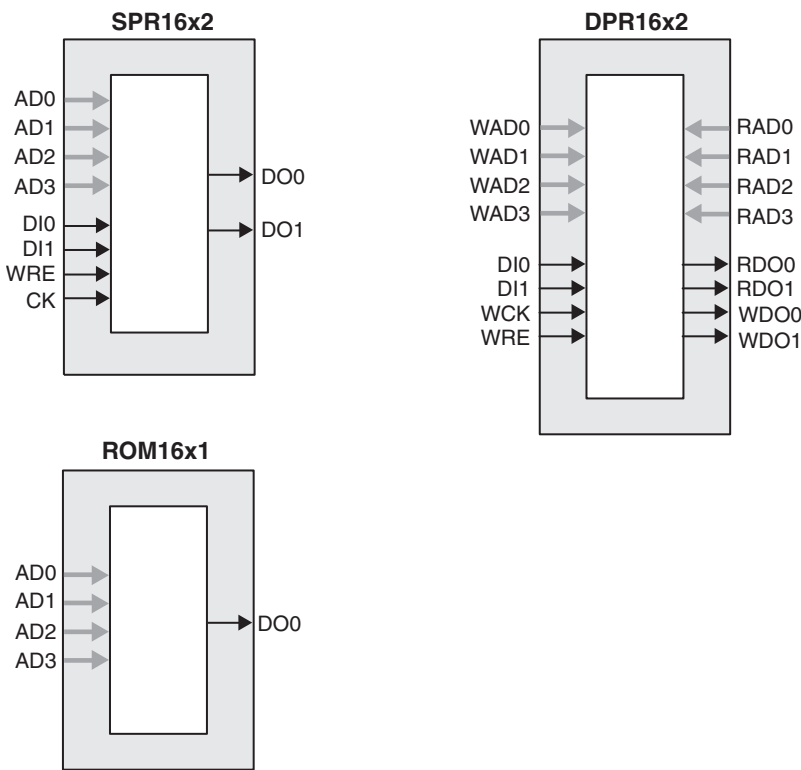
The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-4 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices, one Slice functions as the read-write port. The other companion Slice supports the read-only port. For more information on RAM mode in LatticeXP devices, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required for Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of Slices	1	2

Note: SPR = Single Port RAM, DPR = Dual Port RAM

Figure 2-4. Distributed Memory Primitives

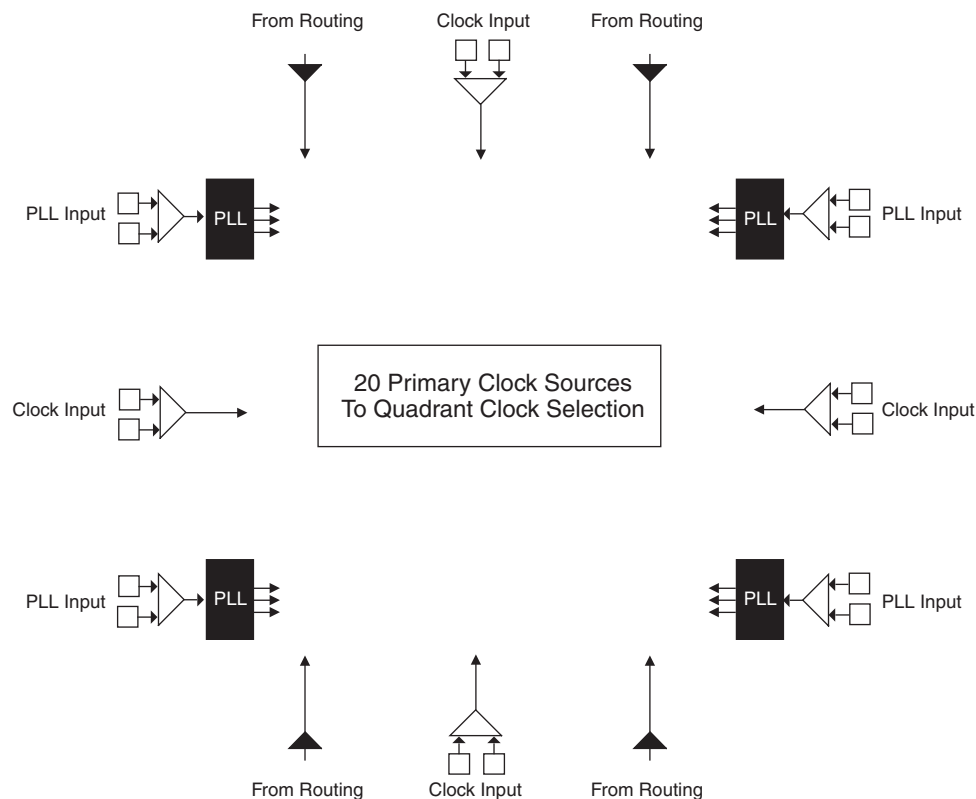


ROM Mode: The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

Figure 2-5. Primary Clock Sources

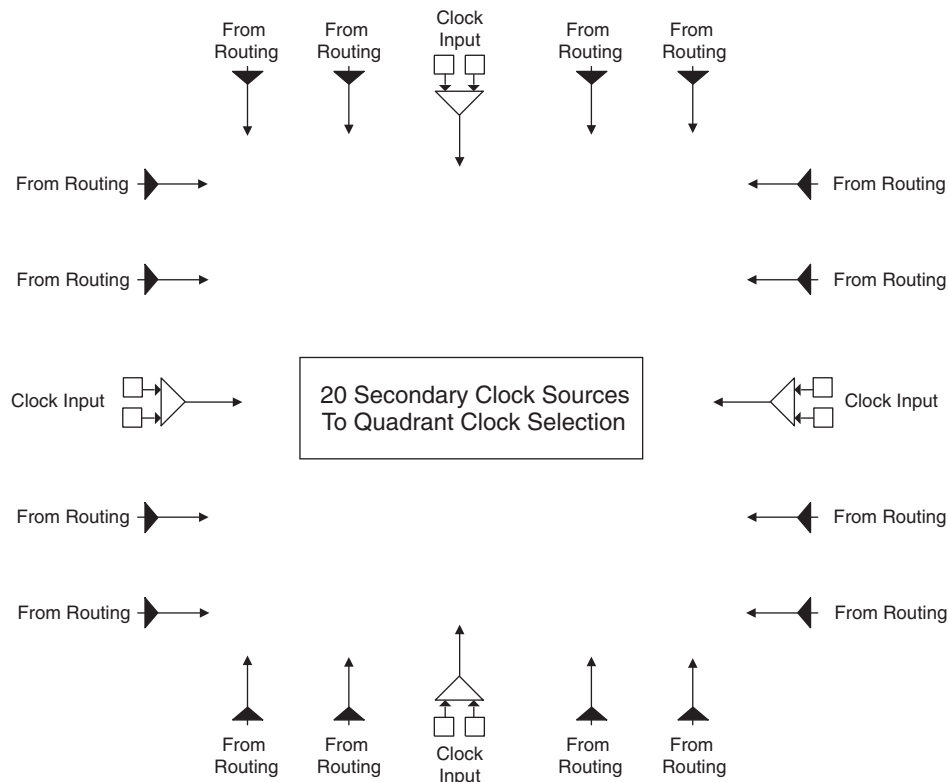


Note: Smaller devices have two PLLs.

Secondary Clock Sources

LatticeXP devices have four secondary clock resources per quadrant. The secondary clock branches are tapped at every PFU. These secondary clock networks can also be used for controls and high fanout data. These secondary clocks are derived from four clock input pads and 16 routing signals as shown in Figure 2-6.

Figure 2-6. Secondary Clock Sources



Clock Routing

The clock routing structure in LatticeXP devices consists of four Primary Clock lines and a Secondary Clock network per quadrant. The primary clocks are generated from MUXs located in each quadrant. Figure 2-7 shows this clock routing. The four secondary clocks are generated from MUXs located in each quadrant as shown in Figure 2-8. Each slice derives its clock from the primary clock lines, secondary clock lines and routing as shown in Figure 2-9.

Figure 2-7. Per Quadrant Primary Clock Selection

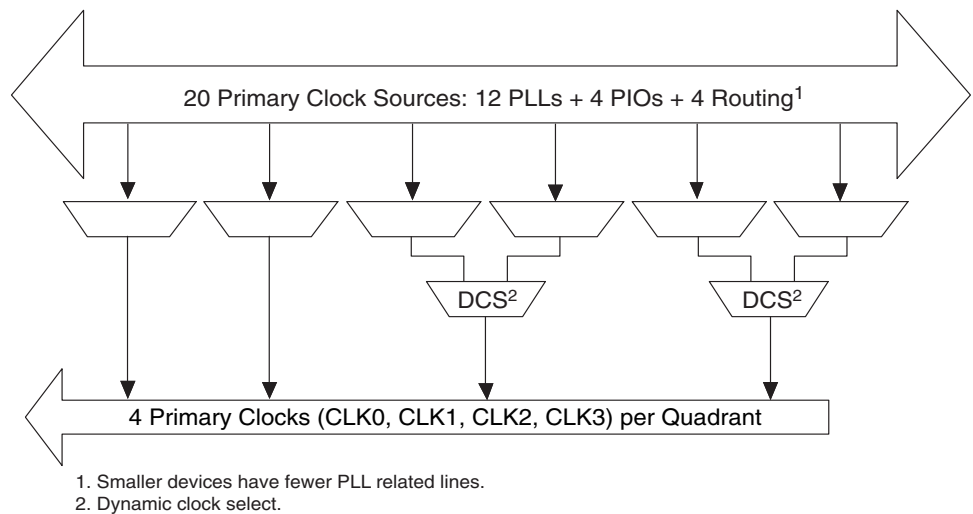
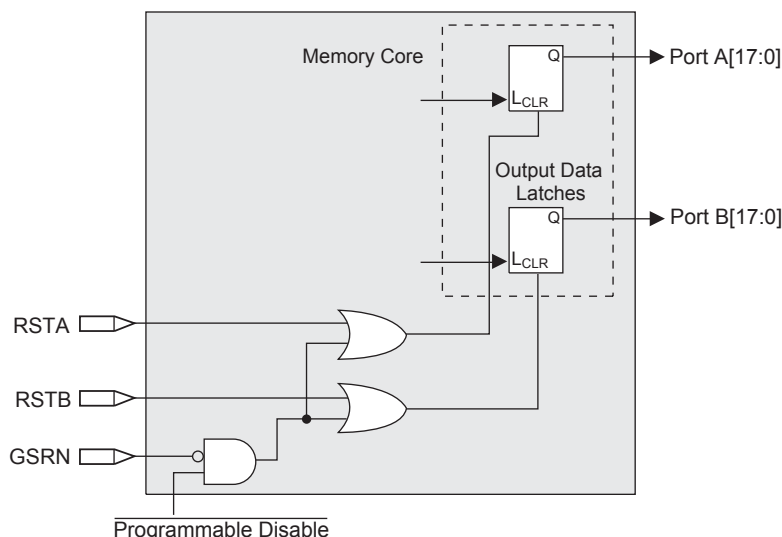
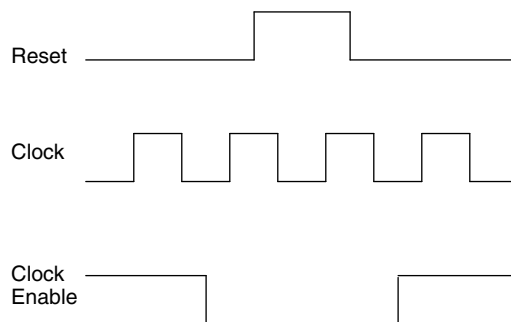


Figure 2-15. Memory Core Reset

For further information on sysMEM EBR block, see the details of additional technical documentation at the end of this data sheet.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-16. The GSR input to the EBR is always asynchronous.

Figure 2-16. EBR Asynchronous Reset (Including GSR) Timing Diagram

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

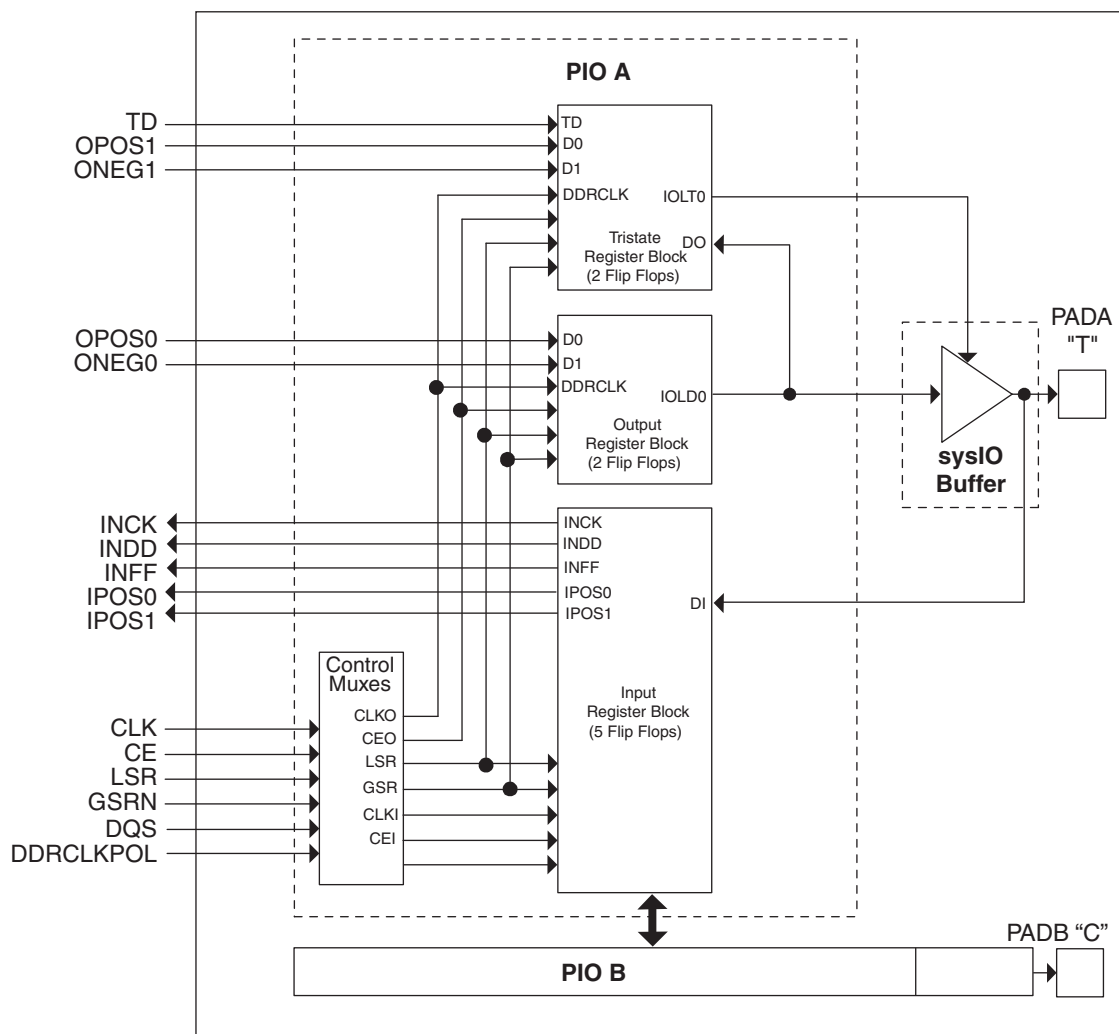
These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

Programmable I/O Cells (PICs)

Each PIC contains two PIOs connected to their respective sysIO Buffers which are then connected to the PADs as shown in Figure 2-17. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to sysIO buffer, and receives input from the buffer.

Figure 2-17. PIC Diagram



In the LatticeXP family, seven PIOs or four (3.5) PICs are grouped together to provide two LVDS differential pairs, one PIC pair and one single I/O, as shown in Figure 2-18.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”). The PAD Labels “T” and “C” distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 14 PIOs (a group of 8 PICs) contains a delay element to facilitate the generation of DQS signals as shown in Figure 2-19. The DQS signal feeds the DQS bus which spans the set of 13 PIOs (8 PICs). The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table in this data sheet.

Initialization Supply Current^{1, 2, 3, 4, 5, 6}**Over Recommended Operating Conditions**

Symbol	Parameter	Device	Typ. ⁷	Units
I_{CC}	Core Power Supply	LFXP3E	40	mA
		LFXP6E	50	mA
		LFXP10E	110	mA
		LFXP15E	140	mA
		LFXP20E	250	mA
		LFXP3C	60	mA
		LFXP6C	70	mA
		LFXP10C	150	mA
		LFXP15C	180	mA
		LFXP20C	290	mA
I_{CCAUX}	Auxiliary Power Supply $V_{CCAUX} = 3.3V$	LFXP3E/C	50	mA
		LFXP6E/C	60	mA
		LFXP10E/C	90	mA
		LFXP15 /C	110	mA
		LFXP20E/C	130	mA
I_{CCJ}	V_{CCJ} Power Supply	All	2	mA

1. Until DONE signal is active.

2. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.

3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

4. Frequency 0MHz.

5. Typical user pattern.

6. Assume normal bypass capacitor/decoupling capacitor across the supply.

7. $T_A=25^{\circ}C$, power supplies at nominal voltage.

Power Supply and NC Connections

Signals	100 TQFP	144 TQFP	208 PQFP	256 fpBGA	388 fpBGA	484 fpBGA
V _{CC}	28, 77	14, 39, 73, 112	19, 35, 53, 80, 107, 151, 158, 182	D4, D13, E5, E12, M5, M12, N4, N13	H9, J8, J15, K8, K15, L8, L15, M8, M15, N8, N15, P8, P15, R9	F10, F13, G9, G10, G13, G14, H8, H15, J7, J16, K6, K7, K16, K17, N6, N7, N16, N17, P7, P16, R8, R15, T9, T10, T13, T14, U10, U13
V _{CCIO0}	94	133	189, 199	F7, F8	G8, G9, G10, G11, H8	F11, G11, H10, H11
V _{CCIO1}	82	119	167, 177	F9, F10	G12, G13, G14, G15, H15	F12, G12, H12, H13
V _{CCIO2}	65	98	140, 149	G11, H11	H16, J16, K16, L16	K15, L15, L16, L17
V _{CCIO3}	58	88	115, 125	J11, K11	M16, N16, P16, R16	M15, M16, M17, N15
V _{CCIO4}	47	61, 68	87, 97	L9, L10	R15, T12, T13, T14, T15	R12, R13, T12, U12
V _{CCIO5}	38	49	64, 74	L7, L8	R8, T8, T9, T10, T11	R10, R11, T11, U11
V _{CCIO6}	22	21	28, 41	J6, K6	M7, N7, P7, R7	M6, M7, M8, N8
V _{CCIO7}	7	8	13, 23	G6, H6	H7, J7, K7, L7	K8, L6, L7, L8
V _{CCJ}	73	108	154	D16	E20	E20
V _{CCP0}	17	19	25	H4	M2	L5
V _{CCP1}	60	91	128	J12	M21	L18
V _{CCAUX}	25, 71	36, 106	50, 152	E4, E13, M4, M13	G7, G16, T7, T16	G7, G8, G15, G16, H7, H16, R7, R16, T7, T8, T15, T16
GND ¹	10, 18, 21, 33, 43, 44, 52, 59, 68, 84, 90, 99	3, 11, 20, 28, 44, 54, 56, 64, 75, 85, 90, 101, 121, 127, 136	5, 7, 16, 26, 38, 47, 49, 59, 69, 79, 82, 92, 106, 109, 118, 121, 127, 130, 135, 143, 163, 172, 181, 184, 194, 207	A1, A16, F6, F11, G7, G8, G9, G10, H5, H7, H8, H9, H10, J7, J8, J9, J10, J13, K7, K8, K9, K10, L6, L11, T1, T16	A1, A22, H10, H11, H12, H13, H14, J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N1, N9, N10, N11, N12, N13, N14, N22, P9, P10, P11, P12, P13, P14, R10, R11, R12, R13, R14, AB1, AB22	A1, A2, A21, A22, B1, B22, H9, H14, J8, J9, J10, J11, J12, J13, J14, J15, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, M20, N2, N9, N10, N11, N12, N13, N14, P8, P9, P10, P11, P12, P13, P14, P15, R9, R14, AA1, AA22, AB1, AB2, AB21, AB22
NC ²	—	—	XP3: 27, 33, 34, 129, 133, 134	—	XP10: C2, C15, C16, C17, D4, D5, D6, D7, D16, D17, E4, E19, W3, W4, W7, W17, W18, W19, W20, Y3, Y15, Y16, AA1, AA2	XP15: B21, C4, C5, C6, C18, C19, C20, C21, D6, D18, E4, E6, E18, F6, L1, L19, L20, M1, M2, M19, M21, N1, N21, N22, P1, P2, U5, U6, U17, U18, V5, V6, V17, V18, W17, W18, W19, Y3, Y4, Y5

1. All grounds must be electrically connected at the board level.

2. NC pins should not be connected to any active signals, V_{CC} or GND.

LFXP3 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	Pin Function	Bank	Differential	Dual Function
44	GNDIO4	4	-	-
45	PB15A	4	T	PCLKT4_0
46	PB15B	4	C	PCLKC4_0
47	VCCIO4	4	-	-
48	PB19A	4	T	DQS
49	PB19B	4	C	VREF1_4
50	PB24A	4	-	VREF2_4
51	PR18B	3	C ³	-
52	GNDIO3	3	-	-
53	PR18A	3	T ³	-
54	PR15B	3	-	VREF1_3
55	PR14A	3	-	VREF2_3
56	PR13B	3	C	-
57	PR13A	3	T	-
58	VCCIO3	3	-	-
59	GNDP1	-	-	-
60	VCCP1	-	-	-
61	PR9B	2	C	PCLKC2_0
62	PR9A	2	T	PCLKT2_0
63	PR8B	2	C	RUM0_PLLC_IN_A
64	PR8A	2	T	RUM0_PLLT_IN_A
65	VCCIO2	2	-	-
66	PR6B	2	-	VREF1_2
67	PR5A	2	-	VREF2_2
68	GNDIO2	2	-	-
69	PR3B	2	C	RUM0_PLLC_FB_A
70	PR3A	2	T	RUM0_PLLT_FB_A
71	VCCAUX	-	-	-
72	TDO	-	-	-
73	VCCJ	-	-	-
74	TDI	-	-	-
75	TMS	-	-	-
76	TCK	-	-	-
77	VCC	-	-	-
78	PT24A	1	-	-
79	PT23A	1	-	D0
80	PT22B	1	-	D1
81	PT21A	1	-	D2
82	VCCIO1	1	-	-
83	PT20B	1	-	D3
84	GNDIO1	1	-	-
85	PT17A	1	-	D4
86	PT16A	1	-	D5
87	PT15B	1	-	D6

LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
1	PROGRAMN	7	-	-	PROGRAMN	7	-	-
2	CCLK	7	-	-	CCLK	7	-	-
3	GND	-	-	-	GND	-	-	-
4	PL2A	7	T ³	-	PL2A	7	T ³	-
5	PL2B	7	C ³	-	PL2B	7	C ³	-
6	PL3A	7	T	LUM0_PLLT_FB_A	PL3A	7	T	LUM0_PLLT_FB_A
7	PL3B	7	C	LUM0_PLLC_FB_A	PL3B	7	C	LUM0_PLLC_FB_A
8	VCCIO7	7	-	-	VCCIO7	7	-	-
9	PL5A	7	-	VREF1_7	PL5A	7	-	VREF1_7
10	PL6B	7	-	VREF2_7	PL6B	7	-	VREF2_7
11	GNDIO7	7	-	-	GNDIO7	7	-	-
12	PL7A	7	T ³	DQS	PL7A	7	T ³	DQS
13	PL7B	7	C ³	-	PL7B	7	C ³	-
14	VCC	-	-	-	VCC	-	-	-
15	PL8A	7	T	LUM0_PLLT_IN_A	PL8A	7	T	LUM0_PLLT_IN_A
16	PL8B	7	C	LUM0_PLLC_IN_A	PL8B	7	C	LUM0_PLLC_IN_A
17	PL9A	7	T ³	-	PL9A	7	T ³	-
18	PL9B	7	C ³	-	PL9B	7	C ³	-
19	VCCP0	-	-	-	VCCP0	-	-	-
20	GNDP0	-	-	-	GNDP0	-	-	-
21	VCCIO6	6	-	-	VCCIO6	6	-	-
22	PL11A	6	T ³	-	PL16A	6	T ³	-
23	PL11B	6	C ³	-	PL16B	6	C ³	-
24	PL12A	6	T	PCLKT6_0	PL17A	6	T	PCLKT6_0
25	PL12B	6	C	PCLKC6_0	PL17B	6	C	PCLKC6_0
26	PL13A	6	T ³	-	PL18A	6	T ³	-
27	PL13B	6	C ³	-	PL18B	6	C ³	-
28	GNDIO6	6	-	-	GNDIO6	6	-	-
29	PL14A	6	-	VREF1_6	PL22A	6	-	VREF1_6
30	PL15B	6	-	VREF2_6	PL23B	6	-	VREF2_6
31	PL16A	6	T ³	DQS	PL24A	6	T ³	DQS
32	PL16B	6	C ³	-	PL24B	6	C ³	-
33	PL17A	6	-	-	PL25A	6	-	-
34	PL18A	6	T ³	-	PL26A	6	T ³	-
35	PL18B	6	C ³	-	PL26B	6	C ³	-
36	VCCAUX	-	-	-	VCCAUX	-	-	-
37	SLEEPN ¹ /TOE ²	-	-	-	SLEEPN ¹ /TOE ²	-	-	-
38	INITN	5	-	-	INITN	5	-	-
39	VCC	-	-	-	VCC	-	-	-
40	PB2B	5	-	VREF1_5	PB5B	5	-	VREF1_5
41	PB5B	5	-	VREF2_5	PB8B	5	-	VREF2_5
42	PB7A	5	T	-	PB10A	5	T	-
43	PB7B	5	C	-	PB10B	5	C	-
44	GNDIO5	5	-	-	GNDIO5	5	-	-
45	PB9A	5	-	-	PB12A	5	-	-
46	PB10B	5	-	-	PB13B	5	-	-

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP6				LFXP10			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
K4	PL20A	6	T	-	PL29A	6	T	-
K5	PL20B	6	C	-	PL29B	6	C	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
N1	PL23B	6	-	VREF2_6	PL31A	6	-	VREF2_6
N2	PL21B	6	C ³	-	PL32B	6	-	-
P1	PL24A	6	T ³	DQS	PL33A	6	T ³	DQS
P2	PL24B	6	C ³	-	PL33B	6	C ³	-
L5	PL25A	6	T	-	PL34A	6	T	LLM0_PLLT_FB_A
M6	PL25B	6	C	-	PL34B	6	C	LLM0_PLLC_FB_A
M3	PL26A	6	T ³	-	PL35A	6	T ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
N3	PL26B	6	C ³	-	PL35B	6	C ³	-
P4	SLEEPN ¹ /TOE ²	-	-	-	SLEEPN ¹ /TOE ²	-	-	-
P3	INITN	5	-	-	INITN	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
R4	PB2A	5	T	-	PB6A	5	T	-
N5	PB2B	5	C	-	PB6B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
P5	PB5B	5	-	VREF1_5	PB7A	5	T	VREF1_5
R1	PB3B	5	C	-	PB7B	5	C	-
N6	PB4A	5	-	-	PB8A	5	-	-
M7	PB3A	5	T	-	PB9B	5	-	-
R2	PB6A	5	T	DQS	PB10A	5	T	DQS
T2	PB6B	5	C	-	PB10B	5	C	-
R3	PB7A	5	T	-	PB11A	5	T	-
T3	PB7B	5	C	-	PB11B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
T4	PB8A	5	T	-	PB12A	5	T	-
R5	PB8B	5	C	VREF2_5	PB12B	5	C	VREF2_5
N7	PB9A	5	T	-	PB13A	5	T	-
M8	PB9B	5	C	-	PB13B	5	C	-
T5	PB10A	5	T	-	PB14A	5	T	-
P6	PB10B	5	C	-	PB14B	5	C	-
T6	PB11A	5	T	-	PB15A	5	T	-
R6	PB11B	5	C	-	PB15B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
P7	PB12A	5	-	-	PB16A	5	-	-
N8	PB13B	5	-	-	PB17B	5	-	-
R7	PB14A	5	T	DQS	PB18A	5	T	DQS
T7	PB14B	5	C	-	PB18B	5	C	-
P8	PB15A	5	T	-	PB19A	5	T	-
T8	PB15B	5	C	-	PB19B	5	C	-

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
G10	GND	-	-	-	GND	-	-	-
G7	GND	-	-	-	GND	-	-	-
G8	GND	-	-	-	GND	-	-	-
G9	GND	-	-	-	GND	-	-	-
H10	GND	-	-	-	GND	-	-	-
H7	GND	-	-	-	GND	-	-	-
H8	GND	-	-	-	GND	-	-	-
H9	GND	-	-	-	GND	-	-	-
J10	GND	-	-	-	GND	-	-	-
J7	GND	-	-	-	GND	-	-	-
J8	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-
K10	GND	-	-	-	GND	-	-	-
K7	GND	-	-	-	GND	-	-	-
K8	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-
L6	GND	-	-	-	GND	-	-	-
T1	GND	-	-	-	GND	-	-	-
T16	GND	-	-	-	GND	-	-	-
D13	VCC	-	-	-	VCC	-	-	-
D4	VCC	-	-	-	VCC	-	-	-
E12	VCC	-	-	-	VCC	-	-	-
E5	VCC	-	-	-	VCC	-	-	-
M12	VCC	-	-	-	VCC	-	-	-
M5	VCC	-	-	-	VCC	-	-	-
N13	VCC	-	-	-	VCC	-	-	-
N4	VCC	-	-	-	VCC	-	-	-
E13	VCCAUX	-	-	-	VCCAUX	-	-	-
E4	VCCAUX	-	-	-	VCCAUX	-	-	-
M13	VCCAUX	-	-	-	VCCAUX	-	-	-
M4	VCCAUX	-	-	-	VCCAUX	-	-	-
F7	VCCIO0	0	-	-	VCCIO0	0	-	-
F8	VCCIO0	0	-	-	VCCIO0	0	-	-
F10	VCCIO1	1	-	-	VCCIO1	1	-	-
F9	VCCIO1	1	-	-	VCCIO1	1	-	-
G11	VCCIO2	2	-	-	VCCIO2	2	-	-
H11	VCCIO2	2	-	-	VCCIO2	2	-	-
J11	VCCIO3	3	-	-	VCCIO3	3	-	-
K11	VCCIO3	3	-	-	VCCIO3	3	-	-
L10	VCCIO4	4	-	-	VCCIO4	4	-	-
L9	VCCIO4	4	-	-	VCCIO4	4	-	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
C20	PT38A	1	T	-	PT43A	1	T	-	PT47A	1	T	-
C21	PT37B	1	C	-	PT42B	1	C	-	PT46B	1	C	-
C22	PT37A	1	T	-	PT42A	1	T	-	PT46A	1	T	-
B22	PT36B	1	C	-	PT41B	1	C	-	PT45B	1	C	-
A21	PT36A	1	T	-	PT41A	1	T	-	PT45A	1	T	-
D15	PT35B	1	C	-	PT40B	1	C	-	PT44B	1	C	-
D14	PT35A	1	T	-	PT40A	1	T	-	PT44A	1	T	-
B21	PT34B	1	C	VREF1_1	PT39B	1	C	VREF1_1	PT43B	1	C	VREF1_1
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
A20	PT34A	1	T	DQS	PT39A	1	T	DQS	PT43A	1	T	DQS
B20	PT33B	1	-	-	PT38B	1	-	-	PT42B	1	-	-
A19	PT32A	1	-	-	PT37A	1	-	-	PT41A	1	-	-
B19	PT31B	1	C	-	PT36B	1	C	-	PT40B	1	C	-
A18	PT31A	1	T	-	PT36A	1	T	-	PT40A	1	T	-
C14	PT30B	1	C	-	PT35B	1	C	-	PT39B	1	C	-
C13	PT30A	1	T	D0	PT35A	1	T	D0	PT39A	1	T	D0
B18	PT29B	1	C	D1	PT34B	1	C	D1	PT38B	1	C	D1
A17	PT29A	1	T	VREF2_1	PT34A	1	T	VREF2_1	PT38A	1	T	VREF2_1
B17	PT28B	1	C	-	PT33B	1	C	-	PT37B	1	C	-
A16	PT28A	1	T	D2	PT33A	1	T	D2	PT37A	1	T	D2
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
B16	PT27B	1	C	D3	PT32B	1	C	D3	PT36B	1	C	D3
A15	PT27A	1	T	-	PT32A	1	T	-	PT36A	1	T	-
B15	PT26B	1	C	-	PT31B	1	C	-	PT35B	1	C	-
A14	PT26A	1	T	DQS	PT31A	1	T	DQS	PT35A	1	T	DQS
D13	PT25B	1	-	-	PT30B	1	-	-	PT34B	1	-	-
D12	PT24A	1	-	D4	PT29A	1	-	D4	PT33A	1	-	D4
B14	PT23B	1	C	-	PT28B	1	C	-	PT32B	1	C	-
A13	PT23A	1	T	D5	PT28A	1	T	D5	PT32A	1	T	D5
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
B13	PT22B	1	C	D6	PT27B	1	C	D6	PT31B	1	C	D6
A12	PT22A	1	T	-	PT27A	1	T	-	PT31A	1	T	-
B12	PT21B	1	C	D7	PT26B	1	C	D7	PT30B	1	C	D7
C12	PT21A	1	T	-	PT26A	1	T	-	PT30A	1	T	-
C11	PT20B	0	C	BUSY	PT25B	0	C	BUSY	PT29B	0	C	BUSY
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
B11	PT20A	0	T	CS1N	PT25A	0	T	CS1N	PT29A	0	T	CS1N
A11	PT19B	0	C	PCLKC0_0	PT24B	0	C	PCLKC0_0	PT28B	0	C	PCLKC0_0
A10	PT19A	0	T	PCLKT0_0	PT24A	0	T	PCLKT0_0	PT28A	0	T	PCLKT0_0
B10	PT18B	0	C	-	PT23B	0	C	-	PT27B	0	C	-
B9	PT18A	0	T	DQS	PT23A	0	T	DQS	PT27A	0	T	DQS
D11	PT17B	0	-	-	PT22B	0	-	-	PT26B	0	-	-
D10	PT16A	0	-	DOUT	PT21A	0	-	DOUT	PT25A	0	-	DOUT
A9	PT15B	0	C	-	PT20B	0	C	-	PT24B	0	C	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C8	PT15A	0	T	WRITEN	PT20A	0	T	WRITEN	PT24A	0	T	WRITEN
B8	PT14B	0	C	-	PT19B	0	C	-	PT23B	0	C	-
A8	PT14A	0	T	VREF1_0	PT19A	0	T	VREF1_0	PT23A	0	T	VREF1_0
C7	PT13B	0	C	-	PT18B	0	C	-	PT22B	0	C	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L1	-	-	-	-	PL23A	7	T ³	-
M1	-	-	-	-	PL23B	7	C ³	-
M2	-	-	-	-	PL24A	7	-	-
L5	VCCP0	-	-	-	VCCP0	-	-	-
N2	GNDP0	-	-	-	GNDP0	-	-	-
N1	-	-	-	-	PL25B	6	-	-
P2	-	-	-	-	PL26A	6	T ³	-
P1	-	-	-	-	PL26B	6	C ³	-
M4	PL23A	6	T ³	-	PL27A	6	T ³	-
M3	PL23B	6	C ³	-	PL27B	6	C ³	-
R2	PL24A	6	T	PCLKT6_0	PL28A	6	T	PCLKT6_0
-	GNDIO6	6	-	-	GNDIO6	6	-	-
R1	PL24B	6	C	PCLKC6_0	PL28B	6	C	PCLKC6_0
N3	PL25A	6	T ³	-	PL29A	6	T ³	-
N4	PL25B	6	C ³	-	PL29B	6	C ³	-
M5	PL26A	6	-	-	PL30A	6	-	-
N5	PL27B	6	-	VREF1_6	PL31B	6	-	VREF1_6
T2	PL28A	6	T ³	DQS	PL32A	6	T ³	DQS
T1	PL28B	6	C ³	-	PL32B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
U2	PL29A	6	T	LLM0_PLLT_IN_A	PL33A	6	T	LLM0_PLLT_IN_A
U1	PL29B	6	C	LLM0_PLLC_IN_A	PL33B	6	C	LLM0_PLLC_IN_A
P3	PL30A	6	T ³	-	PL34A	6	T ³	-
P4	PL30B	6	C ³	-	PL34B	6	C ³	-
P6	PL32A	6	T ³	-	PL36A	6	T ³	-
P5	PL32B	6	C ³	-	PL36B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
V2	PL33A	6	T	-	PL37A	6	T	-
V1	PL33B	6	C	-	PL37B	6	C	-
W2	PL34A	6	T ³	-	PL38A	6	T ³	-
W1	PL34B	6	C ³	-	PL38B	6	C ³	-
R3	PL35A	6	-	VREF2_6	PL39A	6	-	VREF2_6
R4	PL36B	6	-	-	PL40B	6	-	-
R6	PL37A	6	T ³	DQS	PL41A	6	T ³	DQS
R5	PL37B	6	C ³	-	PL41B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
Y2	PL38A	6	T	LLM0_PLLT_FB_A	PL42A	6	T	LLM0_PLLT_FB_A
Y1	PL38B	6	C	LLM0_PLLC_FB_A	PL42B	6	C	LLM0_PLLC_FB_A
T3	PL39A	6	T ³	-	PL43A	6	T ³	-
T4	PL39B	6	C ³	-	PL43B	6	C ³	-
W3	PL40A	6	T ³	-	PL44A	6	T ³	-
V3	PL40B	6	C ³	-	PL44B	6	C ³	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
AB5	PB16A	5	T	-	PB20A	5	T	-
AB6	PB16B	5	C	-	PB20B	5	C	-
AA8	PB17A	5	T	-	PB21A	5	T	-
AA9	PB17B	5	C	VREF2_5	PB21B	5	C	VREF2_5
W10	PB18A	5	T	-	PB22A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
V10	PB18B	5	C	-	PB22B	5	C	-
AB7	PB19A	5	T	-	PB23A	5	T	-
AB8	PB19B	5	C	-	PB23B	5	C	-
AB9	PB20A	5	T	-	PB24A	5	T	-
AB10	PB20B	5	C	-	PB24B	5	C	-
Y10	PB21A	5	-	-	PB25A	5	-	-
AA10	PB22B	5	-	-	PB26B	5	-	-
W11	PB23A	5	T	DQS	PB27A	5	T	DQS
V11	PB23B	5	C	-	PB27B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y11	PB24A	5	T	-	PB28A	5	T	-
AA11	PB24B	5	C	-	PB28B	5	C	-
AB11	PB25A	5	T	-	PB29A	5	T	-
AB12	PB25B	5	C	-	PB29B	5	C	-
Y12	PB26A	4	T	-	PB30A	4	T	-
AA12	PB26B	4	C	-	PB30B	4	C	-
W12	PB27A	4	T	PCLKT4_0	PB31A	4	T	PCLKT4_0
V12	PB27B	4	C	PCLKC4_0	PB31B	4	C	PCLKC4_0
-	GNDIO4	4	-	-	GNDIO4	4	-	-
AB13	PB28A	4	T	-	PB32A	4	T	-
AB14	PB28B	4	C	-	PB32B	4	C	-
AA13	PB29A	4	-	-	PB33A	4	-	-
Y13	PB30B	4	-	-	PB34B	4	-	-
AB15	PB31A	4	T	DQS	PB35A	4	T	DQS
AB16	PB31B	4	C	VREF1_4	PB35B	4	C	VREF1_4
V13	PB32A	4	T	-	PB36A	4	T	-
W13	PB32B	4	C	-	PB36B	4	C	-
AA14	PB33A	4	T	-	PB37A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA15	PB33B	4	C	-	PB37B	4	C	-
AB17	PB34A	4	T	-	PB38A	4	T	-
AB18	PB34B	4	C	-	PB38B	4	C	-
W14	PB35A	4	T	-	PB39A	4	T	-
Y14	PB35B	4	C	-	PB39B	4	C	-
U14	PB36A	4	T	VREF2_4	PB40A	4	T	VREF2_4
V14	PB36B	4	C	-	PB40B	4	C	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
AB19	PB37A	4	-	-	PB41A	4	-	-
AB20	PB38B	4	-	-	PB42B	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
V15	PB39A	4	T	DQS	PB43A	4	T	DQS
U15	PB39B	4	C	-	PB43B	4	C	-
Y15	PB40A	4	T	-	PB44A	4	T	-
W15	PB40B	4	C	-	PB44B	4	C	-
AA16	PB41A	4	T	-	PB45A	4	T	-
AA17	PB41B	4	C	-	PB45B	4	C	-
AA18	PB42A	4	T	-	PB46A	4	T	-
AA19	PB42B	4	C	-	PB46B	4	C	-
Y16	PB43A	4	T	-	PB47A	4	T	-
W16	PB43B	4	C	-	PB47B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA20	PB44A	4	T	-	PB48A	4	T	-
AA21	PB44B	4	C	-	PB48B	4	C	-
Y17	PB45A	4	-	-	PB49A	4	-	-
Y18	PB46B	4	-	-	PB50B	4	-	-
Y19	PB47A	4	T	DQS	PB51A	4	T	DQS
Y20	PB47B	4	C	-	PB51B	4	C	-
V16	PB48A	4	T	-	PB52A	4	T	-
U16	PB48B	4	C	-	PB52B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
U18	-	-	-	-	PB53A	4	T	-
V18	-	-	-	-	PB53B	4	C	-
W19	-	-	-	-	PB54A	4	T	-
W18	-	-	-	-	PB54B	4	C	-
U17	-	-	-	-	PB55A	4	T	-
V17	-	-	-	-	PB55B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
W17	-	-	-	-	PB56A	4	-	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
V19	PR43A	3	-	-	PR47A	3	-	-
U20	PR42B	3	C ³	-	PR46B	3	C ³	-
U19	PR42A	3	T ³	-	PR46A	3	T ³	-
V20	PR41B	3	C	-	PR45B	3	C	-
W20	PR41A	3	T	-	PR45A	3	T	-
T17	PR40B	3	C ³	-	PR44B	3	C ³	-
T18	PR40A	3	T ³	-	PR44A	3	T ³	-
T19	PR39B	3	C ³	-	PR43B	3	C ³	-
T20	PR39A	3	T ³	-	PR43A	3	T ³	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
J15	GND	-	-	-	GND	-	-	-
J8	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-
K10	GND	-	-	-	GND	-	-	-
K11	GND	-	-	-	GND	-	-	-
K12	GND	-	-	-	GND	-	-	-
K13	GND	-	-	-	GND	-	-	-
K14	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-
L10	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-
L12	GND	-	-	-	GND	-	-	-
L13	GND	-	-	-	GND	-	-	-
L14	GND	-	-	-	GND	-	-	-
L9	GND	-	-	-	GND	-	-	-
M10	GND	-	-	-	GND	-	-	-
M11	GND	-	-	-	GND	-	-	-
M12	GND	-	-	-	GND	-	-	-
M13	GND	-	-	-	GND	-	-	-
M14	GND	-	-	-	GND	-	-	-
M9	GND	-	-	-	GND	-	-	-
N10	GND	-	-	-	GND	-	-	-
N11	GND	-	-	-	GND	-	-	-
N12	GND	-	-	-	GND	-	-	-
N13	GND	-	-	-	GND	-	-	-
N14	GND	-	-	-	GND	-	-	-
N9	GND	-	-	-	GND	-	-	-
P10	GND	-	-	-	GND	-	-	-
P11	GND	-	-	-	GND	-	-	-
P12	GND	-	-	-	GND	-	-	-
P13	GND	-	-	-	GND	-	-	-
P14	GND	-	-	-	GND	-	-	-
P15	GND	-	-	-	GND	-	-	-
P8	GND	-	-	-	GND	-	-	-
P9	GND	-	-	-	GND	-	-	-
R14	GND	-	-	-	GND	-	-	-
R9	GND	-	-	-	GND	-	-	-
F10	VCC	-	-	-	VCC	-	-	-
F13	VCC	-	-	-	VCC	-	-	-
G10	VCC	-	-	-	VCC	-	-	-
G13	VCC	-	-	-	VCC	-	-	-
G14	VCC	-	-	-	VCC	-	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

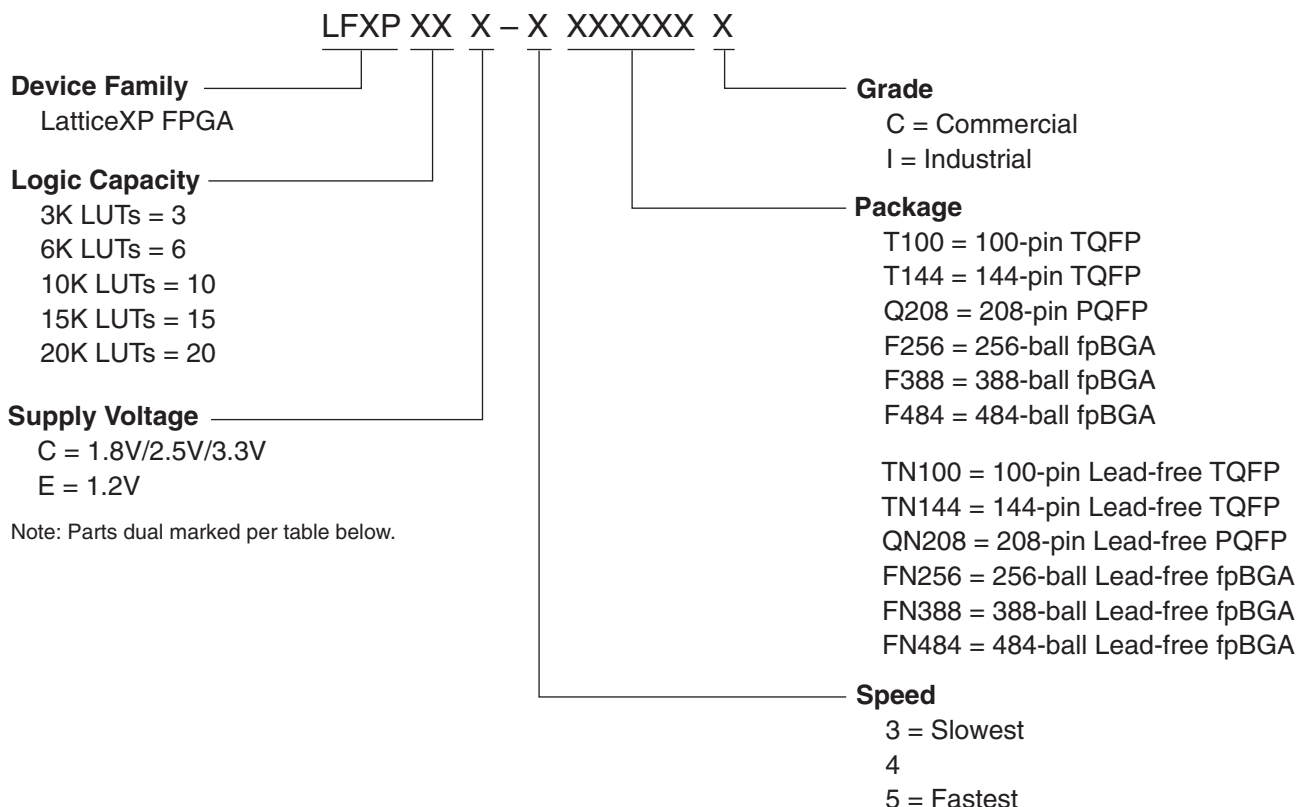
Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
H13	VCCIO1	1	-	-	VCCIO1	1	-	-
K15	VCCIO2	2	-	-	VCCIO2	2	-	-
L15	VCCIO2	2	-	-	VCCIO2	2	-	-
L16	VCCIO2	2	-	-	VCCIO2	2	-	-
L17	VCCIO2	2	-	-	VCCIO2	2	-	-
M15	VCCIO3	3	-	-	VCCIO3	3	-	-
M16	VCCIO3	3	-	-	VCCIO3	3	-	-
M17	VCCIO3	3	-	-	VCCIO3	3	-	-
N15	VCCIO3	3	-	-	VCCIO3	3	-	-
R12	VCCIO4	4	-	-	VCCIO4	4	-	-
R13	VCCIO4	4	-	-	VCCIO4	4	-	-
T12	VCCIO4	4	-	-	VCCIO4	4	-	-
U12	VCCIO4	4	-	-	VCCIO4	4	-	-
R10	VCCIO5	5	-	-	VCCIO5	5	-	-
R11	VCCIO5	5	-	-	VCCIO5	5	-	-
T11	VCCIO5	5	-	-	VCCIO5	5	-	-
U11	VCCIO5	5	-	-	VCCIO5	5	-	-
M6	VCCIO6	6	-	-	VCCIO6	6	-	-
M7	VCCIO6	6	-	-	VCCIO6	6	-	-
M8	VCCIO6	6	-	-	VCCIO6	6	-	-
N8	VCCIO6	6	-	-	VCCIO6	6	-	-
K8	VCCIO7	7	-	-	VCCIO7	7	-	-
L6	VCCIO7	7	-	-	VCCIO7	7	-	-
L7	VCCIO7	7	-	-	VCCIO7	7	-	-
L8	VCCIO7	7	-	-	VCCIO7	7	-	-

1. Applies to LFXP "C" only.

2. Applies to LFXP "E" only.

3. Supports dedicated LVDS outputs.

Part Number Description



Ordering Information (Contact Factory for Specific Device Availability)

Note: LatticeXP devices are dual marked. For example, the commercial speed grade LFXP10E-4F256C is also marked with industrial grade -3I (LFXP10E-3F256I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:

