Lattice Semiconductor Corporation - LFXP3C-4QN208I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	3000
Total RAM Bits	55296
Number of I/O	136
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp3c-4qn208i

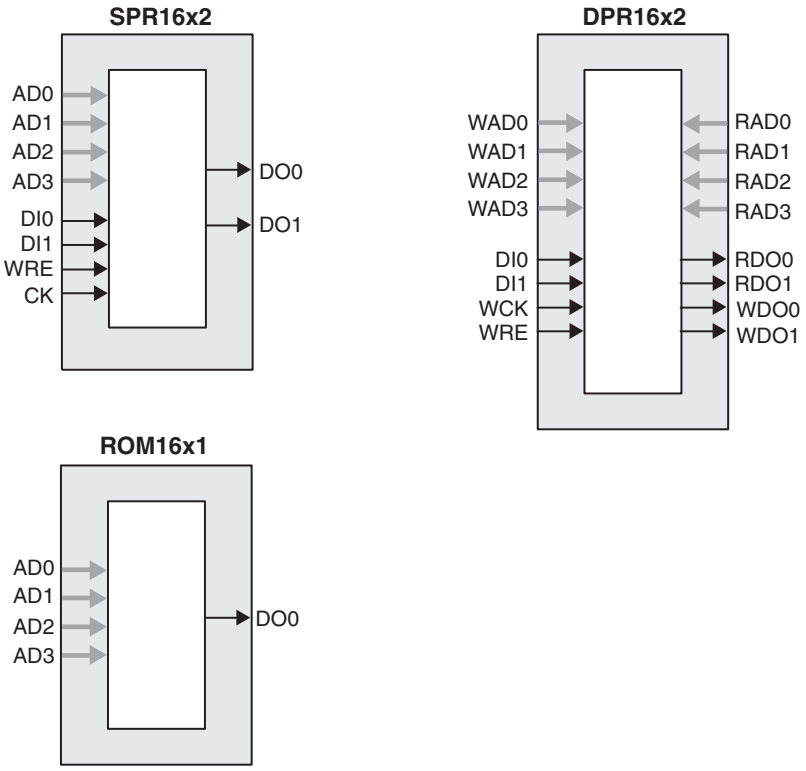
The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-4 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices, one Slice functions as the read-write port. The other companion Slice supports the read-only port. For more information on RAM mode in LatticeXP devices, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required for Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of Slices	1	2

Note: SPR = Single Port RAM, DPR = Dual Port RAM

Figure 2-4. Distributed Memory Primitives

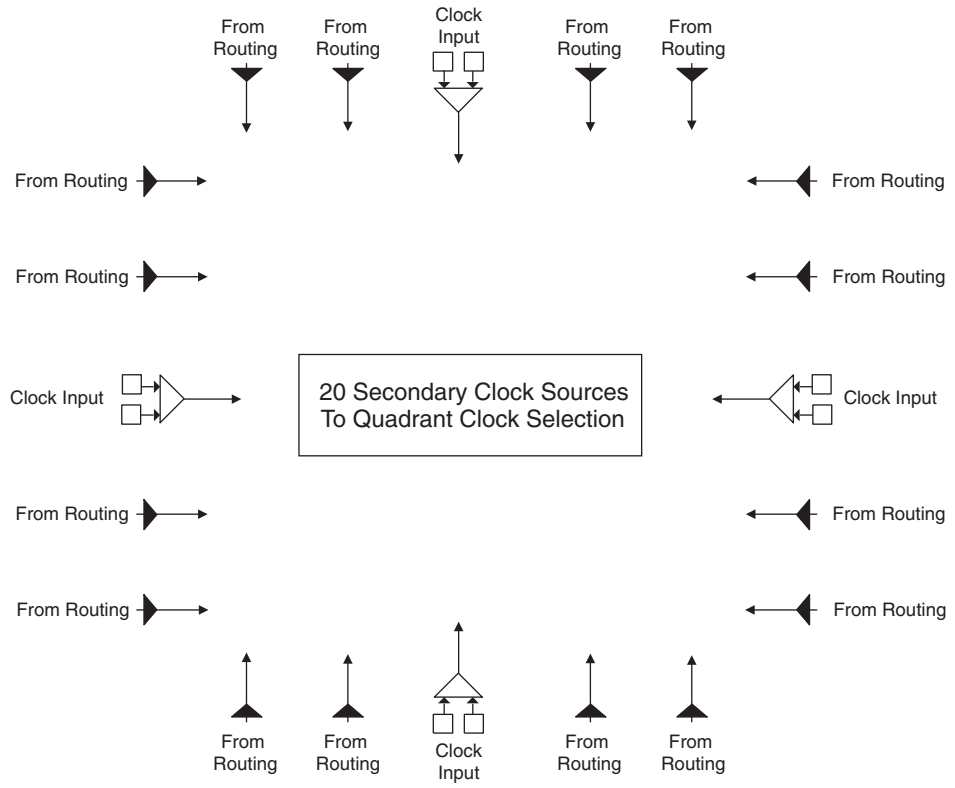


ROM Mode: The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

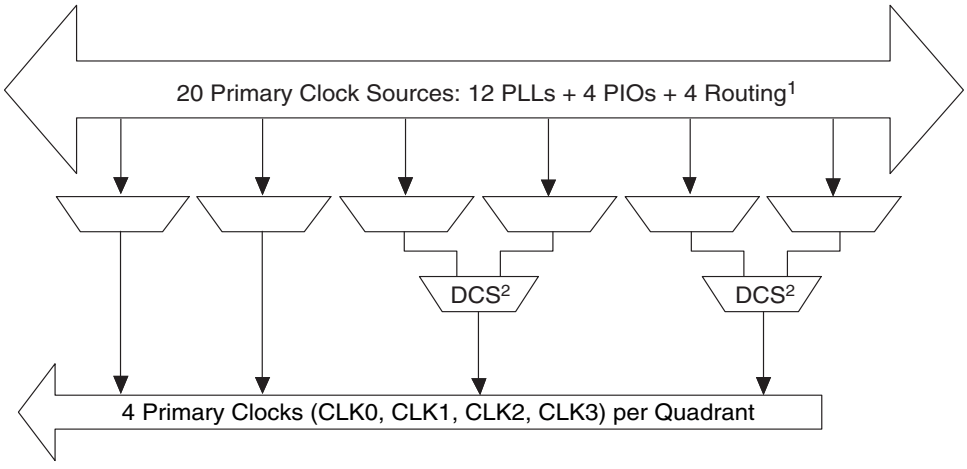
Figure 2-6. Secondary Clock Sources



Clock Routing

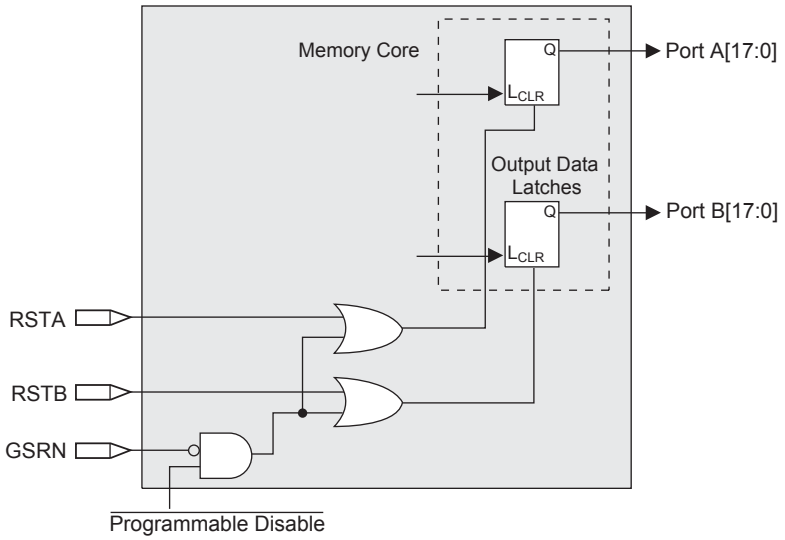
The clock routing structure in LatticeXP devices consists of four Primary Clock lines and a Secondary Clock network per quadrant. The primary clocks are generated from MUXs located in each quadrant. Figure 2-7 shows this clock routing. The four secondary clocks are generated from MUXs located in each quadrant as shown in Figure 2-8. Each slice derives its clock from the primary clock lines, secondary clock lines and routing as shown in Figure 2-9.

Figure 2-7. Per Quadrant Primary Clock Selection



1. Smaller devices have fewer PLL related lines.
2. Dynamic clock select.

Figure 2-15. Memory Core Reset

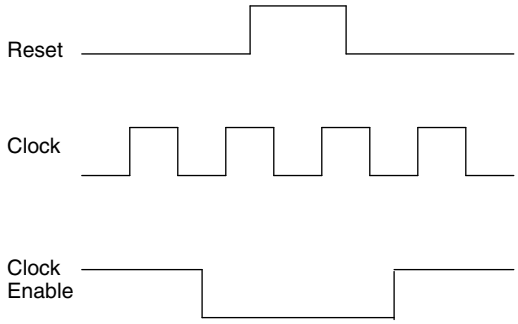


For further information on sysMEM EBR block, see the details of additional technical documentation at the end of this data sheet.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-16. The GSR input to the EBR is always asynchronous.

Figure 2-16. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

Programmable I/O Cells (PICs)

Each PIC contains two PIOs connected to their respective sysIO Buffers which are then connected to the PADs as shown in Figure 2-17. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to sysIO buffer, and receives input from the buffer.

Figure 2-21. Input Register DDR Waveforms

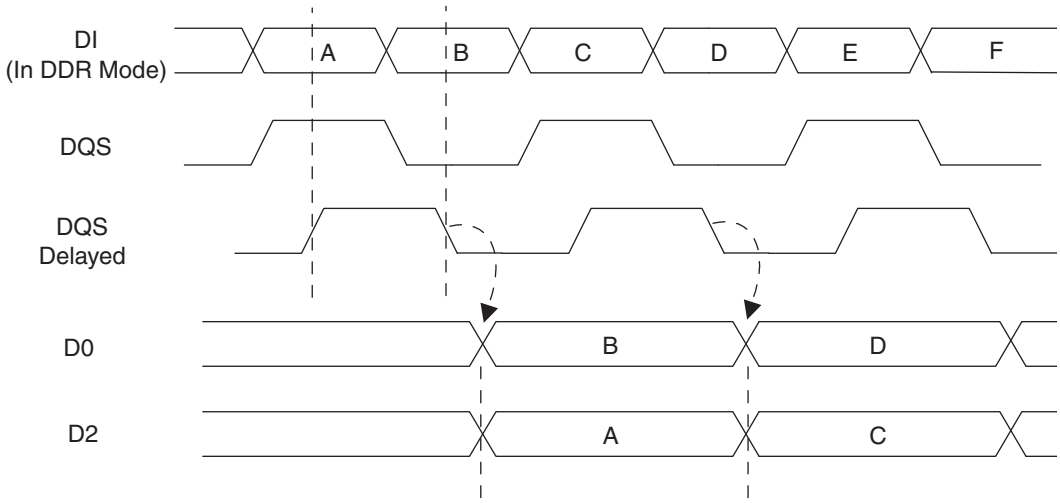
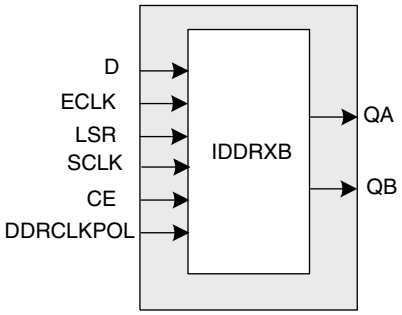


Figure 2-22. INDDRXB Primitive



Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-23 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or as a latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-24 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

Figure 2-26. DQS Local Bus

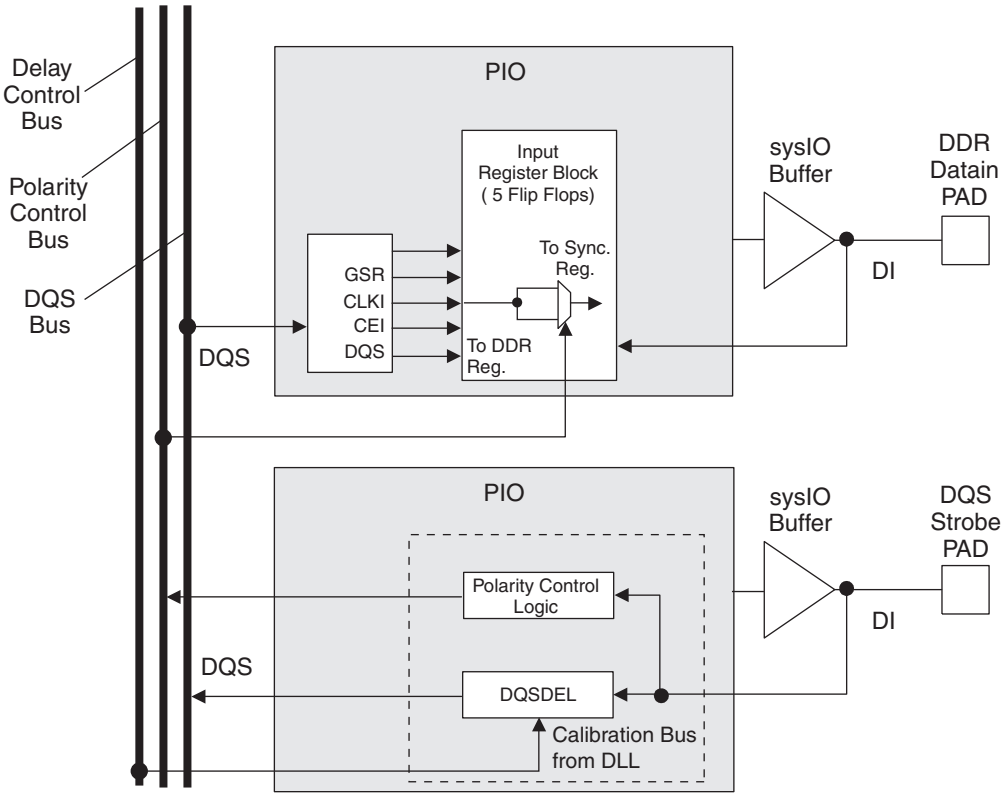


Figure 2-27. DLL Calibration Bus and DQS/DQS Transition Distribution

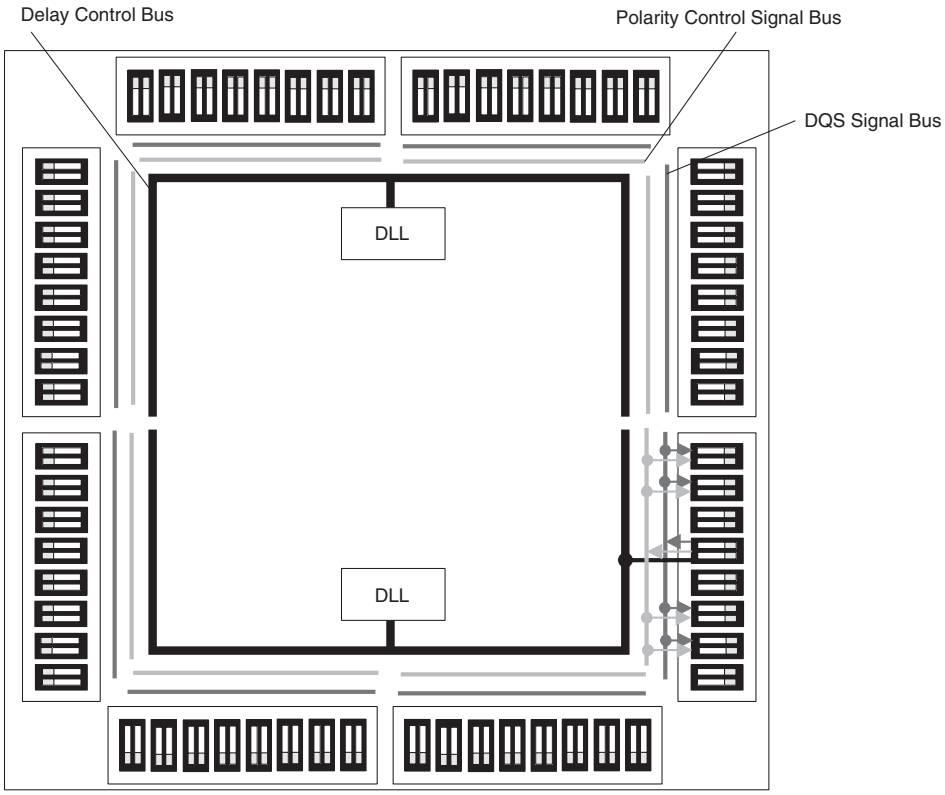
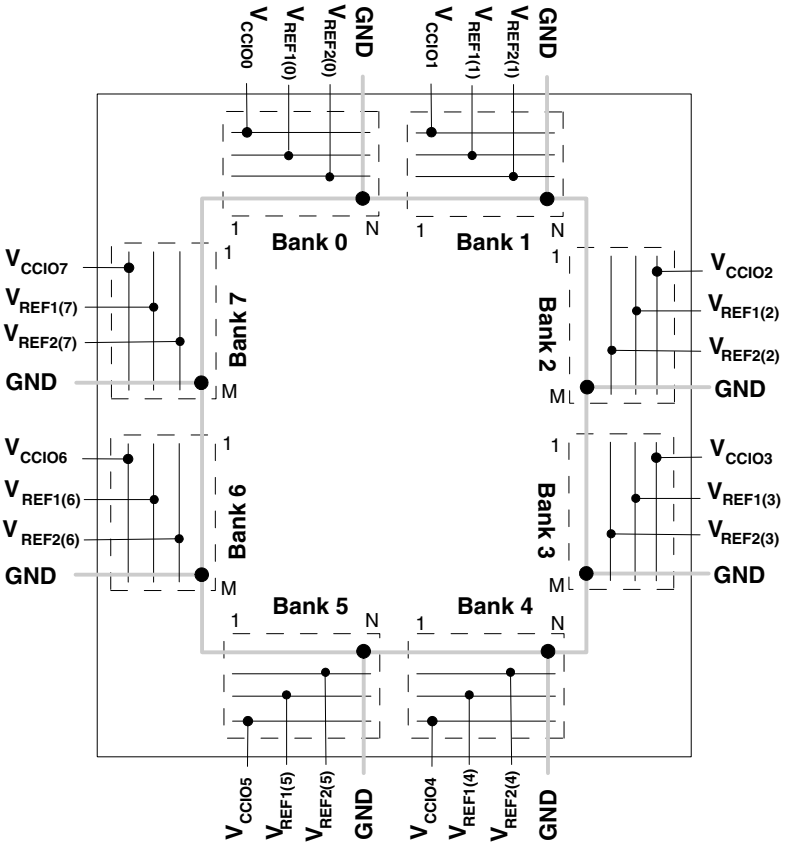


Figure 2-28. LatticeXP Banks



Note: N and M are the maximum number of I/Os per bank.

LatticeXP devices contain two types of sysIO buffer pairs.

1. **Top and Bottom sysIO Buffer Pair (Single-Ended Outputs Only)**
   The sysIO buffer pairs in the top and bottom banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

   Only the I/Os on the top and bottom banks have PCI clamps. Note that the PCI clamp is enabled after V_{CC}, V_{CCAUX} and V_{CCIO} are at valid operating levels and the device has been configured.

2. **Left and Right sysIO Buffer Pair (Differential and Single-Ended Outputs)**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. The referenced input buffer can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

   Select I/Os in the left and right banks have LVDS differential output drivers. Refer to the Logic Signal Connections tables for more information.

Derating Logic Timing

Logic timing provided in the following sections of this data sheet and in the ispLEVER design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best-case process can be much better than the values given in the tables. The ispLEVER design tool from Lattice can provide logic timing numbers at a particular temperature and voltage.

LatticeXP Internal Timing Parameters[1] (Continued)

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register	—	1.61	—	1.94	—	2.32	ns
PLL Parameters								
t_{RSTREC}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
t_{RSTSU}	Reset Signal Setup Time	1.00	—	1.00	—	1.00	—	ns

1. Internal parameters are characterized but not tested on every device.

Timing v.F0.11

Timing Diagrams

PFU Timing Diagrams

Figure 3-6. Slice Single/Dual Port Write Cycle Timing

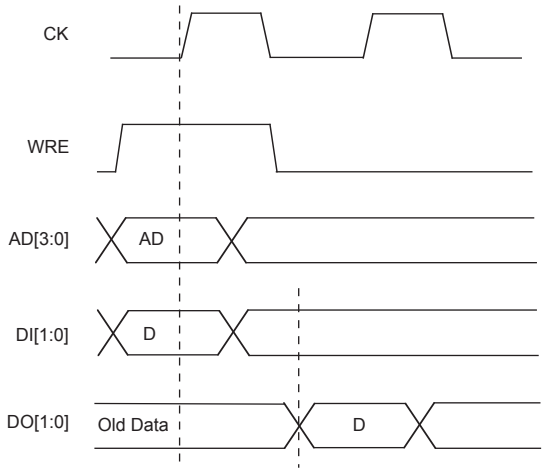
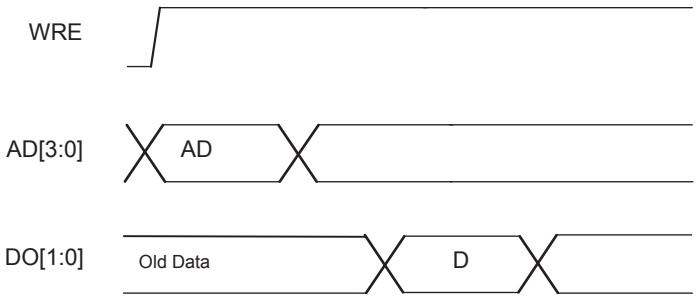


Figure 3-7. Slice Single /Dual Port Read Cycle Timing



LFXP3 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	Pin Function	Bank	Differential	Dual Function
88	PT14B	1	-	D7
89	PT13B	0	C	BUSY
90	GNDIO0	0	-	-
91	PT13A	0	T	CS1N
92	PT12B	0	C	PCLKC0_0
93	PT12A	0	T	PCLKT0_0
94	VCCIO0	0	-	-
95	PT9A	0	-	DOUT
96	PT8A	0	-	WRITEN
97	PT6A	0	-	DI
98	PT5A	0	-	CSN
99	GND	-	-	-
100	CFG0	0	-	-

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA

Ball Number	LFXP6				LFXP10			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
C2	PROGRAMN	7	-	-	PROGRAMN	7	-	-
C1	CCLK	7	-	-	CCLK	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
D2	PL3A	7	T	LUM0_PLLT_FB_A	PL3A	7	T	LUM0_PLLT_FB_A
D3	PL3B	7	C	LUM0_PLLC_FB_A	PL3B	7	C	LUM0_PLLC_FB_A
D1	PL2A	7	T[3]	-	PL5A	7	-	-
E2	PL5A	7	-	VREF1_7	PL6B	7	-	VREF1_7
-	GNDIO7	7	-	-	GNDIO7	7	-	-
E1	PL7A	7	T[3]	DQS	PL7A	7	T[3]	DQS
F1	PL7B	7	C[3]	-	PL7B	7	C[3]	-
E3	PL12A	7	T	-	PL8A	7	T	-
F4	PL12B	7	C	-	PL8B	7	C	-
F3	PL4A	7	T[3]	-	PL9A	7	T[3]	-
F2	PL4B	7	C[3]	-	PL9B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
G1	PL2B	7	C[3]	-	PL11B	7	-	-
G3	PL8A	7	T	LUM0_PLLT_IN_A	PL12A	7	T	LUM0_PLLT_IN_A
G2	PL8B	7	C	LUM0_PLLC_IN_A	PL12B	7	C	LUM0_PLLC_IN_A
H1	PL9A	7	T[3]	-	PL13A	7	T[3]	-
H2	PL9B	7	C[3]	-	PL13B	7	C[3]	-
G4	PL6B	7	-	VREF2_7	PL14A	7	-	VREF2_7
G5	PL14A	7	-	-	PL15B	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
J1	PL11A	7	T[3]	-	PL16A	7	T[3]	DQS
J2	PL11B	7	C[3]	-	PL16B	7	C[3]	-
H3	PL13A	7	T[3]	-	PL18A	7	T[3]	-
J3	PL13B	7	C[3]	-	PL18B	7	C[3]	-
H4	VCCP0	-	-	-	VCCP0	-	-	-
H5	GNDP0	-	-	-	GNDP0	-	-	-
K1	PL17A	6	T	PCLKT6_0	PL20A	6	T	PCLKT6_0
K2	PL17B	6	C	PCLKC6_0	PL20B	6	C	PCLKC6_0
-	GNDIO6	6	-	-	GNDIO6	6	-	-
J4	PL15B	6	-	-	PL22A	6	-	-
J5	PL22A	6	-	VREF1_6	PL23B	6	-	VREF1_6
L1	PL16A	6	T[3]	-	PL24A	6	T[3]	DQS
L2	PL16B	6	C[3]	-	PL24B	6	C[3]	-
M1	PL18A	6	T[3]	-	PL25A	6	T	LLM0_PLLT_IN_A
M2	PL18B	6	C[3]	-	PL25B	6	C	LLM0_PLLC_IN_A
K3	PL19A	6	T[3]	-	PL26A	6	T[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
L3	PL19B	6	C[3]	-	PL26B	6	C[3]	-
L4	PL21A	6	T[3]	-	PL28A	6	-	-

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP6				LFXP10			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L15	PR21B	3	C[3]	-	PR28B	3	C[3]	-
L14	PR21A	3	T[3]	-	PR28A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
L12	PR17B	3	C	-	PR26A	3	-	-
M16	PR20B	3	C	-	PR25B	3	C	RLM0_PLLC_IN_A
N16	PR20A	3	T	-	PR25A	3	T	RLM0_PLLT_IN_A
K14	PR19B	3	C[3]	-	PR24B	3	C[3]	-
K15	PR19A	3	T[3]	-	PR24A	3	T[3]	DQS
K12	PR17A	3	T	-	PR23B	3	-	-
K13	PR22A	3	-	VREF2_3	PR22A	3	-	VREF2_3
-	GNDIO3	3	-	-	GNDIO3	3	-	-
L16	PR18B	3	C[3]	-	PR21B	3	C[3]	-
K16	PR18A	3	T[3]	-	PR21A	3	T[3]	-
J15	PR16B	3	C[3]	-	PR19B	3	C[3]	-
J14	PR16A	3	T[3]	-	PR19A	3	T[3]	-
J13	GNDP1	-	-	-	GNDP1	-	-	-
J12	VCCP1	-	-	-	VCCP1	-	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
J16	PR12B	2	C	PCLKC2_0	PR17B	2	C	PCLKC2_0
H16	PR12A	2	T	PCLKT2_0	PR17A	2	T	PCLKT2_0
H13	PR13B	2	C[3]	-	PR16B	2	C[3]	-
H12	PR13A	2	T[3]	-	PR16A	2	T[3]	DQS
H15	PR2B	2	C[3]	-	PR15B	2	-	-
H14	PR6B	2	-	VREF1_2	PR14A	2	-	VREF1_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G15	PR11B	2	C[3]	-	PR13B	2	C[3]	-
G14	PR11A	2	T[3]	-	PR13A	2	T[3]	-
G16	PR8B	2	C	RUM0_PLLC_IN_A	PR12B	2	C	RUM0_PLLC_IN_A
F16	PR8A	2	T	RUM0_PLLT_IN_A	PR12A	2	T	RUM0_PLLT_IN_A
G13	PR2A	2	T[3]	-	PR11B	2	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G12	PR9B	2	C[3]	-	PR8B	2	C	-
F13	PR9A	2	T[3]	-	PR8A	2	T	-
B16	PR7B	2	C[3]	-	PR7B	2	C[3]	-
C16	PR7A	2	T[3]	DQS	PR7A	2	T[3]	DQS
F15	PR14A	2	-	-	PR6B	2	-	-
E15	PR5A	2	-	VREF2_2	PR5A	2	-	VREF2_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
F14	PR4B	2	C[3]	-	PR4B	2	C[3]	-
E14	PR4A	2	T[3]	-	PR4A	2	T[3]	-
D15	PR3B	2	C	RUM0_PLLC_FB_A	PR3B	2	C	RUM0_PLLC_FB_A
C15	PR3A	2	T	RUM0_PLLT_FB_A	PR3A	2	T	RUM0_PLLT_FB_A

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
C2	PROGRAMN	7	-	-	PROGRAMN	7	-	-
C1	CCLK	7	-	-	CCLK	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
D2	PL7A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A
D3	PL7B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A
D1	PL9A	7	-	-	PL9A	7	-	-
E2	PL10B	7	-	VREF1_7	PL10B	7	-	VREF1_7
E1	PL11A	7	T[3]	DQS	PL11A	7	T[3]	DQS
F1	PL11B	7	C[3]	-	PL11B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
E3	PL12A	7	T	-	PL12A	7	T	-
F4	PL12B	7	C	-	PL12B	7	C	-
F3	PL13A	7	T[3]	-	PL13A	7	T[3]	-
F2	PL13B	7	C[3]	-	PL13B	7	C[3]	-
G1	PL15B	7	-	-	PL15B	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
G3	PL16A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A
G2	PL16B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A
H1	PL17A	7	T[3]	-	PL17A	7	T[3]	-
H2	PL17B	7	C[3]	-	PL17B	7	C[3]	-
G4	PL18A	7	-	VREF2_7	PL18A	7	-	VREF2_7
G5	PL19B	7	-	-	PL19B	7	-	-
J1	PL20A	7	T[3]	DQS	PL20A	7	T[3]	DQS
-	GNDIO7	7	-	-	GNDIO7	7	-	-
J2	PL20B	7	C[3]	-	PL20B	7	C[3]	-
H3	PL22A	7	T[3]	-	PL22A	7	T[3]	-
J3	PL22B	7	C[3]	-	PL22B	7	C[3]	-
H4	VCCP0	-	-	-	VCCP0	-	-	-
H5	GNDP0	-	-	-	GNDP0	-	-	-
K1	PL24A	6	T	PCLKT6_0	PL28A	6	T	PCLKT6_0
-	GNDIO6	6	-	-	GNDIO6	6	-	-
K2	PL24B	6	C	PCLKC6_0	PL28B	6	C	PCLKC6_0
J4	PL26A	6	-	-	PL30A	6	-	-
J5	PL27B	6	-	VREF1_6	PL31B	6	-	VREF1_6
L1	PL28A	6	T[3]	DQS	PL32A	6	T[3]	DQS
L2	PL28B	6	C[3]	-	PL32B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
M1	PL29A	6	T	LLM0_PLLT_IN_A	PL33A	6	T	LLM0_PLLT_IN_A
M2	PL29B	6	C	LLM0_PLLC_IN_A	PL33B	6	C	LLM0_PLLC_IN_A
K3	PL30A	6	T[3]	-	PL34A	6	T[3]	-
L3	PL30B	6	C[3]	-	PL34B	6	C[3]	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
F4	PROGRAMN	7	-	-	PROGRAMN	7	-	-	PROGRAMN	7	-	-
G4	CCLK	7	-	-	CCLK	7	-	-	CCLK	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
D2	PL2A	7	T[3]	-	PL6A	7	T[3]	-	PL6A	7	T[3]	-
D1	PL2B	7	C[3]	-	PL6B	7	C[3]	-	PL6B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
E2	PL3A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A
E3	PL3B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A
F3	PL4A	7	T[3]	-	PL8A	7	T[3]	-	PL8A	7	T[3]	-
F2	PL4B	7	C[3]	-	PL8B	7	C[3]	-	PL8B	7	C[3]	-
H4	PL5A	7	-	-	PL9A	7	-	-	PL9A	7	-	-
H3	PL6B	7	-	VREF1_7	PL10B	7	-	VREF1_7	PL10B	7	-	VREF1_7
G3	PL7A	7	T[3]	DQS	PL11A	7	T[3]	DQS	PL11A	7	T[3]	DQS
G2	PL7B	7	C[3]	-	PL11B	7	C[3]	-	PL11B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
F1	PL8A	7	T	-	PL12A	7	T	-	PL12A	7	T	-
E1	PL8B	7	C	-	PL12B	7	C	-	PL12B	7	C	-
J4	PL9A	7	T[3]	-	PL13A	7	T[3]	-	PL13A	7	T[3]	-
K4	PL9B	7	C[3]	-	PL13B	7	C[3]	-	PL13B	7	C[3]	-
G1	PL11A	7	T[3]	-	PL15A	7	T[3]	-	PL15A	7	T[3]	-
H2	PL11B	7	C[3]	-	PL15B	7	C[3]	-	PL15B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
J2	PL12A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A
H1	PL12B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A
J1	PL13A	7	T[3]	-	PL17A	7	T[3]	-	PL17A	7	T[3]	-
K2	PL13B	7	C[3]	-	PL17B	7	C[3]	-	PL17B	7	C[3]	-
K3	PL14A	7	-	VREF2_7	PL18A	7	-	VREF2_7	PL18A	7	-	VREF2_7
J3	PL15B	7	-	-	PL19B	7	-	-	PL19B	7	-	-
K1	PL16A	7	T[3]	DQS	PL20A	7	T[3]	DQS	PL20A	7	T[3]	DQS
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
L2	PL16B	7	C[3]	-	PL20B	7	C[3]	-	PL20B	7	C[3]	-
L3	PL17A	7	T	-	PL21A	7	T	-	PL21A	7	T	-
L4	PL17B	7	C	-	PL21B	7	C	-	PL21B	7	C	-
L1	PL18A	7	T[3]	-	PL22A	7	T[3]	-	PL22A	7	T[3]	-
M1	PL18B	7	C[3]	-	PL22B	7	C[3]	-	PL22B	7	C[3]	-
M2	VCCP0	-	-	-	VCCP0	-	-	-	VCCP0	-	-	-
N1	GNDP0	-	-	-	GNDP0	-	-	-	GNDP0	-	-	-
M3	PL19A	6	T[3]	-	PL23A	6	T[3]	-	PL27A	6	T[3]	-
M4	PL19B	6	C[3]	-	PL23B	6	C[3]	-	PL27B	6	C[3]	-
P1	PL20A	6	T	PCLKT6_0	PL24A	6	T	PCLKT6_0	PL28A	6	T	PCLKT6_0
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
N2	PL20B	6	C	PCLKC6_0	PL24B	6	C	PCLKC6_0	PL28B	6	C	PCLKC6_0
R1	PL21A	6	T[3]	-	PL25A	6	T[3]	-	PL29A	6	T[3]	-
P2	PL21B	6	C[3]	-	PL25B	6	C[3]	-	PL29B	6	C[3]	-
N3	PL22A	6	-	-	PL26A	6	-	-	PL30A	6	-	-
N4	PL23B	6	-	VREF1_6	PL27B	6	-	VREF1_6	PL31B	6	-	VREF1_6
T1	PL24A	6	T[3]	DQS	PL28A	6	T[3]	DQS	PL32A	6	T[3]	DQS
R2	PL24B	6	C[3]	-	PL28B	6	C[3]	-	PL32B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
AA20	PB36B	4	C	-	PB41B	4	C	-	PB45B	4	C	-
AB21	PB37A	4	T	-	PB42A	4	T	-	PB46A	4	T	-
AA21	PB37B	4	C	-	PB42B	4	C	-	PB46B	4	C	-
AA22	PB38A	4	T	-	PB43A	4	T	-	PB47A	4	T	-
Y21	PB38B	4	C	-	PB43B	4	C	-	PB47B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
W16	PB39A	4	-	-	PB44A	4	T	-	PB48A	4	T	-
W17	-	-	-	-	PB44B	4	C	-	PB48B	4	C	-
Y15	-	-	-	-	PB45A	4	-	-	PB49A	4	-	-
Y16	-	-	-	-	PB46B	4	-	-	PB50B	4	-	-
W19	-	-	-	-	PB47A	4	T	DQS	PB51A	4	T	DQS
W18	-	-	-	-	PB47B	4	C	-	PB51B	4	C	-
W20	-	-	-	-	PB48A	4	-	-	PB52A	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
T20	PR35B	3	C[3]	-	PR39B	3	C[3]	-	PR43B	3	C[3]	-
T19	PR35A	3	T[3]	-	PR39A	3	T[3]	-	PR43A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
U19	PR34B	3	C	RLM0_PLLC_FB_A	PR38B	3	C	RLM0_PLLC_FB_A	PR42B	3	C	RLM0_PLLC_FB_A
U20	PR34A	3	T	RLM0_PLLT_FB_A	PR38A	3	T	RLM0_PLLT_FB_A	PR42A	3	T	RLM0_PLLT_FB_A
V19	PR33B	3	C[3]	-	PR37B	3	C[3]	-	PR41B	3	C[3]	-
V20	PR33A	3	T[3]	DQS	PR37A	3	T[3]	DQS	PR41A	3	T[3]	DQS
R19	PR32B	3	-	-	PR36B	3	-	-	PR40B	3	-	-
R20	PR31A	3	-	VREF1_3	PR35A	3	-	VREF1_3	PR39A	3	-	VREF1_3
W21	PR30B	3	C[3]	-	PR34B	3	C[3]	-	PR38B	3	C[3]	-
Y22	PR30A	3	T[3]	-	PR34A	3	T[3]	-	PR38A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
P19	PR29B	3	C	-	PR33B	3	C	-	PR37B	3	C	-
P20	PR29A	3	T	-	PR33A	3	T	-	PR37A	3	T	-
V21	PR28B	3	C[3]	-	PR32B	3	C[3]	-	PR36B	3	C[3]	-
W22	PR28A	3	T[3]	-	PR32A	3	T[3]	-	PR36A	3	T[3]	-
U21	PR26B	3	C[3]	-	PR30B	3	C[3]	-	PR34B	3	C[3]	-
V22	PR26A	3	T[3]	-	PR30A	3	T[3]	-	PR34A	3	T[3]	-
T21	PR25B	3	C	RLM0_PLLC_IN_A	PR29B	3	C	RLM0_PLLC_IN_A	PR33B	3	C	RLM0_PLLC_IN_A
U22	PR25A	3	T	RLM0_PLLT_IN_A	PR29A	3	T	RLM0_PLLT_IN_A	PR33A	3	T	RLM0_PLLT_IN_A
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
R21	PR24B	3	C[3]	-	PR28B	3	C[3]	-	PR32B	3	C[3]	-
T22	PR24A	3	T[3]	DQS	PR28A	3	T[3]	DQS	PR32A	3	T[3]	DQS
N19	PR23B	3	-	-	PR27B	3	-	-	PR31B	3	-	-
N20	PR22A	3	-	VREF2_3	PR26A	3	-	VREF2_3	PR30A	3	-	VREF2_3
R22	PR21B	3	C[3]	-	PR25B	3	C[3]	-	PR29B	3	C[3]	-
P22	PR21A	3	T[3]	-	PR25A	3	T[3]	-	PR29A	3	T[3]	-
P21	PR20B	3	C	-	PR24B	3	C	-	PR28B	3	C	-
N21	PR20A	3	T	-	PR24A	3	T	-	PR28A	3	T	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
M20	PR19B	3	C[3]	-	PR23B	3	C[3]	-	PR27B	3	C[3]	-
M19	PR19A	3	T[3]	-	PR23A	3	T[3]	-	PR27A	3	T[3]	-
N22	GNDP1	-	-	-	GNDP1	-	-	-	GNDP1	-	-	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
M21	VCCP1	-	-	-	VCCP1	-	-	-	VCCP1	-	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
M22	PR18B	2	C[3]	-	PR22B	2	C[3]	-	PR22B	2	C[3]	-
L22	PR18A	2	T[3]	-	PR22A	2	T[3]	-	PR22A	2	T[3]	-
K22	PR17B	2	C	PCLKC2_0	PR21B	2	C	PCLKC2_0	PR21B	2	C	PCLKC2_0
K21	PR17A	2	T	PCLKT2_0	PR21A	2	T	PCLKT2_0	PR21A	2	T	PCLKT2_0
L19	PR16B	2	C[3]	-	PR20B	2	C[3]	-	PR20B	2	C[3]	-
K20	PR16A	2	T[3]	DQS	PR20A	2	T[3]	DQS	PR20A	2	T[3]	DQS
L20	PR15B	2	-	-	PR19B	2	-	-	PR19B	2	-	-
L21	PR14A	2	-	VREF1_2	PR18A	2	-	VREF1_2	PR18A	2	-	VREF1_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
J22	PR13B	2	C[3]	-	PR17B	2	C[3]	-	PR17B	2	C[3]	-
J21	PR13A	2	T[3]	-	PR17A	2	T[3]	-	PR17A	2	T[3]	-
H22	PR12B	2	C	RUM0_PLLC_IN_A	PR16B	2	C	RUM0_PLLC_IN_A	PR16B	2	C	RUM0_PLLC_IN_A
H21	PR12A	2	T	RUM0_PLLT_IN_A	PR16A	2	T	RUM0_PLLT_IN_A	PR16A	2	T	RUM0_PLLT_IN_A
K19	PR11B	2	C[3]	-	PR15B	2	C[3]	-	PR15B	2	C[3]	-
J19	PR11A	2	T[3]	-	PR15A	2	T[3]	-	PR15A	2	T[3]	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
J20	PR9B	2	C[3]	-	PR13B	2	C[3]	-	PR13B	2	C[3]	-
H20	PR9A	2	T[3]	-	PR13A	2	T[3]	-	PR13A	2	T[3]	-
H19	PR8B	2	C	-	PR12B	2	C	-	PR12B	2	C	-
G19	PR8A	2	T	-	PR12A	2	T	-	PR12A	2	T	-
G22	PR7B	2	C[3]	-	PR11B	2	C[3]	-	PR11B	2	C[3]	-
G21	PR7A	2	T[3]	DQS	PR11A	2	T[3]	DQS	PR11A	2	T[3]	DQS
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
F20	PR6B	2	-	-	PR10B	2	-	-	PR10B	2	-	-
G20	PR5A	2	-	VREF2_2	PR9A	2	-	VREF2_2	PR9A	2	-	VREF2_2
F22	PR4B	2	C[3]	-	PR8B	2	C[3]	-	PR8B	2	C[3]	-
F21	PR4A	2	T[3]	-	PR8A	2	T[3]	-	PR8A	2	T[3]	-
E22	PR3B	2	C	RUM0_PLLC_FB_A	PR7B	2	C	RUM0_PLLC_FB_A	PR7B	2	C	RUM0_PLLC_FB_A
E21	PR3A	2	T	RUM0_PLLT_FB_A	PR7A	2	T	RUM0_PLLT_FB_A	PR7A	2	T	RUM0_PLLT_FB_A
D22	PR2B	2	C[3]	-	PR6B	2	C[3]	-	PR6B	2	C[3]	-
D21	PR2A	2	T[3]	-	PR6A	2	T[3]	-	PR6A	2	T[3]	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
F19	TDO	-	-	-	TDO	-	-	-	TDO	-	-	-
E20	VCCJ	-	-	-	VCCJ	-	-	-	VCCJ	-	-	-
D20	TDI	-	-	-	TDI	-	-	-	TDI	-	-	-
D19	TMS	-	-	-	TMS	-	-	-	TMS	-	-	-
D18	TCK	-	-	-	TCK	-	-	-	TCK	-	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
E19	-	-	-	-	PT48A	1	-	-	PT52A	1	-	-
D17	-	-	-	-	PT47B	1	C	-	PT51B	1	C	-
D16	-	-	-	-	PT47A	1	T	DQS	PT51A	1	T	DQS
C16	-	-	-	-	PT46B	1	-	-	PT50B	1	-	-
C15	-	-	-	-	PT45A	1	-	-	PT49A	1	-	-
C17	-	-	-	-	PT44B	1	C	-	PT48B	1	C	-
C18	PT39A	1	-	-	PT44A	1	T	-	PT48A	1	T	-
C19	PT38B	1	C	-	PT43B	1	C	-	PT47B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
C20	PT38A	1	T	-	PT43A	1	T	-	PT47A	1	T	-
C21	PT37B	1	C	-	PT42B	1	C	-	PT46B	1	C	-
C22	PT37A	1	T	-	PT42A	1	T	-	PT46A	1	T	-
B22	PT36B	1	C	-	PT41B	1	C	-	PT45B	1	C	-
A21	PT36A	1	T	-	PT41A	1	T	-	PT45A	1	T	-
D15	PT35B	1	C	-	PT40B	1	C	-	PT44B	1	C	-
D14	PT35A	1	T	-	PT40A	1	T	-	PT44A	1	T	-
B21	PT34B	1	C	VREF1_1	PT39B	1	C	VREF1_1	PT43B	1	C	VREF1_1
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
A20	PT34A	1	T	DQS	PT39A	1	T	DQS	PT43A	1	T	DQS
B20	PT33B	1	-	-	PT38B	1	-	-	PT42B	1	-	-
A19	PT32A	1	-	-	PT37A	1	-	-	PT41A	1	-	-
B19	PT31B	1	C	-	PT36B	1	C	-	PT40B	1	C	-
A18	PT31A	1	T	-	PT36A	1	T	-	PT40A	1	T	-
C14	PT30B	1	C	-	PT35B	1	C	-	PT39B	1	C	-
C13	PT30A	1	T	D0	PT35A	1	T	D0	PT39A	1	T	D0
B18	PT29B	1	C	D1	PT34B	1	C	D1	PT38B	1	C	D1
A17	PT29A	1	T	VREF2_1	PT34A	1	T	VREF2_1	PT38A	1	T	VREF2_1
B17	PT28B	1	C	-	PT33B	1	C	-	PT37B	1	C	-
A16	PT28A	1	T	D2	PT33A	1	T	D2	PT37A	1	T	D2
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
B16	PT27B	1	C	D3	PT32B	1	C	D3	PT36B	1	C	D3
A15	PT27A	1	T	-	PT32A	1	T	-	PT36A	1	T	-
B15	PT26B	1	C	-	PT31B	1	C	-	PT35B	1	C	-
A14	PT26A	1	T	DQS	PT31A	1	T	DQS	PT35A	1	T	DQS
D13	PT25B	1	-	-	PT30B	1	-	-	PT34B	1	-	-
D12	PT24A	1	-	D4	PT29A	1	-	D4	PT33A	1	-	D4
B14	PT23B	1	C	-	PT28B	1	C	-	PT32B	1	C	-
A13	PT23A	1	T	D5	PT28A	1	T	D5	PT32A	1	T	D5
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
B13	PT22B	1	C	D6	PT27B	1	C	D6	PT31B	1	C	D6
A12	PT22A	1	T	-	PT27A	1	T	-	PT31A	1	T	-
B12	PT21B	1	C	D7	PT26B	1	C	D7	PT30B	1	C	D7
C12	PT21A	1	T	-	PT26A	1	T	-	PT30A	1	T	-
C11	PT20B	0	C	BUSY	PT25B	0	C	BUSY	PT29B	0	C	BUSY
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
B11	PT20A	0	T	CS1N	PT25A	0	T	CS1N	PT29A	0	T	CS1N
A11	PT19B	0	C	PCLKC0_0	PT24B	0	C	PCLKC0_0	PT28B	0	C	PCLKC0_0
A10	PT19A	0	T	PCLKT0_0	PT24A	0	T	PCLKT0_0	PT28A	0	T	PCLKT0_0
B10	PT18B	0	C	-	PT23B	0	C	-	PT27B	0	C	-
B9	PT18A	0	T	DQS	PT23A	0	T	DQS	PT27A	0	T	DQS
D11	PT17B	0	-	-	PT22B	0	-	-	PT26B	0	-	-
D10	PT16A	0	-	DOUT	PT21A	0	-	DOUT	PT25A	0	-	DOUT
A9	PT15B	0	C	-	PT20B	0	C	-	PT24B	0	C	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C8	PT15A	0	T	WRITEN	PT20A	0	T	WRITEN	PT24A	0	T	WRITEN
B8	PT14B	0	C	-	PT19B	0	C	-	PT23B	0	C	-
A8	PT14A	0	T	VREF1_0	PT19A	0	T	VREF1_0	PT23A	0	T	VREF1_0
C7	PT13B	0	C	-	PT18B	0	C	-	PT22B	0	C	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
AB19	PB37A	4	-	-	PB41A	4	-	-
AB20	PB38B	4	-	-	PB42B	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
V15	PB39A	4	T	DQS	PB43A	4	T	DQS
U15	PB39B	4	C	-	PB43B	4	C	-
Y15	PB40A	4	T	-	PB44A	4	T	-
W15	PB40B	4	C	-	PB44B	4	C	-
AA16	PB41A	4	T	-	PB45A	4	T	-
AA17	PB41B	4	C	-	PB45B	4	C	-
AA18	PB42A	4	T	-	PB46A	4	T	-
AA19	PB42B	4	C	-	PB46B	4	C	-
Y16	PB43A	4	T	-	PB47A	4	T	-
W16	PB43B	4	C	-	PB47B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA20	PB44A	4	T	-	PB48A	4	T	-
AA21	PB44B	4	C	-	PB48B	4	C	-
Y17	PB45A	4	-	-	PB49A	4	-	-
Y18	PB46B	4	-	-	PB50B	4	-	-
Y19	PB47A	4	T	DQS	PB51A	4	T	DQS
Y20	PB47B	4	C	-	PB51B	4	C	-
V16	PB48A	4	T	-	PB52A	4	T	-
U16	PB48B	4	C	-	PB52B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
U18	-	-	-	-	PB53A	4	T	-
V18	-	-	-	-	PB53B	4	C	-
W19	-	-	-	-	PB54A	4	T	-
W18	-	-	-	-	PB54B	4	C	-
U17	-	-	-	-	PB55A	4	T	-
V17	-	-	-	-	PB55B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
W17	-	-	-	-	PB56A	4	-	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
V19	PR43A	3	-	-	PR47A	3	-	-
U20	PR42B	3	C[3]	-	PR46B	3	C[3]	-
U19	PR42A	3	T[3]	-	PR46A	3	T[3]	-
V20	PR41B	3	C	-	PR45B	3	C	-
W20	PR41A	3	T	-	PR45A	3	T	-
T17	PR40B	3	C[3]	-	PR44B	3	C[3]	-
T18	PR40A	3	T[3]	-	PR44A	3	T[3]	-
T19	PR39B	3	C[3]	-	PR43B	3	C[3]	-
T20	PR39A	3	T[3]	-	PR43A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
R18	PR38B	3	C	RLM0_PLLC_FB_A	PR42B	3	C	RLM0_PLLC_FB_A
R17	PR38A	3	T	RLM0_PLLT_FB_A	PR42A	3	T	RLM0_PLLT_FB_A
Y22	PR37B	3	C[3]	-	PR41B	3	C[3]	-
Y21	PR37A	3	T[3]	DQS	PR41A	3	T[3]	DQS
W22	PR36B	3	-	-	PR40B	3	-	-
W21	PR35A	3	-	VREF1_3	PR39A	3	-	VREF1_3
P17	PR34B	3	C[3]	-	PR38B	3	C[3]	-
P18	PR34A	3	T[3]	-	PR38A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
R19	PR33B	3	C	-	PR37B	3	C	-
R20	PR33A	3	T	-	PR37A	3	T	-
V22	PR32B	3	C[3]	-	PR36B	3	C[3]	-
V21	PR32A	3	T[3]	-	PR36A	3	T[3]	-
U22	PR30B	3	C[3]	-	PR34B	3	C[3]	-
U21	PR30A	3	T[3]	-	PR34A	3	T[3]	-
P19	PR29B	3	C	RLM0_PLLC_IN_A	PR33B	3	C	RLM0_PLLC_IN_A
P20	PR29A	3	T	RLM0_PLLT_IN_A	PR33A	3	T	RLM0_PLLT_IN_A
-	GNDIO3	3	-	-	GNDIO3	3	-	-
T22	PR28B	3	C[3]	-	PR32B	3	C[3]	-
T21	PR28A	3	T[3]	DQS	PR32A	3	T[3]	DQS
R22	PR27B	3	-	-	PR31B	3	-	-
R21	PR26A	3	-	VREF2_3	PR30A	3	-	VREF2_3
N19	PR25B	3	C[3]	-	PR29B	3	C[3]	-
N20	PR25A	3	T[3]	-	PR29A	3	T[3]	-
N18	PR24B	3	C	-	PR28B	3	C	-
M18	PR24A	3	T	-	PR28A	3	T	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
P22	PR23B	3	C[3]	-	PR27B	3	C[3]	-
P21	PR23A	3	T[3]	-	PR27A	3	T[3]	-
N22	-	-	-	-	PR26B	3	C[3]	-
N21	-	-	-	-	PR26A	3	T[3]	-
M19	-	-	-	-	PR25B	3	-	-
M20	GNDP1	-	-	-	GNDP1	-	-	-
L18	VCCP1	-	-	-	VCCP1	-	-	-
M21	-	-	-	-	PR24A	2	-	-
M22	PR22B	2	C[3]	-	PR23B	2	C[3]	-
L22	PR22A	2	T[3]	-	PR23A	2	T[3]	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
L19	-	-	-	-	PR22B	2	C[3]	-
L20	-	-	-	-	PR22A	2	T[3]	-
L21	PR21B	2	C	PCLKC2_0	PR21B	2	C	PCLKC2_0
K22	PR21A	2	T	PCLKT2_0	PR21A	2	T	PCLKT2_0

Commercial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15C-3F484C	300	1.8/2.5/3.3V	-3	fpBGA	484	COM	15.5K
LFXP15C-4F484C	300	1.8/2.5/3.3V	-4	fpBGA	484	COM	15.5K
LFXP15C-5F484C	300	1.8/2.5/3.3V	-5	fpBGA	484	COM	15.5K
LFXP15C-3F388C	268	1.8/2.5/3.3V	-3	fpBGA	388	COM	15.5K
LFXP15C-4F388C	268	1.8/2.5/3.3V	-4	fpBGA	388	COM	15.5K
LFXP15C-5F388C	268	1.8/2.5/3.3V	-5	fpBGA	388	COM	15.5K
LFXP15C-3F256C	188	1.8/2.5/3.3V	-3	fpBGA	256	COM	15.5K
LFXP15C-4F256C	188	1.8/2.5/3.3V	-4	fpBGA	256	COM	15.5K
LFXP15C-5F256C	188	1.8/2.5/3.3V	-5	fpBGA	256	COM	15.5K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20C-3F484C	340	1.8/2.5/3.3V	-3	fpBGA	484	COM	19.7K
LFXP20C-4F484C	340	1.8/2.5/3.3V	-4	fpBGA	484	COM	19.7K
LFXP20C-5F484C	340	1.8/2.5/3.3V	-5	fpBGA	484	COM	19.7K
LFXP20C-3F388C	268	1.8/2.5/3.3V	-3	fpBGA	388	COM	19.7K
LFXP20C-4F388C	268	1.8/2.5/3.3V	-4	fpBGA	388	COM	19.7K
LFXP20C-5F388C	268	1.8/2.5/3.3V	-5	fpBGA	388	COM	19.7K
LFXP20C-3F256C	188	1.8/2.5/3.3V	-3	fpBGA	256	COM	19.7K
LFXP20C-4F256C	188	1.8/2.5/3.3V	-4	fpBGA	256	COM	19.7K
LFXP20C-5F256C	188	1.8/2.5/3.3V	-5	fpBGA	256	COM	19.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3E-3Q208C	136	1.2V	-3	PQFP	208	COM	3.1K
LFXP3E-4Q208C	136	1.2V	-4	PQFP	208	COM	3.1K
LFXP3E-5Q208C	136	1.2V	-5	PQFP	208	COM	3.1K
LFXP3E-3T144C	100	1.2V	-3	TQFP	144	COM	3.1K
LFXP3E-4T144C	100	1.2V	-4	TQFP	144	COM	3.1K
LFXP3E-5T144C	100	1.2V	-5	TQFP	144	COM	3.1K
LFXP3E-3T100C	62	1.2V	-3	TQFP	100	COM	3.1K
LFXP3E-4T100C	62	1.2V	-4	TQFP	100	COM	3.1K
LFXP3E-5T100C	62	1.2V	-5	TQFP	100	COM	3.1K