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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6000
Total RAM Bits	73728
Number of I/O	100
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp6c-3t144c

Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In ¹
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output ¹

1. See Figure 2-2 for connection details.

2. Requires two PFUs.

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SP 16x2	ROM 16x1 x 2
PFF Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	N/A	ROM 16x1 x 2

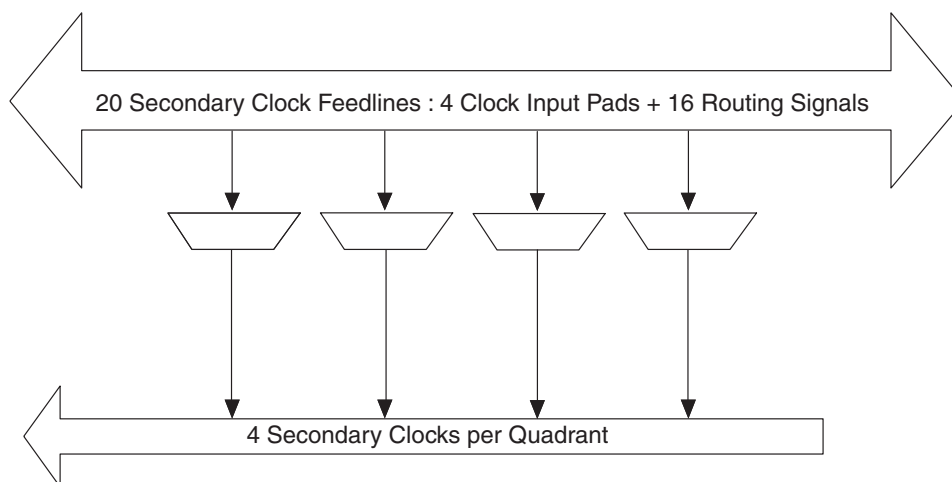
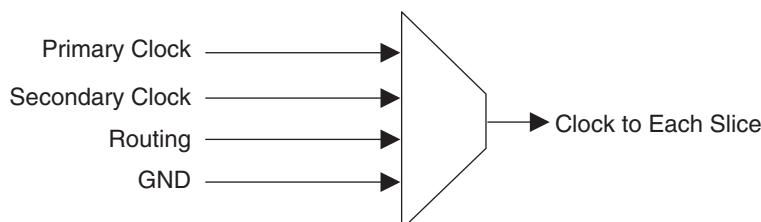
Logic Mode: In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other Slices.

Ripple Mode: Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Two additional signals: Carry Generate and Carry Propagate are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode: In this mode, distributed RAM can be constructed using each LUT block as a 16x1-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

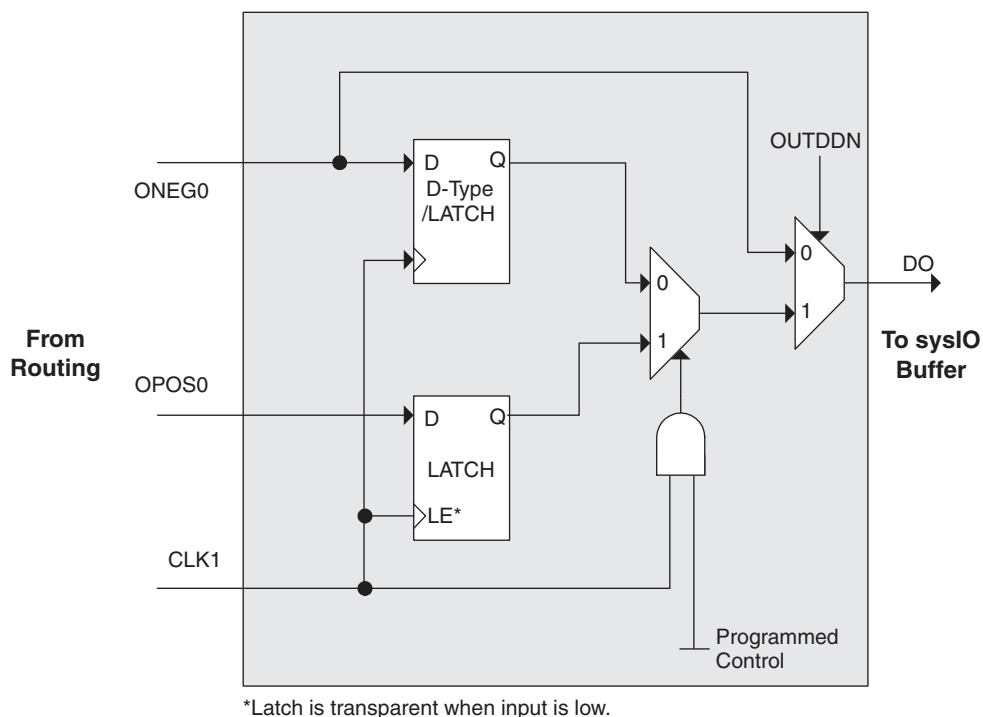
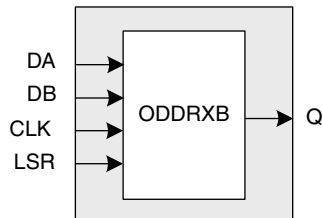
Figure 2-8. Per Quadrant Secondary Clock Selection**Figure 2-9. Slice Clock Selection**

sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signals to the feedback divider: from CLKOP (PLL internal), from clock net (CLKOP or CLKOS) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the t_{LOCK} parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

Figure 2-23. Output Register Block**Figure 2-24. ODDRXB Primitive****Tristate Register Block**

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-25 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Table 2-8. Supported Output Standards

Output Standard	Drive	V _{CCIO} (Nom.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVC MOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVC MOS25	4mA, 8mA, 12mA 16mA, 20mA	2.5
LVC MOS18	4mA, 8mA, 12mA 16mA	1.8
LVC MOS15	4mA, 8mA	1.5
LVC MOS12	2mA, 6mA	1.2
LVC MOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVC MOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVC MOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVC MOS15, Open Drain	4mA, 8mA	—
LVC MOS12, Open Drain	2mA, 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II, III	N/A	1.8
HSTL15 Class I, III	N/A	1.5
SSTL3 Class I, II	N/A	3.3
SSTL2 Class I, II	N/A	2.5
SSTL18 Class I	N/A	1.8
Differential Interfaces		
Differential SSTL3, Class I, II	N/A	3.3
Differential SSTL2, Class I, II	N/A	2.5
Differential SSTL18, Class I	N/A	1.8
Differential HSTL18, Class I, II, III	N/A	1.8
Differential HSTL15, Class I, III	N/A	1.5
LVDS	N/A	2.5
BLVDS ¹	N/A	2.5
LVPECL ¹	N/A	3.3

1. Emulated with external resistors.

Hot Socketing

The LatticeXP devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits, which allows easy integration with the rest of the system. These capabilities make the LatticeXP ideal for many multiple power supply and hot-swap applications.

Sleep Mode

The LatticeXP “C” devices (V_{CC} = 1.8/2.5/3.3V) have a sleep mode that allows standby current to be reduced by up to three orders of magnitude during periods of system inactivity. Entry and exit to Sleep Mode is controlled by the SLEEPN pin.

During Sleep Mode, the FPGA logic is non-operational, registers and EBR contents are not maintained and I/Os are tri-stated. Do not enter Sleep Mode during device programming or configuration operation. In Sleep Mode, power supplies can be maintained in their normal operating range, eliminating the need for external switching of power supplies. Table 2-9 compares the characteristics of Normal, Off and Sleep Modes.

Initialization Supply Current^{1, 2, 3, 4, 5, 6}**Over Recommended Operating Conditions**

Symbol	Parameter	Device	Typ. ⁷	Units
I_{CC}	Core Power Supply	LFXP3E	40	mA
		LFXP6E	50	mA
		LFXP10E	110	mA
		LFXP15E	140	mA
		LFXP20E	250	mA
		LFXP3C	60	mA
		LFXP6C	70	mA
		LFXP10C	150	mA
		LFXP15C	180	mA
		LFXP20C	290	mA
I_{CCAUX}	Auxiliary Power Supply $V_{CCAUX} = 3.3V$	LFXP3E/C	50	mA
		LFXP6E/C	60	mA
		LFXP10E/C	90	mA
		LFXP15 /C	110	mA
		LFXP20E/C	130	mA
I_{CCJ}	V_{CCJ} Power Supply	All	2	mA

1. Until DONE signal is active.

2. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.

3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

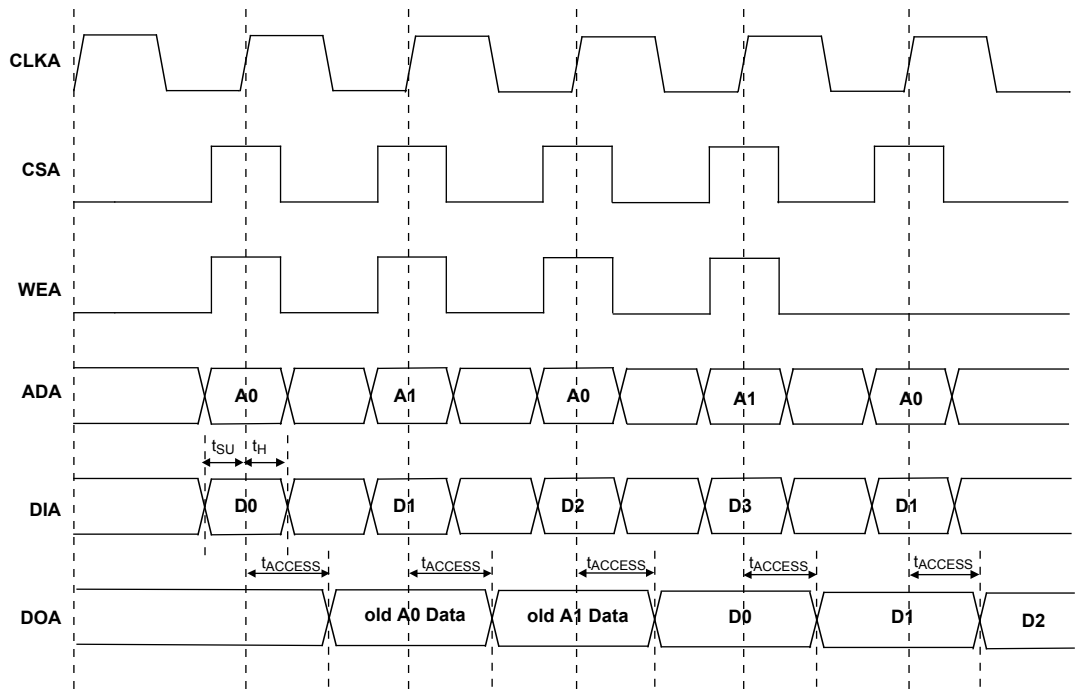
4. Frequency 0MHz.

5. Typical user pattern.

6. Assume normal bypass capacitor/decoupling capacitor across the supply.

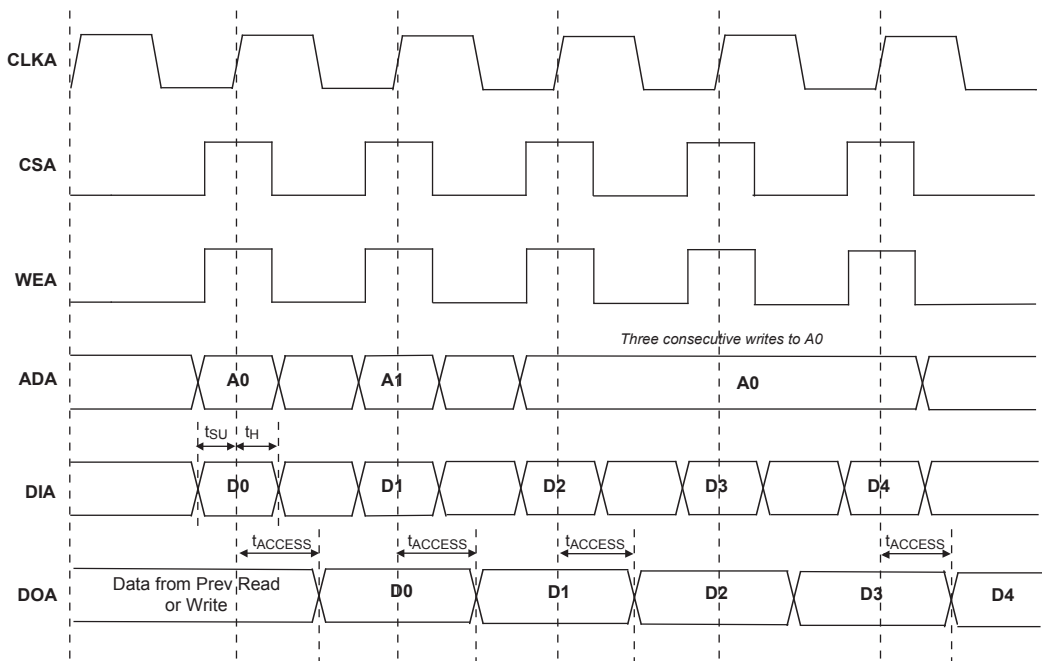
7. $T_A=25^{\circ}C$, power supplies at nominal voltage.

Figure 3-10. Read Before Write (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

Figure 3-11. Write Through (SP Read/Write On Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
P[Edge] [Row/Column Number*]_[A/B]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic. During configuration, the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
GSRN	I	Global RESET signal. (Active low). Any I/O pin can be configured to be GSRN.
NC	—	No connect.
GND	—	GND - Ground. Dedicated Pins.
V _{CC}	—	VCC - The power supply pins for core logic. Dedicated Pins.
V _{CCAUX}	—	V _{CCAUX} - The Auxiliary power supply pin. It powers all the differential and referenced input buffers. Dedicated Pins.
V _{CCP0}	—	Voltage supply pins for ULM0PLL (and LLM1PLL ¹).
V _{CCP1}	—	Voltage supply pins for URM0PLL (and LRM1PLL ¹).
GNDP0	—	Ground pins for ULM0PLL (and LLM1PLL ¹).
GNDP1	—	Ground pins for URM0PLL (and LRM1PLL ¹).
V _{CCIOx}	—	V _{CCIO} - The power supply pins for I/O bank x. Dedicated Pins.
V _{REF1(x)} , V _{REF2(x)}	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V _{REF} inputs. When not used, they may be used as I/O pins.
PLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_PLL[T, C]_IN_A	—	Reference clock (PLL) input Pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A, B, C...at each side.
[LOC][num]_PLL[T, C]_FB_A	—	Optional feedback (PLL) input Pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A, B, C...at each side.
PCLK[T, C]_[n:0]_[3:0]	—	Primary Clock Pads, T = true and C = complement, n per side, indexed by bank and 0, 1, 2, 3 within bank.
[LOC]DQS[num]	—	DQS input Pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = Ball function number. Any pad can be configured to be DQS output.

Pin Information Summary¹

Pin Type		XP3			XP6		
		100 TQFP	144 TQFP	208 PQFP	144 TQFP	208 PQFP	256 fpBGA
Single Ended User I/O		62	100	136	100	142	188
Differential Pair User I/O ²		19	35	56	35	58	80
Configuration	Dedicated	11	11	11	11	11	11
	Muxed	14	14	14	14	14	14
TAP		5	5	5	5	5	5
Dedicated (total without supplies)		6	6	6	6	6	6
V _{CC}		2	4	8	4	8	8
V _{CCAUX}		2	2	2	2	2	4
V _{CCPLL}		2	2	2	2	2	2
V _{CCIO}	Bank0	1	1	2	1	2	2
	Bank1	1	1	2	1	2	2
	Bank2	1	1	2	1	2	2
	Bank3	1	1	2	1	2	2
	Bank4	1	2	2	2	2	2
	Bank5	1	1	2	1	2	2
	Bank6	1	1	2	1	2	2
	Bank7	1	1	2	1	2	2
GND		10	13	24	13	24	24
GND _{PLL}		2	2	2	2	2	2
NC		0	0	6	0	0	0
Single Ended/Differential I/O per Bank ²	Bank0	8/2	12/3	20/8	12/3	20/8	26/11
	Bank1	9/0	12/2	18/6	12/2	18/6	26/11
	Bank2	8/3	12/5	14/6	12/5	17/7	21/9
	Bank3	6/2	13/5	14/6	13/5	14/6	21/9
	Bank4	5/2	14/6	21/9	14/6	21/9	26/11
	Bank5	12/4	12/4	21/9	12/4	21/9	26/11
	Bank6	4/2	13/5	14/6	13/5	17/7	21/9
	Bank7	10/4	12/5	14/6	12/5	14/6	21/9
V _{CCJ}		1	1	1	1	1	1

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.

2. The differential I/O per bank includes both dedicated LVDS and emulated LVDS pin pairs. Please see the Logic Signal Connections table for more information.

LFXP3 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	Pin Function	Bank	Differential	Dual Function
44	GNDIO4	4	-	-
45	PB15A	4	T	PCLKT4_0
46	PB15B	4	C	PCLKC4_0
47	VCCIO4	4	-	-
48	PB19A	4	T	DQS
49	PB19B	4	C	VREF1_4
50	PB24A	4	-	VREF2_4
51	PR18B	3	C ³	-
52	GNDIO3	3	-	-
53	PR18A	3	T ³	-
54	PR15B	3	-	VREF1_3
55	PR14A	3	-	VREF2_3
56	PR13B	3	C	-
57	PR13A	3	T	-
58	VCCIO3	3	-	-
59	GNDP1	-	-	-
60	VCCP1	-	-	-
61	PR9B	2	C	PCLKC2_0
62	PR9A	2	T	PCLKT2_0
63	PR8B	2	C	RUM0_PLLC_IN_A
64	PR8A	2	T	RUM0_PLLT_IN_A
65	VCCIO2	2	-	-
66	PR6B	2	-	VREF1_2
67	PR5A	2	-	VREF2_2
68	GNDIO2	2	-	-
69	PR3B	2	C	RUM0_PLLC_FB_A
70	PR3A	2	T	RUM0_PLLT_FB_A
71	VCCAUX	-	-	-
72	TDO	-	-	-
73	VCCJ	-	-	-
74	TDI	-	-	-
75	TMS	-	-	-
76	TCK	-	-	-
77	VCC	-	-	-
78	PT24A	1	-	-
79	PT23A	1	-	D0
80	PT22B	1	-	D1
81	PT21A	1	-	D2
82	VCCIO1	1	-	-
83	PT20B	1	-	D3
84	GNDIO1	1	-	-
85	PT17A	1	-	D4
86	PT16A	1	-	D5
87	PT15B	1	-	D6

LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
1	PROGRAMN	7	-	-	PROGRAMN	7	-	-
2	CCLK	7	-	-	CCLK	7	-	-
3	GND	-	-	-	GND	-	-	-
4	PL2A	7	T ³	-	PL2A	7	T ³	-
5	PL2B	7	C ³	-	PL2B	7	C ³	-
6	PL3A	7	T	LUM0_PLLT_FB_A	PL3A	7	T	LUM0_PLLT_FB_A
7	PL3B	7	C	LUM0_PLLC_FB_A	PL3B	7	C	LUM0_PLLC_FB_A
8	VCCIO7	7	-	-	VCCIO7	7	-	-
9	PL5A	7	-	VREF1_7	PL5A	7	-	VREF1_7
10	PL6B	7	-	VREF2_7	PL6B	7	-	VREF2_7
11	GNDIO7	7	-	-	GNDIO7	7	-	-
12	PL7A	7	T ³	DQS	PL7A	7	T ³	DQS
13	PL7B	7	C ³	-	PL7B	7	C ³	-
14	VCC	-	-	-	VCC	-	-	-
15	PL8A	7	T	LUM0_PLLT_IN_A	PL8A	7	T	LUM0_PLLT_IN_A
16	PL8B	7	C	LUM0_PLLC_IN_A	PL8B	7	C	LUM0_PLLC_IN_A
17	PL9A	7	T ³	-	PL9A	7	T ³	-
18	PL9B	7	C ³	-	PL9B	7	C ³	-
19	VCCP0	-	-	-	VCCP0	-	-	-
20	GNDP0	-	-	-	GNDP0	-	-	-
21	VCCIO6	6	-	-	VCCIO6	6	-	-
22	PL11A	6	T ³	-	PL16A	6	T ³	-
23	PL11B	6	C ³	-	PL16B	6	C ³	-
24	PL12A	6	T	PCLKT6_0	PL17A	6	T	PCLKT6_0
25	PL12B	6	C	PCLKC6_0	PL17B	6	C	PCLKC6_0
26	PL13A	6	T ³	-	PL18A	6	T ³	-
27	PL13B	6	C ³	-	PL18B	6	C ³	-
28	GNDIO6	6	-	-	GNDIO6	6	-	-
29	PL14A	6	-	VREF1_6	PL22A	6	-	VREF1_6
30	PL15B	6	-	VREF2_6	PL23B	6	-	VREF2_6
31	PL16A	6	T ³	DQS	PL24A	6	T ³	DQS
32	PL16B	6	C ³	-	PL24B	6	C ³	-
33	PL17A	6	-	-	PL25A	6	-	-
34	PL18A	6	T ³	-	PL26A	6	T ³	-
35	PL18B	6	C ³	-	PL26B	6	C ³	-
36	VCCAUX	-	-	-	VCCAUX	-	-	-
37	SLEEPN ¹ /TOE ²	-	-	-	SLEEPN ¹ /TOE ²	-	-	-
38	INITN	5	-	-	INITN	5	-	-
39	VCC	-	-	-	VCC	-	-	-
40	PB2B	5	-	VREF1_5	PB5B	5	-	VREF1_5
41	PB5B	5	-	VREF2_5	PB8B	5	-	VREF2_5
42	PB7A	5	T	-	PB10A	5	T	-
43	PB7B	5	C	-	PB10B	5	C	-
44	GNDIO5	5	-	-	GNDIO5	5	-	-
45	PB9A	5	-	-	PB12A	5	-	-
46	PB10B	5	-	-	PB13B	5	-	-

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
185	PT13A	0	T	CS1N	PT16A	0	T	CS1N
186	PT12B	0	C	PCLKC0_0	PT15B	0	C	PCLKC0_0
187	PT12A	0	T	PCLKT0_0	PT15A	0	T	PCLKT0_0
188	PT11B	0	C	-	PT14B	0	C	-
189	VCCIO0	0	-	-	VCCIO0	0	-	-
190	PT11A	0	T	DQS	PT14A	0	T	DQS
191	PT10B	0	-	-	PT13B	0	-	-
192	PT9A	0	-	DOUT	PT12A	0	-	DOUT
193	PT8B	0	C	-	PT11B	0	C	-
194	GNDIO0	0	-	-	GNDIO0	0	-	-
195	PT8A	0	T	WRITEN	PT11A	0	T	WRITEN
196	PT7B	0	C	-	PT10B	0	C	-
197	PT7A	0	T	VREF1_0	PT10A	0	T	VREF1_0
198	PT6B	0	C	-	PT9B	0	C	-
199	VCCIO0	0	-	-	VCCIO0	0	-	-
200	PT6A	0	T	DI	PT9A	0	T	DI
201	PT5B	0	C	-	PT8B	0	C	-
202	PT5A	0	T	CSN	PT8A	0	T	CSN
203	PT4B	0	C	-	PT7B	0	C	-
204	PT4A	0	T	-	PT7A	0	T	-
205	PT3B	0	-	VREF2_0	PT6B	0	-	VREF2_0
206	PT2B	0	-	-	PT5B	0	-	-
207	GND	-	-	-	GND	-	-	-
208	CFG0	0	-	-	CFG0	0	-	-

1. Applies to LFXP "C" only.
2. Applies to LFXP "E" only.
3. Supports dedicated LVDS outputs.

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP6				LFXP10			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
E16	TDO	-	-	-	TDO	-	-	-
D16	VCCJ	-	-	-	VCCJ	-	-	-
D14	TDI	-	-	-	TDI	-	-	-
C14	TMS	-	-	-	TMS	-	-	-
B14	TCK	-	-	-	TCK	-	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
A15	PT31B	1	C	-	PT35B	1	C	-
B15	PT31A	1	T	-	PT35A	1	T	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
D12	PT28A	1	-	VREF1_1	PT34B	1	C	VREF1_1
C11	PT30A	1	T	DQS	PT34A	1	T	DQS
A14	PT29B	1	-	-	PT33B	1	-	-
B13	PT30B	1	C	-	PT32A	1	-	-
F12	PT27B	1	C	-	PT31B	1	C	-
E11	PT27A	1	T	-	PT31A	1	T	-
A13	PT26B	1	C	-	PT30B	1	C	-
C13	PT26A	1	T	D0	PT30A	1	T	D0
-	GNDIO1	1	-	-	GNDIO1	1	-	-
C10	PT25B	1	C	D1	PT29B	1	C	D1
E10	PT25A	1	T	VREF2_1	PT29A	1	T	VREF2_1
A12	PT24B	1	C	-	PT28B	1	C	-
B12	PT24A	1	T	D2	PT28A	1	T	D2
C12	PT23B	1	C	D3	PT27B	1	C	D3
A11	PT23A	1	T	-	PT27A	1	T	-
B11	PT22B	1	C	-	PT26B	1	C	-
D11	PT22A	1	T	DQS	PT26A	1	T	DQS
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B9	PT21B	1	-	-	PT25B	1	-	-
D9	PT20A	1	-	D4	PT24A	1	-	D4
A10	PT19B	1	C	-	PT23B	1	C	-
B10	PT19A	1	T	D5	PT23A	1	T	D5
D10	PT18B	1	C	D6	PT22B	1	C	D6
A9	PT18A	1	T	-	PT22A	1	T	-
C9	PT17B	1	C	D7	PT21B	1	C	D7
C8	PT17A	1	T	-	PT21A	1	T	-
E9	PT16B	0	C	BUSY	PT20B	0	C	BUSY
-	GNDIO0	0	-	-	GNDIO0	0	-	-
B8	PT16A	0	T	CS1N	PT20A	0	T	CS1N
A8	PT15B	0	C	PCLKC0_0	PT19B	0	C	PCLKC0_0
A7	PT15A	0	T	PCLKT0_0	PT19A	0	T	PCLKT0_0
B7	PT14B	0	C	-	PT18B	0	C	-
C7	PT14A	0	T	DQS	PT18A	0	T	DQS

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L7	VCCIO5	5	-	-	VCCIO5	5	-	-
L8	VCCIO5	5	-	-	VCCIO5	5	-	-
J6	VCCIO6	6	-	-	VCCIO6	6	-	-
K6	VCCIO6	6	-	-	VCCIO6	6	-	-
G6	VCCIO7	7	-	-	VCCIO7	7	-	-
H6	VCCIO7	7	-	-	VCCIO7	7	-	-

1. Applies to LFXP "C" only.
2. Applies to LFXP "E" only.
3. Supports dedicated LVDS outputs.

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
U1	PL25A	6	T	LLM0_PLLT_IN_A	PL29A	6	T	LLM0_PLLT_IN_A	PL33A	6	T	LLM0_PLLT_IN_A
T2	PL25B	6	C	LLM0_PLLC_IN_A	PL29B	6	C	LLM0_PLLC_IN_A	PL33B	6	C	LLM0_PLLC_IN_A
V1	PL26A	6	T ³	-	PL30A	6	T ³	-	PL34A	6	T ³	-
U2	PL26B	6	C ³	-	PL30B	6	C ³	-	PL34B	6	C ³	-
W1	PL28A	6	T ³	-	PL32A	6	T ³	-	PL36A	6	T ³	-
V2	PL28B	6	C ³	-	PL32B	6	C ³	-	PL36B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	-	-	-	GNDIO6	6	-	-
P3	PL29A	6	T	-	PL33A	6	T	-	PL37A	6	T	-
P4	PL29B	6	C	-	PL33B	6	C	-	PL37B	6	C	-
Y1	PL30A	6	T ³	-	PL34A	6	T ³	-	PL38A	6	T ³	-
W2	PL30B	6	C ³	-	PL34B	6	C ³	-	PL38B	6	C ³	-
R3	PL31A	6	-	VREF2_6	PL35A	6	-	VREF2_6	PL39A	6	-	VREF2_6
R4	PL32B	6	-	-	PL36B	6	-	-	PL40B	6	-	-
T3	PL33A	6	T ³	DQS	PL37A	6	T ³	DQS	PL41A	6	T ³	DQS
T4	PL33B	6	C ³	-	PL37B	6	C ³	-	PL41B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
V4	PL34A	6	T	LLM0_PLLT_FB_A	PL38A	6	T	LLM0_PLLT_FB_A	PL42A	6	T	LLM0_PLLT_FB_A
V3	PL34B	6	C	LLM0_PLLC_FB_A	PL38B	6	C	LLM0_PLLC_FB_A	PL42B	6	C	LLM0_PLLC_FB_A
U4	PL35A	6	T ³	-	PL39A	6	T ³	-	PL43A	6	T ³	-
U3	PL35B	6	C ³	-	PL39B	6	C ³	-	PL43B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
W5	SLEEPN ¹ / TOE ²	-	-	-	SLEEPN ¹ / TOE ²	-	-	-	SLEEPN ¹ / TOE ²	-	-	-
Y2	INITN	5	-	-	INITN	5	-	-	INITN	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y3	-	-	-	-	PB3B	5	-	-	PB7B	5	-	-
W3	-	-	-	-	PB4A	5	T	-	PB8A	5	T	-
W4	-	-	-	-	PB4B	5	C	-	PB8B	5	C	-
AA2	-	-	-	-	PB5A	5	-	-	PB9A	5	-	-
AA1	-	-	-	-	PB6B	5	-	-	PB10B	5	-	-
W6	PB2A	5	-	-	PB7A	5	T	DQS	PB11A	5	T	DQS
W7	-	-	-	-	PB7B	5	C	-	PB11B	5	C	-
Y4	PB3A	5	T	-	PB8A	5	T	-	PB12A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y5	PB3B	5	C	-	PB8B	5	C	-	PB12B	5	C	-
AB2	PB4A	5	T	-	PB9A	5	T	-	PB13A	5	T	-
AA3	PB4B	5	C	-	PB9B	5	C	-	PB13B	5	C	-
AB3	PB5A	5	T	-	PB10A	5	T	-	PB14A	5	T	-
AA4	PB5B	5	C	-	PB10B	5	C	-	PB14B	5	C	-
W8	PB6A	5	T	-	PB11A	5	T	-	PB15A	5	T	-
W9	PB6B	5	C	-	PB11B	5	C	-	PB15B	5	C	-
AB4	PB7A	5	T	VREF1_5	PB12A	5	T	VREF1_5	PB16A	5	T	VREF1_5
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
AA5	PB7B	5	C	-	PB12B	5	C	-	PB16B	5	C	-
AB5	PB8A	5	-	-	PB13A	5	-	-	PB17A	5	-	-
Y6	PB9B	5	-	-	PB14B	5	-	-	PB18B	5	-	-
AA6	PB10A	5	T	DQS	PB15A	5	T	DQS	PB19A	5	T	DQS
AB6	PB10B	5	C	-	PB15B	5	C	-	PB19B	5	C	-
Y9	PB11A	5	T	-	PB16A	5	T	-	PB20A	5	T	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
Y10	PB11B	5	C	-	PB16B	5	C	-	PB20B	5	C	-
AA7	PB12A	5	T	-	PB17A	5	T	-	PB21A	5	T	-
AB7	PB12B	5	C	VREF2_5	PB17B	5	C	VREF2_5	PB21B	5	C	VREF2_5
Y7	PB13A	5	T	-	PB18A	5	T	-	PB22A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
AA8	PB13B	5	C	-	PB18B	5	C	-	PB22B	5	C	-
AB8	PB14A	5	T	-	PB19A	5	T	-	PB23A	5	T	-
Y8	PB14B	5	C	-	PB19B	5	C	-	PB23B	5	C	-
AB9	PB15A	5	T	-	PB20A	5	T	-	PB24A	5	T	-
AA9	PB15B	5	C	-	PB20B	5	C	-	PB24B	5	C	-
W10	PB16A	5	-	-	PB21A	5	-	-	PB25A	5	-	-
W11	PB17B	5	-	-	PB22B	5	-	-	PB26B	5	-	-
AB10	PB18A	5	T	DQS	PB23A	5	T	DQS	PB27A	5	T	DQS
AA10	PB18B	5	C	-	PB23B	5	C	-	PB27B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
AA11	PB19A	5	T	-	PB24A	5	T	-	PB28A	5	T	-
AB11	PB19B	5	C	-	PB24B	5	C	-	PB28B	5	C	-
Y11	PB20A	5	T	-	PB25A	5	T	-	PB29A	5	T	-
Y12	PB20B	5	C	-	PB25B	5	C	-	PB29B	5	C	-
AB12	PB21A	4	T	-	PB26A	4	T	-	PB30A	4	T	-
AA12	PB21B	4	C	-	PB26B	4	C	-	PB30B	4	C	-
AB13	PB22A	4	T	PCLKT4_0	PB27A	4	T	PCLKT4_0	PB31A	4	T	PCLKT4_0
AA13	PB22B	4	C	PCLKC4_0	PB27B	4	C	PCLKC4_0	PB31B	4	C	PCLKC4_0
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA14	PB23A	4	T	-	PB28A	4	T	-	PB32A	4	T	-
AB14	PB23B	4	C	-	PB28B	4	C	-	PB32B	4	C	-
W12	PB24A	4	-	-	PB29A	4	-	-	PB33A	4	-	-
W13	PB25B	4	-	-	PB30B	4	-	-	PB34B	4	-	-
AA15	PB26A	4	T	DQS	PB31A	4	T	DQS	PB35A	4	T	DQS
AB15	PB26B	4	C	VREF1_4	PB31B	4	C	VREF1_4	PB35B	4	C	VREF1_4
AA16	PB27A	4	T	-	PB32A	4	T	-	PB36A	4	T	-
AB16	PB27B	4	C	-	PB32B	4	C	-	PB36B	4	C	-
Y17	PB28A	4	T	-	PB33A	4	T	-	PB37A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA17	PB28B	4	C	-	PB33B	4	C	-	PB37B	4	C	-
Y13	PB29A	4	T	-	PB34A	4	T	-	PB38A	4	T	-
Y14	PB29B	4	C	-	PB34B	4	C	-	PB38B	4	C	-
AB17	PB30A	4	T	-	PB35A	4	T	-	PB39A	4	T	-
Y18	PB30B	4	C	-	PB35B	4	C	-	PB39B	4	C	-
AA18	PB31A	4	T	VREF2_4	PB36A	4	T	VREF2_4	PB40A	4	T	VREF2_4
AB18	PB31B	4	C	-	PB36B	4	C	-	PB40B	4	C	-
Y19	PB32A	4	-	-	PB37A	4	-	-	PB41A	4	-	-
AB19	PB33B	4	-	-	PB38B	4	-	-	PB42B	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA19	PB34A	4	T	DQS	PB39A	4	T	DQS	PB43A	4	T	DQS
Y20	PB34B	4	C	-	PB39B	4	C	-	PB43B	4	C	-
W14	PB35A	4	T	-	PB40A	4	T	-	PB44A	4	T	-
W15	PB35B	4	C	-	PB40B	4	C	-	PB44B	4	C	-
AB20	PB36A	4	T	-	PB41A	4	T	-	PB45A	4	T	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
M21	VCCP1	-	-	-	VCCP1	-	-	-	VCCP1	-	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
M22	PR18B	2	C ³	-	PR22B	2	C ³	-	PR22B	2	C ³	-
L22	PR18A	2	T ³	-	PR22A	2	T ³	-	PR22A	2	T ³	-
K22	PR17B	2	C	PCLKC2_0	PR21B	2	C	PCLKC2_0	PR21B	2	C	PCLKC2_0
K21	PR17A	2	T	PCLKT2_0	PR21A	2	T	PCLKT2_0	PR21A	2	T	PCLKT2_0
L19	PR16B	2	C ³	-	PR20B	2	C ³	-	PR20B	2	C ³	-
K20	PR16A	2	T ³	DQS	PR20A	2	T ³	DQS	PR20A	2	T ³	DQS
L20	PR15B	2	-	-	PR19B	2	-	-	PR19B	2	-	-
L21	PR14A	2	-	VREF1_2	PR18A	2	-	VREF1_2	PR18A	2	-	VREF1_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
J22	PR13B	2	C ³	-	PR17B	2	C ³	-	PR17B	2	C ³	-
J21	PR13A	2	T ³	-	PR17A	2	T ³	-	PR17A	2	T ³	-
H22	PR12B	2	C	RUM0_PLLC_IN_A	PR16B	2	C	RUM0_PLLC_IN_A	PR16B	2	C	RUM0_PLLC_IN_A
H21	PR12A	2	T	RUM0_PLLT_IN_A	PR16A	2	T	RUM0_PLLT_IN_A	PR16A	2	T	RUM0_PLLT_IN_A
K19	PR11B	2	C ³	-	PR15B	2	C ³	-	PR15B	2	C ³	-
J19	PR11A	2	T ³	-	PR15A	2	T ³	-	PR15A	2	T ³	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
J20	PR9B	2	C ³	-	PR13B	2	C ³	-	PR13B	2	C ³	-
H20	PR9A	2	T ³	-	PR13A	2	T ³	-	PR13A	2	T ³	-
H19	PR8B	2	C	-	PR12B	2	C	-	PR12B	2	C	-
G19	PR8A	2	T	-	PR12A	2	T	-	PR12A	2	T	-
G22	PR7B	2	C ³	-	PR11B	2	C ³	-	PR11B	2	C ³	-
G21	PR7A	2	T ³	DQS	PR11A	2	T ³	DQS	PR11A	2	T ³	DQS
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
F20	PR6B	2	-	-	PR10B	2	-	-	PR10B	2	-	-
G20	PR5A	2	-	VREF2_2	PR9A	2	-	VREF2_2	PR9A	2	-	VREF2_2
F22	PR4B	2	C ³	-	PR8B	2	C ³	-	PR8B	2	C ³	-
F21	PR4A	2	T ³	-	PR8A	2	T ³	-	PR8A	2	T ³	-
E22	PR3B	2	C	RUM0_PLLC_FB_A	PR7B	2	C	RUM0_PLLC_FB_A	PR7B	2	C	RUM0_PLLC_FB_A
E21	PR3A	2	T	RUM0_PLLT_FB_A	PR7A	2	T	RUM0_PLLT_FB_A	PR7A	2	T	RUM0_PLLT_FB_A
D22	PR2B	2	C ³	-	PR6B	2	C ³	-	PR6B	2	C ³	-
D21	PR2A	2	T ³	-	PR6A	2	T ³	-	PR6A	2	T ³	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-	GNDIO2	2	-	-
F19	TDO	-	-	-	TDO	-	-	-	TDO	-	-	-
E20	VCCJ	-	-	-	VCCJ	-	-	-	VCCJ	-	-	-
D20	TDI	-	-	-	TDI	-	-	-	TDI	-	-	-
D19	TMS	-	-	-	TMS	-	-	-	TMS	-	-	-
D18	TCK	-	-	-	TCK	-	-	-	TCK	-	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
E19	-	-	-	-	PT48A	1	-	-	PT52A	1	-	-
D17	-	-	-	-	PT47B	1	C	-	PT51B	1	C	-
D16	-	-	-	-	PT47A	1	T	DQS	PT51A	1	T	DQS
C16	-	-	-	-	PT46B	1	-	-	PT50B	1	-	-
C15	-	-	-	-	PT45A	1	-	-	PT49A	1	-	-
C17	-	-	-	-	PT44B	1	C	-	PT48B	1	C	-
C18	PT39A	1	-	-	PT44A	1	T	-	PT48A	1	T	-
C19	PT38B	1	C	-	PT43B	1	C	-	PT47B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
AB5	PB16A	5	T	-	PB20A	5	T	-
AB6	PB16B	5	C	-	PB20B	5	C	-
AA8	PB17A	5	T	-	PB21A	5	T	-
AA9	PB17B	5	C	VREF2_5	PB21B	5	C	VREF2_5
W10	PB18A	5	T	-	PB22A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
V10	PB18B	5	C	-	PB22B	5	C	-
AB7	PB19A	5	T	-	PB23A	5	T	-
AB8	PB19B	5	C	-	PB23B	5	C	-
AB9	PB20A	5	T	-	PB24A	5	T	-
AB10	PB20B	5	C	-	PB24B	5	C	-
Y10	PB21A	5	-	-	PB25A	5	-	-
AA10	PB22B	5	-	-	PB26B	5	-	-
W11	PB23A	5	T	DQS	PB27A	5	T	DQS
V11	PB23B	5	C	-	PB27B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y11	PB24A	5	T	-	PB28A	5	T	-
AA11	PB24B	5	C	-	PB28B	5	C	-
AB11	PB25A	5	T	-	PB29A	5	T	-
AB12	PB25B	5	C	-	PB29B	5	C	-
Y12	PB26A	4	T	-	PB30A	4	T	-
AA12	PB26B	4	C	-	PB30B	4	C	-
W12	PB27A	4	T	PCLKT4_0	PB31A	4	T	PCLKT4_0
V12	PB27B	4	C	PCLKC4_0	PB31B	4	C	PCLKC4_0
-	GNDIO4	4	-	-	GNDIO4	4	-	-
AB13	PB28A	4	T	-	PB32A	4	T	-
AB14	PB28B	4	C	-	PB32B	4	C	-
AA13	PB29A	4	-	-	PB33A	4	-	-
Y13	PB30B	4	-	-	PB34B	4	-	-
AB15	PB31A	4	T	DQS	PB35A	4	T	DQS
AB16	PB31B	4	C	VREF1_4	PB35B	4	C	VREF1_4
V13	PB32A	4	T	-	PB36A	4	T	-
W13	PB32B	4	C	-	PB36B	4	C	-
AA14	PB33A	4	T	-	PB37A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA15	PB33B	4	C	-	PB37B	4	C	-
AB17	PB34A	4	T	-	PB38A	4	T	-
AB18	PB34B	4	C	-	PB38B	4	C	-
W14	PB35A	4	T	-	PB39A	4	T	-
Y14	PB35B	4	C	-	PB39B	4	C	-
U14	PB36A	4	T	VREF2_4	PB40A	4	T	VREF2_4
V14	PB36B	4	C	-	PB40B	4	C	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
AB19	PB37A	4	-	-	PB41A	4	-	-
AB20	PB38B	4	-	-	PB42B	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
V15	PB39A	4	T	DQS	PB43A	4	T	DQS
U15	PB39B	4	C	-	PB43B	4	C	-
Y15	PB40A	4	T	-	PB44A	4	T	-
W15	PB40B	4	C	-	PB44B	4	C	-
AA16	PB41A	4	T	-	PB45A	4	T	-
AA17	PB41B	4	C	-	PB45B	4	C	-
AA18	PB42A	4	T	-	PB46A	4	T	-
AA19	PB42B	4	C	-	PB46B	4	C	-
Y16	PB43A	4	T	-	PB47A	4	T	-
W16	PB43B	4	C	-	PB47B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA20	PB44A	4	T	-	PB48A	4	T	-
AA21	PB44B	4	C	-	PB48B	4	C	-
Y17	PB45A	4	-	-	PB49A	4	-	-
Y18	PB46B	4	-	-	PB50B	4	-	-
Y19	PB47A	4	T	DQS	PB51A	4	T	DQS
Y20	PB47B	4	C	-	PB51B	4	C	-
V16	PB48A	4	T	-	PB52A	4	T	-
U16	PB48B	4	C	-	PB52B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
U18	-	-	-	-	PB53A	4	T	-
V18	-	-	-	-	PB53B	4	C	-
W19	-	-	-	-	PB54A	4	T	-
W18	-	-	-	-	PB54B	4	C	-
U17	-	-	-	-	PB55A	4	T	-
V17	-	-	-	-	PB55B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
W17	-	-	-	-	PB56A	4	-	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
V19	PR43A	3	-	-	PR47A	3	-	-
U20	PR42B	3	C ³	-	PR46B	3	C ³	-
U19	PR42A	3	T ³	-	PR46A	3	T ³	-
V20	PR41B	3	C	-	PR45B	3	C	-
W20	PR41A	3	T	-	PR45A	3	T	-
T17	PR40B	3	C ³	-	PR44B	3	C ³	-
T18	PR40A	3	T ³	-	PR44A	3	T ³	-
T19	PR39B	3	C ³	-	PR43B	3	C ³	-
T20	PR39A	3	T ³	-	PR43A	3	T ³	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-

Commercial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15E-3FN484C	300	1.2V	-3	fpBGA	484	COM	15.5K
LFXP15E-4FN484C	300	1.2V	-4	fpBGA	484	COM	15.5K
LFXP15E-5FN484C	300	1.2V	-5	fpBGA	484	COM	15.5K
LFXP15E-3FN388C	268	1.2V	-3	fpBGA	388	COM	15.5K
LFXP15E-4FN388C	268	1.2V	-4	fpBGA	388	COM	15.5K
LFXP15E-5FN388C	268	1.2V	-5	fpBGA	388	COM	15.5K
LFXP15E-3FN256C	188	1.2V	-3	fpBGA	256	COM	15.5K
LFXP15E-4FN256C	188	1.2V	-4	fpBGA	256	COM	15.5K
LFXP15E-5FN256C	188	1.2V	-5	fpBGA	256	COM	15.5K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20E-3FN484C	340	1.2V	-3	fpBGA	484	COM	19.7K
LFXP20E-4FN484C	340	1.2V	-4	fpBGA	484	COM	19.7K
LFXP20E-5FN484C	340	1.2V	-5	fpBGA	484	COM	19.7K
LFXP20E-3FN388C	268	1.2V	-3	fpBGA	388	COM	19.7K
LFXP20E-4FN388C	268	1.2V	-4	fpBGA	388	COM	19.7K
LFXP20E-5FN388C	268	1.2V	-5	fpBGA	388	COM	19.7K
LFXP20E-3FN256C	188	1.2V	-3	fpBGA	256	COM	19.7K
LFXP20E-4FN256C	188	1.2V	-4	fpBGA	256	COM	19.7K
LFXP20E-5FN256C	188	1.2V	-5	fpBGA	256	COM	19.7K

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3C-3QN208I	136	1.8/2.5/3.3V	-3	PQFP	208	IND	3.1K
LFXP3C-4QN208I	136	1.8/2.5/3.3V	-4	PQFP	208	IND	3.1K
LFXP3C-3TN144I	100	1.8/2.5/3.3V	-3	TQFP	144	IND	3.1K
LFXP3C-4TN144I	100	1.8/2.5/3.3V	-4	TQFP	144	IND	3.1K
LFXP3C-3TN100I	62	1.8/2.5/3.3V	-3	TQFP	100	IND	3.1K
LFXP3C-4TN100I	62	1.8/2.5/3.3V	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6C-3FN256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	5.8K
LFXP6C-4FN256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	5.8K
LFXP6C-3QN208I	142	1.8/2.5/3.3V	-3	PQFP	208	IND	5.8K
LFXP6C-4QN208I	142	1.8/2.5/3.3V	-4	PQFP	208	IND	5.8K
LFXP6C-3TN144I	100	1.8/2.5/3.3V	-3	TQFP	144	IND	5.8K
LFXP6C-4TN144I	100	1.8/2.5/3.3V	-4	TQFP	144	IND	5.8K

Date	Version	Section	Change Summary
September 2005 (cont.)	03.0 (cont.)	DC and Switching Characteristics (cont.)	Updated Typical Building Block Function Performance timing numbers.
			Updated External Switching Characteristics timing numbers.
			Updated Internal Timing Parameters.
			Updated LatticeXP Family timing adders.
			Updated LatticeXP "C" Sleep Mode timing numbers.
			Updated JTAG Port Timing numbers.
		Pinout Information	Added clarification to SLEEPN and TOE description.
			Clarification of dedicated LVDS outputs.
		Supplemental Information	Updated list of technical notes.
September 2005	03.1	Pinout Information	Power Supply and NC Connections table corrected VCCP1 pin number for 208 PQFP.
December 2005	04.0	Introduction	Moved data sheet from Advance to Final.
		Architecture	Added clarification to Typical I/O Behavior During Power-up section.
		DC and Switching Characteristics	Added clarification to Recommended Operating Conditions.
			Updated timing numbers.
		Pinout Information	Updated Signal Descriptions table.
			Added clarification to Differential I/O Per Bank.
			Updated Differential dedicated LVDS output support.
		Ordering Information	Added 208 PQFP lead-free package and ordering part numbers.
February 2006	04.1	Pinout Information	Corrected description of Signal Names VREF1(x) and VREF2(x).
March 2006	04.2	DC and Switching Characteristics	Corrected condition for IIL and IIH.
March 2006	04.3	DC and Switching Characteristics	Added clarification to Recommended Operating Conditions for VCCAUX.
April 2006	04.4	Pinout Information	Removed Bank designator "5" from SLEEPN/TOE ball function.
May 2006	04.5	DC and Switching Characteristics	Added footnote 2 regarding threshold level for PROGRAMN to sysCON-FIG Port Timing Specifications table.
June 2006	04.6	DC and Switching Characteristics	Corrected LVDS25E Output Termination Example.
August 2006	04.7	Architecture	Added clarification to Typical I/O Behavior During Power-Up section.
			Added clarification to Left and Right sysIO Buffer Pair section.
		DC and Switching Characteristics	Changes to LVDS25E Output Termination Example diagram.
December 2006	04.8	Architecture	EBR Asynchronous Reset section added.
February 2007	04.9	Architecture	Updated EBR Asynchronous Reset section.
July 2007	05.0	Introduction	Updated LatticeXP Family Selection Guide table.
		Architecture	Updated Typical I/O Behavior During Power-up text section.
		DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics table. Split out LVCMOS 1.2 by supply voltage.
November 2007	05.1	DC and Switching Characteristics	Added JTAG Port Timing Waveforms diagram.
		Pinout Information	Added Thermal Management text section.
		Supplemental Information	Updated title list.