Lattice Semiconductor Corporation - LFXP6C-4FN256C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6000
Total RAM Bits	73728
Number of I/O	188
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp6c-4fn256c

Figure 2-8. Per Quadrant Secondary Clock Selection

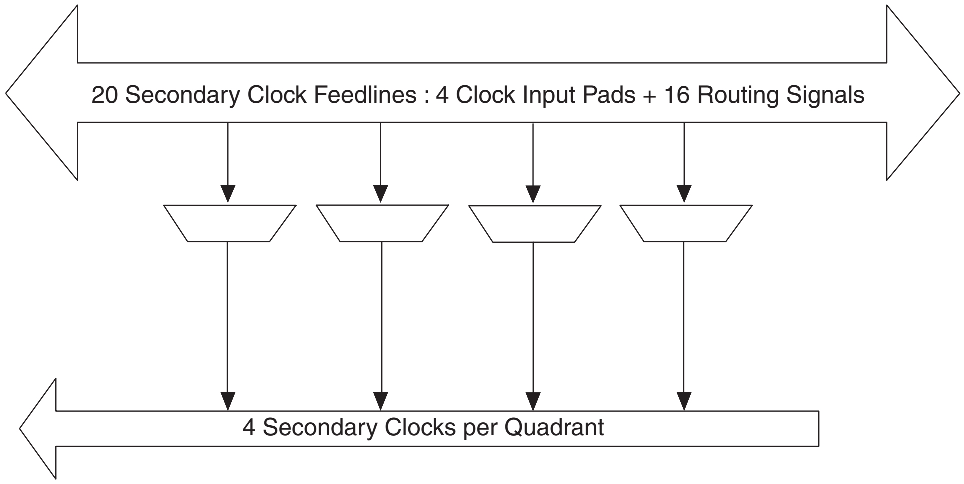
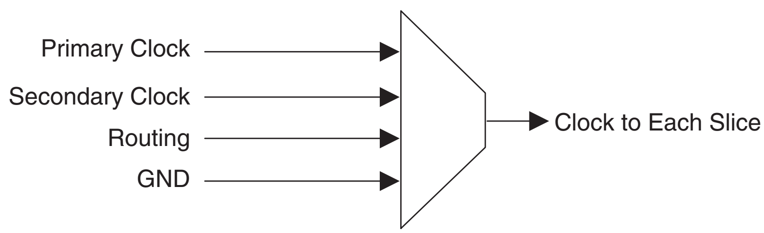


Figure 2-9. Slice Clock Selection



sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signals to the feedback divider: from CLKOP (PLL internal), from clock net (CLKOP or CLKOS) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the t_{LOCK} parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

Figure 2-26. DQS Local Bus

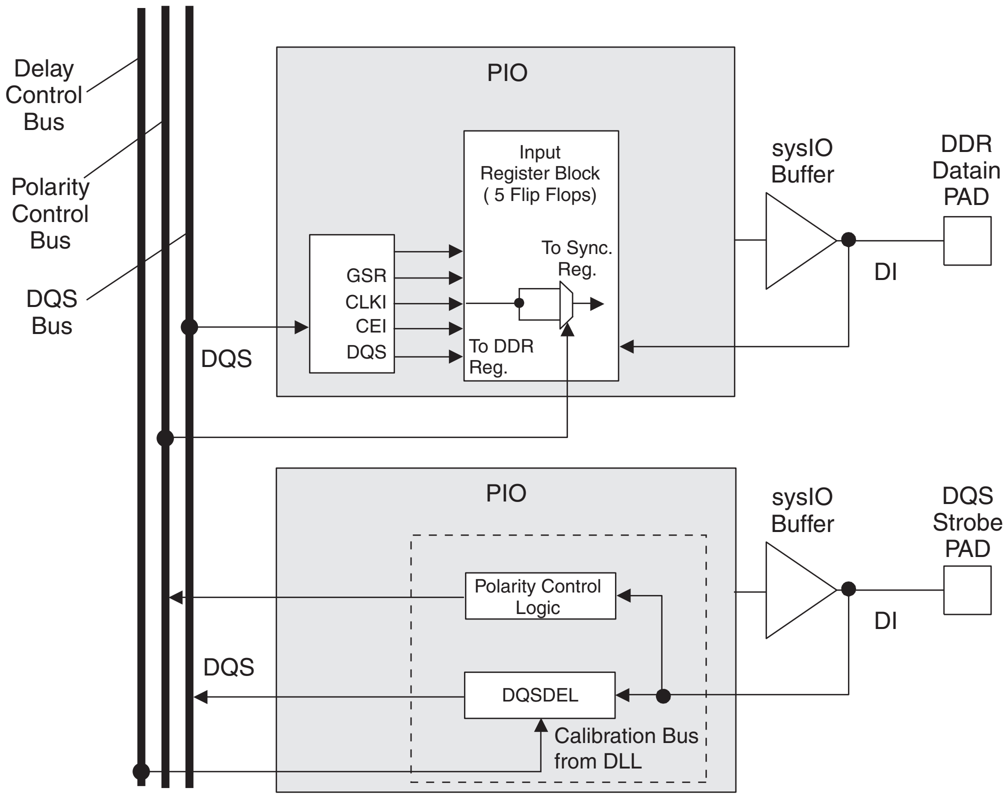


Figure 2-27. DLL Calibration Bus and DQS/DQS Transition Distribution

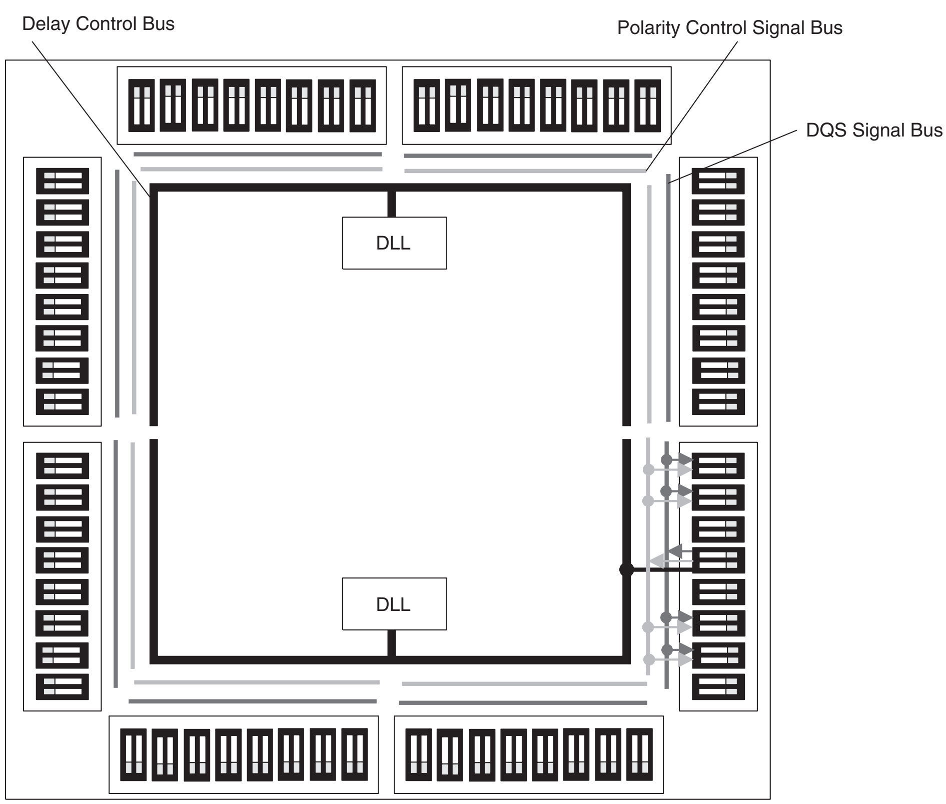


Figure 2-29 provides a pictorial representation of the different programming ports and modes available in the LatticeXP devices.

On power-up, the FPGA SRAM is ready to be configured with the sysCONFIG port active. The IEEE 1149.1 serial mode can be activated any time after power-up by sending the appropriate command through the TAP port.

Leave Alone I/O

When using 1532 mode for non-volatile memory programming, users may specify I/Os as high, low, tristated or held at current value. This provides excellent flexibility for implementing systems where reprogramming occurs on-the-fly.

TransFR (Transparent Field Reconfiguration)

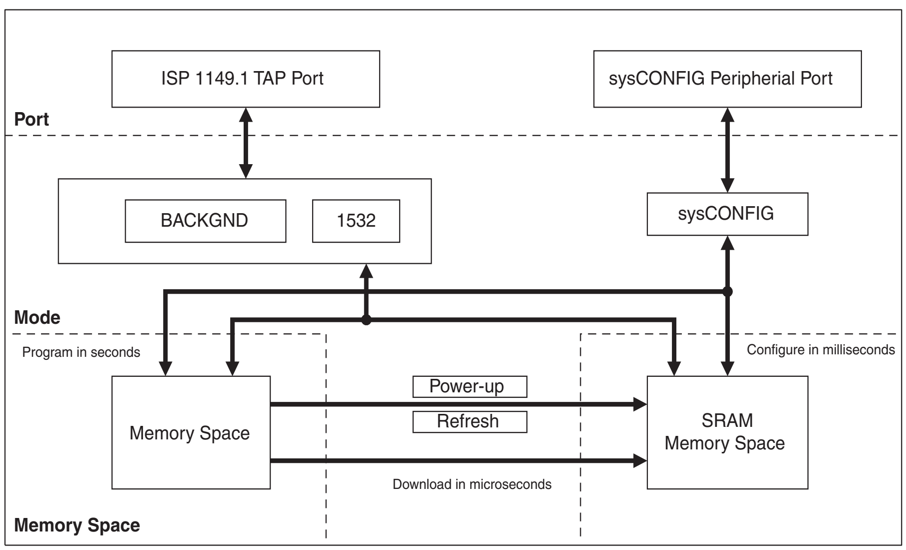
TransFR (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. See Lattice technical note #TN1087, *Minimizing System Interruption During Configuration Using TransFR Technology,* for details.

Security

The LatticeXP devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile memory spaces. Once set, the only way to clear security bits is to erase the memory space.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

Figure 2-29. ispXP Block Diagram



Internal Logic Analyzer Capability (ispTRACY)

All LatticeXP devices support an internal logic analyzer diagnostic feature. The diagnostic features provide capabilities similar to an external logic analyzer, such as programmable event and trigger condition and deep trace memory. This feature is enabled by Lattice's ispTRACY. The ispTRACY utility is added into the user design at compile time.

For more information on ispTRACY, please see information regarding additional technical documentation at the end of this data sheet.

Oscillator

Every LatticeXP device has an internal CMOS oscillator which is used to derive a master serial clock for configuration. The oscillator and the master serial clock run continuously in the configuration mode. The default value of the

Supply Current (Standby)[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LFXP3E	15	mA
		LFXP6E	20	mA
		LFXP10E	35	mA
		LFXP15E	45	mA
		LFXP20E	55	mA
		LFXP3C	35	mA
		LFXP6C	40	mA
		LFXP10C	70	mA
		LFXP15C	80	mA
		LFXP20C	90	mA
I_{CCP}	PLL Power Supply (per PLL)	All	8	mA
I_{CCAUX}	Auxiliary Power Supply V_{CCAUX} = 3.3V	LFXP3E/C	22	mA
		LFXP6E/C	22	mA
		LFXP10E/C	30	mA
		LFXP15E/C	30	mA
		LFXP20E/C	30	mA
I_{CCIO}	Bank Power Supply[6]	All	2	mA
I_{CCJ}	V_{CCJ} Power Supply	All	1	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the VCCIO or GND.
3. Frequency 0MHz.
4. User pattern: blank.
5. T_A=25°C, power supplies at nominal voltage.
6. Per bank.

Typical Building Block Function Performance[1]

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	-5 Timing	Units
Basic Functions		
16-bit decoder	6.1	ns
32-bit decoder	7.3	ns
64-bit decoder	8.2	ns
4:1 MUX	4.9	ns
8:1 MUX	5.3	ns
16:1 MUX	5.7	ns
32:1 MUX	6.3	ns

Register to Register Performance

Function	-5 Timing	Units
Basic Functions		
16-bit decoder	351	MHz
32-bit decoder	248	MHz
64-bit decoder	237	MHz
4:1 MUX	590	MHz
8:1 MUX	523	MHz
16:1 MUX	434	MHz
32:1 MUX	355	MHz
8-bit adder	343	MHz
16-bit adder	292	MHz
64-bit adder	130	MHz
16-bit counter	388	MHz
32-bit counter	295	MHz
64-bit counter	200	MHz
64-bit accumulator	164	MHz
Embedded Memory Functions		
Single Port RAM 256x36 bits	254	MHz
True-Dual Port RAM 512x18 bits	254	MHz
Distributed Memory Functions		
16x2 SP RAM	434	MHz
64x2 SP RAM	332	MHz
128x4 SP RAM	235	MHz
32x2 PDP RAM	322	MHz
64x4 PDP RAM	291	MHz

1. These timing numbers were generated using the ispLEVER design tool. Exact performance may vary with design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Timing v.F0.11

LatticeXP External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Device	-5 Min.	-5 Max.	-4 Min.	-4 Max.	-3 Min.	-3 Max.	Units
General I/O Pin Parameters (Using Primary Clock without PLL)[1]									
t_{CO}	Clock to Output - PIO Output Register	LFXP3	—	5.12	—	6.12	—	7.43	ns
		LFXP6	—	5.30	—	6.34	—	7.69	ns
		LFXP10	—	5.52	—	6.60	—	8.00	ns
		LFXP15	—	5.72	—	6.84	—	8.29	ns
		LFXP20	—	5.97	—	7.14	—	8.65	ns
t_{SU}	Clock to Data Setup - PIO Input Register	LFXP3	-0.40	—	-0.28	—	-0.16	—	ns
		LFXP6	-0.33	—	-0.32	—	-0.30	—	ns
		LFXP10	-0.61	—	-0.71	—	-0.81	—	ns
		LFXP15	-0.71	—	-0.77	—	-0.87	—	ns
		LFXP20	-0.95	—	-1.14	—	-1.35	—	ns
t_H	Clock to Data Hold - PIO Input Register	LFXP3	2.10	—	2.50	—	2.98	—	ns
		LFXP6	2.28	—	2.72	—	3.24	—	ns
		LFXP10	3.02	—	3.51	—	3.71	—	ns
		LFXP15	2.70	—	3.22	—	3.85	—	ns
		LFXP20	2.95	—	3.52	—	4.21	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Input Data Delay	LFXP3	2.38	—	2.49	—	2.66	—	ns
		LFXP6	2.92	—	3.18	—	3.42	—	ns
		LFXP10	2.72	—	2.75	—	2.84	—	ns
		LFXP15	2.99	—	3.13	—	3.18	—	ns
		LFXP20	4.47	—	4.56	—	4.80	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFXP3	-0.70	—	-0.80	—	-0.92	—	ns
		LFXP6	-0.47	—	-0.38	—	-0.31	—	ns
		LFXP10	-0.60	—	-0.47	—	-0.32	—	ns
		LFXP15	-1.05	—	-0.98	—	-1.01	—	ns
		LFXP20	-0.80	—	-0.58	—	-0.31	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All	—	400	—	360	—	320	MHz
DDR I/O Pin Parameters[2]									
t_{DVADQ}	Data Valid After DQS (DDR Read)	All	—	0.19	—	0.19	—	0.19	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	All	0.67	—	0.67	—	0.67	—	UI
t_{DQVBS}	Data Valid Before DQS	All	0.20	—	0.20	—	0.20	—	UI
t_{DQVAS}	Data Valid After DQS	All	0.20	—	0.20	—	0.20	—	UI
f_{MAX_DDR}	DDR Clock Frequency	All	95	166	95	133	95	100	MHz
Primary and Secondary Clocks									
f_{MAX_PRI}	Frequency for Primary Clock Tree	All	—	450	—	412	—	375	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All	1.19	—	1.19	—	1.19	—	ns
t_{SKEW_PRI}	Primary Clock Skew within an I/O Bank	LFXP3/6/10/15	—	250	—	300	—	350	ps
		LFXP20	—	300	—	350	—	400	ps

1. General timing numbers based on LVCMOS 2.5, 12mA.
2. DDR timing numbers based on SSTL I/O.

Timing v.F0.11

LatticeXP Internal Timing Parameters[1]

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t_{LUT4_PFU}	LUT4 Delay (A to D Inputs to F Output)	—	0.28	—	0.34	—	0.40	ns
t_{LUT6_PFU}	LUT6 Delay (A to D Inputs to OFX Output)	—	0.44	—	0.53	—	0.63	ns
t_{LSR_PFU}	Set/Reset to Output of PFU	—	0.90	—	1.08	—	1.29	ns
t_{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.13	—	0.15	—	0.19	—	ns
t_{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.04	—	-0.03	—	-0.03	—	ns
t_{SUD_PFU}	Clock to D Input Setup Time	0.13	—	0.16	—	0.19	—	ns
t_{HD_PFU}	Clock to D Input Hold Time	-0.03	—	-0.02	—	-0.02	—	ns
t_{CK2Q_PFU}	Clock to Q Delay, D-type Register Configuration	—	0.40	—	0.48	—	0.58	ns
t_{LE2Q_PFU}	Clock to Q Delay Latch Configuration	—	0.53	—	0.64	—	0.76	ns
t_{LD2Q_PFU}	D to Q Throughput Delay when Latch is Enabled	—	0.55	—	0.66	—	0.79	ns
PFU Dual Port Memory Mode Timing								
t_{CORAM_PFU}	Clock to Output	—	0.40	—	0.48	—	0.58	ns
t_{SUDATA_PFU}	Data Setup Time	-0.18	—	-0.14	—	-0.11	—	ns
t_{HDATA_PFU}	Data Hold Time	0.28	—	0.34	—	0.40	—	ns
t_{SUADDR_PFU}	Address Setup Time	-0.46	—	-0.37	—	-0.30	—	ns
t_{HADDR_PFU}	Address Hold Time	0.71	—	0.85	—	1.02	—	ns
t_{SUWREN_PFU}	Write/Read Enable Setup Time	-0.22	—	-0.17	—	-0.14	—	ns
t_{HWREN_PFU}	Write/Read Enable Hold Time	0.33	—	0.40	—	0.48	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t_{IN_PIO}	Input Buffer Delay	—	0.62	—	0.72	—	0.85	ns
t_{OUT_PIO}	Output Buffer Delay	—	2.12	—	2.54	—	3.05	ns
IOLOGIC Input/Output Timing								
t_{SUI_PIO}	Input Register Setup Time (Data Before Clock)	1.35	—	1.83	—	2.37	—	ns
t_{HI_PIO}	Input Register Hold Time (Data After Clock)	0.05	—	0.05	—	0.05	—	ns
t_{COO_PIO}	Output Register Clock to Output Delay	—	0.36	—	0.44	—	0.52	ns
t_{SUCE_PIO}	Input Register Clock Enable Setup Time	-0.09	—	-0.07	—	-0.06	—	ns
t_{HCE_PIO}	Input Register Clock Enable Hold Time	0.13	—	0.16	—	0.19	—	ns
t_{SULSR_PIO}	Set/Reset Setup Time	0.19	—	0.23	—	0.28	—	ns
t_{HLSR_PIO}	Set/Reset Hold Time	-0.14	—	-0.11	—	-0.09	—	ns
EBR Timing								
t_{CO_EBR}	Clock to Output from Address or Data	—	4.01	—	4.81	—	5.78	ns
t_{COO_EBR}	Clock to Output from EBR Output Register	—	0.81	—	0.97	—	1.17	ns
t_{SUDATA_EBR}	Setup Data to EBR Memory	-0.26	—	-0.21	—	-0.17	—	ns
t_{HDATA_EBR}	Hold Data to EBR Memory	0.41	—	0.49	—	0.59	—	ns
t_{SUADDR_EBR}	Setup Address to EBR Memory	-0.26	—	-0.21	—	-0.17	—	ns
t_{HADDR_EBR}	Hold Address to EBR Memory	0.41	—	0.49	—	0.59	—	ns
t_{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory	-0.17	—	-0.13	—	-0.11	—	ns
t_{HWREN_EBR}	Hold Write/Read Enable to EBR Memory	0.26	—	0.31	—	0.37	—	ns
t_{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.19	—	0.23	—	0.28	—	ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.13	—	-0.10	—	-0.08	—	ns

Timing Diagrams

PFU Timing Diagrams

Figure 3-6. Slice Single/Dual Port Write Cycle Timing

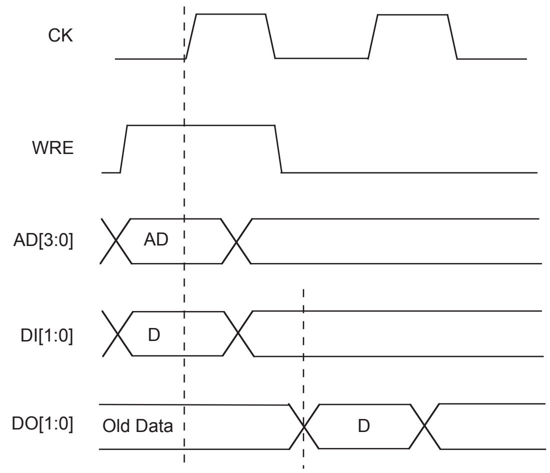
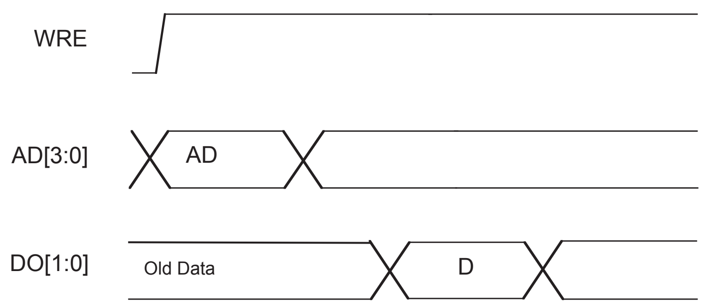


Figure 3-7. Slice Single /Dual Port Read Cycle Timing



Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions
Test and Programming (Dedicated pins. Pull-up is enabled on input pins during configuration.)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data in pin, used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence).
TDO	O	Output pin -Test Data out pin used to shift data out of device using 1149.1.
V_{CCJ}	—	V_{CCJ} - The power supply pin for JTAG Test Access Port.
Configuration Pads (used during sysCONFIG)		
CFG[1:0]	I	Mode pins used to specify configuration modes values latched on rising edge of INITN. During configuration, a pull-up is enabled.
INITN	I/O	Open Drain pin - Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. If CFG1 and CFG0 are high (SDM) then this pin is pulled low.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
DONE	I/O	Open Drain pin - Indicates that the configuration sequence is complete, and the startup sequence is in progress.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
BUSY	I/O	Generally not used. After configuration it is a user-programmable I/O pin.
CSN	I	sysCONFIG chip select (Active low). During configuration, a pull-up is enabled. After configuration it is user a programmable I/O pin.
CS1N	I	sysCONFIG chip select (Active Low). During configuration, a pull-up is enabled. After configuration it is user programmable I/O pin
WRITEN	I	Write Data on Parallel port (Active low). After configuration it is a user programmable I/O pin
D[7:0]	I/O	sysCONFIG Port Data I/O. After configuration these are user programmable I/O pins.
DOUT, CSON	O	Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port. After configuration, it is a user-programmable I/O pin.
DI	I	Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. After configuration it is a user-programmable I/O pin.
SLEEPN[2]	I	Sleep Mode pin - Active low sleep pin.þ When this pin is held high, the device operates normally.þ When driven low, the device moves into Sleep Mode after a specified time.This pin has a weak internal pull-up, but when not used an external pull-up to V_{CC} is recommended.
TOE[3]	I	Test Output Enable tri-states all I/O pins when driven low. This pin has a weak internal pull-up, but when not used an external pull-up to V_{CC} is recommended.

1. Applies toþ LFXP10, LFXP15 and LFXP20 only.
2. Applies to LFXP "C" devices only.
3. Applies to LFXP "E" devices only.

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA

	LFXP6				LFXP10			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
C2	PROGRAMN	7	-	-	PROGRAMN	7	-	-
C1	CCLK	7	-	-	CCLK	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
D2	PL3A	7	T	LUM0_PLLT_FB_A	PL3A	7	T	LUM0_PLLT_FB_A
D3	PL3B	7	C	LUM0_PLLC_FB_A	PL3B	7	C	LUM0_PLLC_FB_A
D1	PL2A	7	T[3]	-	PL5A	7	-	-
E2	PL5A	7	-	VREF1_7	PL6B	7	-	VREF1_7
-	GNDIO7	7	-	-	GNDIO7	7	-	-
E1	PL7A	7	T[3]	DQS	PL7A	7	T[3]	DQS
F1	PL7B	7	C[3]	-	PL7B	7	C[3]	-
E3	PL12A	7	T	-	PL8A	7	T	-
F4	PL12B	7	C	-	PL8B	7	C	-
F3	PL4A	7	T[3]	-	PL9A	7	T[3]	-
F2	PL4B	7	C[3]	-	PL9B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
G1	PL2B	7	C[3]	-	PL11B	7	-	-
G3	PL8A	7	T	LUM0_PLLT_IN_A	PL12A	7	T	LUM0_PLLT_IN_A
G2	PL8B	7	C	LUM0_PLLC_IN_A	PL12B	7	C	LUM0_PLLC_IN_A
H1	PL9A	7	T[3]	-	PL13A	7	T[3]	-
H2	PL9B	7	C[3]	-	PL13B	7	C[3]	-
G4	PL6B	7	-	VREF2_7	PL14A	7	-	VREF2_7
G5	PL14A	7	-	-	PL15B	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
J1	PL11A	7	T[3]	-	PL16A	7	T[3]	DQS
J2	PL11B	7	C[3]	-	PL16B	7	C[3]	-
H3	PL13A	7	T[3]	-	PL18A	7	T[3]	-
J3	PL13B	7	C[3]	-	PL18B	7	C[3]	-
H4	VCCP0	-	-	-	VCCP0	-	-	-
H5	GNDP0	-	-	-	GNDP0	-	-	-
K1	PL17A	6	T	PCLKT6_0	PL20A	6	T	PCLKT6_0
K2	PL17B	6	C	PCLKC6_0	PL20B	6	C	PCLKC6_0
-	GNDIO6	6	-	-	GNDIO6	6	-	-
J4	PL15B	6	-	-	PL22A	6	-	-
J5	PL22A	6	-	VREF1_6	PL23B	6	-	VREF1_6
L1	PL16A	6	T[3]	-	PL24A	6	T[3]	DQS
L2	PL16B	6	C[3]	-	PL24B	6	C[3]	-
M1	PL18A	6	T[3]	-	PL25A	6	T	LLM0_PLLT_IN_A
M2	PL18B	6	C[3]	-	PL25B	6	C	LLM0_PLLC_IN_A
K3	PL19A	6	T[3]	-	PL26A	6	T[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
L3	PL19B	6	C[3]	-	PL26B	6	C[3]	-
L4	PL21A	6	T[3]	-	PL28A	6	-	-

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

	LFXP6				LFXP10			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
K4	PL20A	6	T	-	PL29A	6	T	-
K5	PL20B	6	C	-	PL29B	6	C	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
N1	PL23B	6	-	VREF2_6	PL31A	6	-	VREF2_6
N2	PL21B	6	C[3]	-	PL32B	6	-	-
P1	PL24A	6	T[3]	DQS	PL33A	6	T[3]	DQS
P2	PL24B	6	C[3]	-	PL33B	6	C[3]	-
L5	PL25A	6	T	-	PL34A	6	T	LLM0_PLLT_FB_A
M6	PL25B	6	C	-	PL34B	6	C	LLM0_PLLC_FB_A
M3	PL26A	6	T[3]	-	PL35A	6	T[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
N3	PL26B	6	C[3]	-	PL35B	6	C[3]	-
P4	SLEEPN[1]/TOE[2]	-	-	-	SLEEPN[1]/TOE[2]	-	-	-
P3	INITN	5	-	-	INITN	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
R4	PB2A	5	T	-	PB6A	5	T	-
N5	PB2B	5	C	-	PB6B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
P5	PB5B	5	-	VREF1_5	PB7A	5	T	VREF1_5
R1	PB3B	5	C	-	PB7B	5	C	-
N6	PB4A	5	-	-	PB8A	5	-	-
M7	PB3A	5	T	-	PB9B	5	-	-
R2	PB6A	5	T	DQS	PB10A	5	T	DQS
T2	PB6B	5	C	-	PB10B	5	C	-
R3	PB7A	5	T	-	PB11A	5	T	-
T3	PB7B	5	C	-	PB11B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
T4	PB8A	5	T	-	PB12A	5	T	-
R5	PB8B	5	C	VREF2_5	PB12B	5	C	VREF2_5
N7	PB9A	5	T	-	PB13A	5	T	-
M8	PB9B	5	C	-	PB13B	5	C	-
T5	PB10A	5	T	-	PB14A	5	T	-
P6	PB10B	5	C	-	PB14B	5	C	-
T6	PB11A	5	T	-	PB15A	5	T	-
R6	PB11B	5	C	-	PB15B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
P7	PB12A	5	-	-	PB16A	5	-	-
N8	PB13B	5	-	-	PB17B	5	-	-
R7	PB14A	5	T	DQS	PB18A	5	T	DQS
T7	PB14B	5	C	-	PB18B	5	C	-
P8	PB15A	5	T	-	PB19A	5	T	-
T8	PB15B	5	C	-	PB19B	5	C	-

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

	LFXP6				LFXP10			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L15	PR21B	3	C[3]	-	PR28B	3	C[3]	-
L14	PR21A	3	T[3]	-	PR28A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
L12	PR17B	3	C	-	PR26A	3	-	-
M16	PR20B	3	C	-	PR25B	3	C	RLM0_PLLC_IN_A
N16	PR20A	3	T	-	PR25A	3	T	RLM0_PLLT_IN_A
K14	PR19B	3	C[3]	-	PR24B	3	C[3]	-
K15	PR19A	3	T[3]	-	PR24A	3	T[3]	DQS
K12	PR17A	3	T	-	PR23B	3	-	-
K13	PR22A	3	-	VREF2_3	PR22A	3	-	VREF2_3
-	GNDIO3	3	-	-	GNDIO3	3	-	-
L16	PR18B	3	C[3]	-	PR21B	3	C[3]	-
K16	PR18A	3	T[3]	-	PR21A	3	T[3]	-
J15	PR16B	3	C[3]	-	PR19B	3	C[3]	-
J14	PR16A	3	T[3]	-	PR19A	3	T[3]	-
J13	GNDP1	-	-	-	GNDP1	-	-	-
J12	VCCP1	-	-	-	VCCP1	-	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
J16	PR12B	2	C	PCLKC2_0	PR17B	2	C	PCLKC2_0
H16	PR12A	2	T	PCLKT2_0	PR17A	2	T	PCLKT2_0
H13	PR13B	2	C[3]	-	PR16B	2	C[3]	-
H12	PR13A	2	T[3]	-	PR16A	2	T[3]	DQS
H15	PR2B	2	C[3]	-	PR15B	2	-	-
H14	PR6B	2	-	VREF1_2	PR14A	2	-	VREF1_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G15	PR11B	2	C[3]	-	PR13B	2	C[3]	-
G14	PR11A	2	T[3]	-	PR13A	2	T[3]	-
G16	PR8B	2	C	RUM0_PLLC_IN_A	PR12B	2	C	RUM0_PLLC_IN_A
F16	PR8A	2	T	RUM0_PLLT_IN_A	PR12A	2	T	RUM0_PLLT_IN_A
G13	PR2A	2	T[3]	-	PR11B	2	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G12	PR9B	2	C[3]	-	PR8B	2	C	-
F13	PR9A	2	T[3]	-	PR8A	2	T	-
B16	PR7B	2	C[3]	-	PR7B	2	C[3]	-
C16	PR7A	2	T[3]	DQS	PR7A	2	T[3]	DQS
F15	PR14A	2	-	-	PR6B	2	-	-
E15	PR5A	2	-	VREF2_2	PR5A	2	-	VREF2_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
F14	PR4B	2	C[3]	-	PR4B	2	C[3]	-
E14	PR4A	2	T[3]	-	PR4A	2	T[3]	-
D15	PR3B	2	C	RUM0_PLLC_FB_A	PR3B	2	C	RUM0_PLLC_FB_A
C15	PR3A	2	T	RUM0_PLLT_FB_A	PR3A	2	T	RUM0_PLLT_FB_A

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

	LFXP6				LFXP10			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
K10	GND	-	-	-	GND	-	-	-
K7	GND	-	-	-	GND	-	-	-
K8	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-
L6	GND	-	-	-	GND	-	-	-
T1	GND	-	-	-	GND	-	-	-
T16	GND	-	-	-	GND	-	-	-
D13	VCC	-	-	-	VCC	-	-	-
D4	VCC	-	-	-	VCC	-	-	-
E12	VCC	-	-	-	VCC	-	-	-
E5	VCC	-	-	-	VCC	-	-	-
M12	VCC	-	-	-	VCC	-	-	-
M5	VCC	-	-	-	VCC	-	-	-
N13	VCC	-	-	-	VCC	-	-	-
N4	VCC	-	-	-	VCC	-	-	-
E13	VCCAUX	-	-	-	VCCAUX	-	-	-
E4	VCCAUX	-	-	-	VCCAUX	-	-	-
M13	VCCAUX	-	-	-	VCCAUX	-	-	-
M4	VCCAUX	-	-	-	VCCAUX	-	-	-
F7	VCCIO0	0	-	-	VCCIO0	0	-	-
F8	VCCIO0	0	-	-	VCCIO0	0	-	-
F10	VCCIO1	1	-	-	VCCIO1	1	-	-
F9	VCCIO1	1	-	-	VCCIO1	1	-	-
G11	VCCIO2	2	-	-	VCCIO2	2	-	-
H11	VCCIO2	2	-	-	VCCIO2	2	-	-
J11	VCCIO3	3	-	-	VCCIO3	3	-	-
K11	VCCIO3	3	-	-	VCCIO3	3	-	-
L10	VCCIO4	4	-	-	VCCIO4	4	-	-
L9	VCCIO4	4	-	-	VCCIO4	4	-	-
L7	VCCIO5	5	-	-	VCCIO5	5	-	-
L8	VCCIO5	5	-	-	VCCIO5	5	-	-
J6	VCCIO6	6	-	-	VCCIO6	6	-	-
K6	VCCIO6	6	-	-	VCCIO6	6	-	-
G6	VCCIO7	7	-	-	VCCIO7	7	-	-
H6	VCCIO7	7	-	-	VCCIO7	7	-	-

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

	LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
G10	GND	-	-	-	GND	-	-	-
G7	GND	-	-	-	GND	-	-	-
G8	GND	-	-	-	GND	-	-	-
G9	GND	-	-	-	GND	-	-	-
H10	GND	-	-	-	GND	-	-	-
H7	GND	-	-	-	GND	-	-	-
H8	GND	-	-	-	GND	-	-	-
H9	GND	-	-	-	GND	-	-	-
J10	GND	-	-	-	GND	-	-	-
J7	GND	-	-	-	GND	-	-	-
J8	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-
K10	GND	-	-	-	GND	-	-	-
K7	GND	-	-	-	GND	-	-	-
K8	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-
L6	GND	-	-	-	GND	-	-	-
T1	GND	-	-	-	GND	-	-	-
T16	GND	-	-	-	GND	-	-	-
D13	VCC	-	-	-	VCC	-	-	-
D4	VCC	-	-	-	VCC	-	-	-
E12	VCC	-	-	-	VCC	-	-	-
E5	VCC	-	-	-	VCC	-	-	-
M12	VCC	-	-	-	VCC	-	-	-
M5	VCC	-	-	-	VCC	-	-	-
N13	VCC	-	-	-	VCC	-	-	-
N4	VCC	-	-	-	VCC	-	-	-
E13	VCCAUX	-	-	-	VCCAUX	-	-	-
E4	VCCAUX	-	-	-	VCCAUX	-	-	-
M13	VCCAUX	-	-	-	VCCAUX	-	-	-
M4	VCCAUX	-	-	-	VCCAUX	-	-	-
F7	VCCIO0	0	-	-	VCCIO0	0	-	-
F8	VCCIO0	0	-	-	VCCIO0	0	-	-
F10	VCCIO1	1	-	-	VCCIO1	1	-	-
F9	VCCIO1	1	-	-	VCCIO1	1	-	-
G11	VCCIO2	2	-	-	VCCIO2	2	-	-
H11	VCCIO2	2	-	-	VCCIO2	2	-	-
J11	VCCIO3	3	-	-	VCCIO3	3	-	-
K11	VCCIO3	3	-	-	VCCIO3	3	-	-
L10	VCCIO4	4	-	-	VCCIO4	4	-	-
L9	VCCIO4	4	-	-	VCCIO4	4	-	-

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L7	VCCIO5	5	-	-	VCCIO5	5	-	-
L8	VCCIO5	5	-	-	VCCIO5	5	-	-
J6	VCCIO6	6	-	-	VCCIO6	6	-	-
K6	VCCIO6	6	-	-	VCCIO6	6	-	-
G6	VCCIO7	7	-	-	VCCIO7	7	-	-
H6	VCCIO7	7	-	-	VCCIO7	7	-	-

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

	LFXP10				LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
Y10	PB11B	5	C	-	PB16B	5	C	-	PB20B	5	C	-
AA7	PB12A	5	T	-	PB17A	5	T	-	PB21A	5	T	-
AB7	PB12B	5	C	VREF2_5	PB17B	5	C	VREF2_5	PB21B	5	C	VREF2_5
Y7	PB13A	5	T	-	PB18A	5	T	-	PB22A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
AA8	PB13B	5	C	-	PB18B	5	C	-	PB22B	5	C	-
AB8	PB14A	5	T	-	PB19A	5	T	-	PB23A	5	T	-
Y8	PB14B	5	C	-	PB19B	5	C	-	PB23B	5	C	-
AB9	PB15A	5	T	-	PB20A	5	T	-	PB24A	5	T	-
AA9	PB15B	5	C	-	PB20B	5	C	-	PB24B	5	C	-
W10	PB16A	5	-	-	PB21A	5	-	-	PB25A	5	-	-
W11	PB17B	5	-	-	PB22B	5	-	-	PB26B	5	-	-
AB10	PB18A	5	T	DQS	PB23A	5	T	DQS	PB27A	5	T	DQS
AA10	PB18B	5	C	-	PB23B	5	C	-	PB27B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
AA11	PB19A	5	T	-	PB24A	5	T	-	PB28A	5	T	-
AB11	PB19B	5	C	-	PB24B	5	C	-	PB28B	5	C	-
Y11	PB20A	5	T	-	PB25A	5	T	-	PB29A	5	T	-
Y12	PB20B	5	C	-	PB25B	5	C	-	PB29B	5	C	-
AB12	PB21A	4	T	-	PB26A	4	T	-	PB30A	4	T	-
AA12	PB21B	4	C	-	PB26B	4	C	-	PB30B	4	C	-
AB13	PB22A	4	T	PCLKT4_0	PB27A	4	T	PCLKT4_0	PB31A	4	T	PCLKT4_0
AA13	PB22B	4	C	PCLKC4_0	PB27B	4	C	PCLKC4_0	PB31B	4	C	PCLKC4_0
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA14	PB23A	4	T	-	PB28A	4	T	-	PB32A	4	T	-
AB14	PB23B	4	C	-	PB28B	4	C	-	PB32B	4	C	-
W12	PB24A	4	-	-	PB29A	4	-	-	PB33A	4	-	-
W13	PB25B	4	-	-	PB30B	4	-	-	PB34B	4	-	-
AA15	PB26A	4	T	DQS	PB31A	4	T	DQS	PB35A	4	T	DQS
AB15	PB26B	4	C	VREF1_4	PB31B	4	C	VREF1_4	PB35B	4	C	VREF1_4
AA16	PB27A	4	T	-	PB32A	4	T	-	PB36A	4	T	-
AB16	PB27B	4	C	-	PB32B	4	C	-	PB36B	4	C	-
Y17	PB28A	4	T	-	PB33A	4	T	-	PB37A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA17	PB28B	4	C	-	PB33B	4	C	-	PB37B	4	C	-
Y13	PB29A	4	T	-	PB34A	4	T	-	PB38A	4	T	-
Y14	PB29B	4	C	-	PB34B	4	C	-	PB38B	4	C	-
AB17	PB30A	4	T	-	PB35A	4	T	-	PB39A	4	T	-
Y18	PB30B	4	C	-	PB35B	4	C	-	PB39B	4	C	-
AA18	PB31A	4	T	VREF2_4	PB36A	4	T	VREF2_4	PB40A	4	T	VREF2_4
AB18	PB31B	4	C	-	PB36B	4	C	-	PB40B	4	C	-
Y19	PB32A	4	-	-	PB37A	4	-	-	PB41A	4	-	-
AB19	PB33B	4	-	-	PB38B	4	-	-	PB42B	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA19	PB34A	4	T	DQS	PB39A	4	T	DQS	PB43A	4	T	DQS
Y20	PB34B	4	C	-	PB39B	4	C	-	PB43B	4	C	-
W14	PB35A	4	T	-	PB40A	4	T	-	PB44A	4	T	-
W15	PB35B	4	C	-	PB40B	4	C	-	PB44B	4	C	-
AB20	PB36A	4	T	-	PB41A	4	T	-	PB45A	4	T	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

	LFXP10				LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
AA20	PB36B	4	C	-	PB41B	4	C	-	PB45B	4	C	-
AB21	PB37A	4	T	-	PB42A	4	T	-	PB46A	4	T	-
AA21	PB37B	4	C	-	PB42B	4	C	-	PB46B	4	C	-
AA22	PB38A	4	T	-	PB43A	4	T	-	PB47A	4	T	-
Y21	PB38B	4	C	-	PB43B	4	C	-	PB47B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
W16	PB39A	4	-	-	PB44A	4	T	-	PB48A	4	T	-
W17	-	-	-	-	PB44B	4	C	-	PB48B	4	C	-
Y15	-	-	-	-	PB45A	4	-	-	PB49A	4	-	-
Y16	-	-	-	-	PB46B	4	-	-	PB50B	4	-	-
W19	-	-	-	-	PB47A	4	T	DQS	PB51A	4	T	DQS
W18	-	-	-	-	PB47B	4	C	-	PB51B	4	C	-
W20	-	-	-	-	PB48A	4	-	-	PB52A	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-	GNDIO4	4	-	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
T20	PR35B	3	C[3]	-	PR39B	3	C[3]	-	PR43B	3	C[3]	-
T19	PR35A	3	T[3]	-	PR39A	3	T[3]	-	PR43A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
U19	PR34B	3	C	RLM0_PLLC_FB_A	PR38B	3	C	RLM0_PLLC_FB_A	PR42B	3	C	RLM0_PLLC_FB_A
U20	PR34A	3	T	RLM0_PLLT_FB_A	PR38A	3	T	RLM0_PLLT_FB_A	PR42A	3	T	RLM0_PLLT_FB_A
V19	PR33B	3	C[3]	-	PR37B	3	C[3]	-	PR41B	3	C[3]	-
V20	PR33A	3	T[3]	DQS	PR37A	3	T[3]	DQS	PR41A	3	T[3]	DQS
R19	PR32B	3	-	-	PR36B	3	-	-	PR40B	3	-	-
R20	PR31A	3	-	VREF1_3	PR35A	3	-	VREF1_3	PR39A	3	-	VREF1_3
W21	PR30B	3	C[3]	-	PR34B	3	C[3]	-	PR38B	3	C[3]	-
Y22	PR30A	3	T[3]	-	PR34A	3	T[3]	-	PR38A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
P19	PR29B	3	C	-	PR33B	3	C	-	PR37B	3	C	-
P20	PR29A	3	T	-	PR33A	3	T	-	PR37A	3	T	-
V21	PR28B	3	C[3]	-	PR32B	3	C[3]	-	PR36B	3	C[3]	-
W22	PR28A	3	T[3]	-	PR32A	3	T[3]	-	PR36A	3	T[3]	-
U21	PR26B	3	C[3]	-	PR30B	3	C[3]	-	PR34B	3	C[3]	-
V22	PR26A	3	T[3]	-	PR30A	3	T[3]	-	PR34A	3	T[3]	-
T21	PR25B	3	C	RLM0_PLLC_IN_A	PR29B	3	C	RLM0_PLLC_IN_A	PR33B	3	C	RLM0_PLLC_IN_A
U22	PR25A	3	T	RLM0_PLLT_IN_A	PR29A	3	T	RLM0_PLLT_IN_A	PR33A	3	T	RLM0_PLLT_IN_A
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
R21	PR24B	3	C[3]	-	PR28B	3	C[3]	-	PR32B	3	C[3]	-
T22	PR24A	3	T[3]	DQS	PR28A	3	T[3]	DQS	PR32A	3	T[3]	DQS
N19	PR23B	3	-	-	PR27B	3	-	-	PR31B	3	-	-
N20	PR22A	3	-	VREF2_3	PR26A	3	-	VREF2_3	PR30A	3	-	VREF2_3
R22	PR21B	3	C[3]	-	PR25B	3	C[3]	-	PR29B	3	C[3]	-
P22	PR21A	3	T[3]	-	PR25A	3	T[3]	-	PR29A	3	T[3]	-
P21	PR20B	3	C	-	PR24B	3	C	-	PR28B	3	C	-
N21	PR20A	3	T	-	PR24A	3	T	-	PR28A	3	T	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-	GNDIO3	3	-	-
M20	PR19B	3	C[3]	-	PR23B	3	C[3]	-	PR27B	3	C[3]	-
M19	PR19A	3	T[3]	-	PR23A	3	T[3]	-	PR27A	3	T[3]	-
N22	GNDP1	-	-	-	GNDP1	-	-	-	GNDP1	-	-	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

	LFXP10				LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
K11	GND	-	-	-	GND	-	-	-	GND	-	-	-
K12	GND	-	-	-	GND	-	-	-	GND	-	-	-
K13	GND	-	-	-	GND	-	-	-	GND	-	-	-
K14	GND	-	-	-	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-	GND	-	-	-
L10	GND	-	-	-	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-	GND	-	-	-
L12	GND	-	-	-	GND	-	-	-	GND	-	-	-
L13	GND	-	-	-	GND	-	-	-	GND	-	-	-
L14	GND	-	-	-	GND	-	-	-	GND	-	-	-
L9	GND	-	-	-	GND	-	-	-	GND	-	-	-
M10	GND	-	-	-	GND	-	-	-	GND	-	-	-
M11	GND	-	-	-	GND	-	-	-	GND	-	-	-
M12	GND	-	-	-	GND	-	-	-	GND	-	-	-
M13	GND	-	-	-	GND	-	-	-	GND	-	-	-
M14	GND	-	-	-	GND	-	-	-	GND	-	-	-
M9	GND	-	-	-	GND	-	-	-	GND	-	-	-
N10	GND	-	-	-	GND	-	-	-	GND	-	-	-
N11	GND	-	-	-	GND	-	-	-	GND	-	-	-
N12	GND	-	-	-	GND	-	-	-	GND	-	-	-
N13	GND	-	-	-	GND	-	-	-	GND	-	-	-
N14	GND	-	-	-	GND	-	-	-	GND	-	-	-
N9	GND	-	-	-	GND	-	-	-	GND	-	-	-
P10	GND	-	-	-	GND	-	-	-	GND	-	-	-
P11	GND	-	-	-	GND	-	-	-	GND	-	-	-
P12	GND	-	-	-	GND	-	-	-	GND	-	-	-
P13	GND	-	-	-	GND	-	-	-	GND	-	-	-
P14	GND	-	-	-	GND	-	-	-	GND	-	-	-
P9	GND	-	-	-	GND	-	-	-	GND	-	-	-
R10	GND	-	-	-	GND	-	-	-	GND	-	-	-
R11	GND	-	-	-	GND	-	-	-	GND	-	-	-
R12	GND	-	-	-	GND	-	-	-	GND	-	-	-
R13	GND	-	-	-	GND	-	-	-	GND	-	-	-
R14	GND	-	-	-	GND	-	-	-	GND	-	-	-
H9	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
J15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
J8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
K15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
K8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
L15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
L8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
M15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
M8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
N15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
N8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
P15	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
P8	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
R9	VCC	-	-	-	VCC	-	-	-	VCC	-	-	-
G16	VCCAUX	-	-	-	VCCAUX	-	-	-	VCCAUX	-	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

	LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
J21	PR20B	2	C[3]	-	PR20B	2	C[3]	-
J22	PR20A	2	T[3]	DQS	PR20A	2	T[3]	DQS
K18	PR19B	2	-	-	PR19B	2	-	-
K19	PR18A	2	-	VREF1_2	PR18A	2	-	VREF1_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
K21	PR17B	2	C[3]	-	PR17B	2	C[3]	-
K20	PR17A	2	T[3]	-	PR17A	2	T[3]	-
H21	PR16B	2	C	RUM0_PLLC_IN_A	PR16B	2	C	RUM0_PLLC_IN_A
H22	PR16A	2	T	RUM0_PLLT_IN_A	PR16A	2	T	RUM0_PLLT_IN_A
J20	PR15B	2	C[3]	-	PR15B	2	C[3]	-
J19	PR15A	2	T[3]	-	PR15A	2	T[3]	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
J17	PR13B	2	C[3]	-	PR13B	2	C[3]	-
J18	PR13A	2	T[3]	-	PR13A	2	T[3]	-
G21	PR12B	2	C	-	PR12B	2	C	-
G22	PR12A	2	T	-	PR12A	2	T	-
F21	PR11B	2	C[3]	-	PR11B	2	C[3]	-
F22	PR11A	2	T[3]	DQS	PR11A	2	T[3]	DQS
-	GNDIO2	2	-	-	GNDIO2	2	-	-
H20	PR10B	2	-	-	PR10B	2	-	-
H19	PR9A	2	-	VREF2_2	PR9A	2	-	VREF2_2
H17	PR8B	2	C[3]	-	PR8B	2	C[3]	-
H18	PR8A	2	T[3]	-	PR8A	2	T[3]	-
E21	PR7B	2	C	RUM0_PLLC_FB_A	PR7B	2	C	RUM0_PLLC_FB_A
E22	PR7A	2	T	RUM0_PLLT_FB_A	PR7A	2	T	RUM0_PLLT_FB_A
D21	PR6B	2	C[3]	-	PR6B	2	C[3]	-
D22	PR6A	2	T[3]	-	PR6A	2	T[3]	-
G20	PR5B	2	C[3]	-	PR5B	2	C[3]	-
G19	PR5A	2	T[3]	-	PR5A	2	T[3]	-
G17	PR4B	2	C	-	PR4B	2	C	-
G18	PR4A	2	T	-	PR4A	2	T	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
F18	PR3B	2	C[3]	-	PR3B	2	C[3]	-
F19	PR3A	2	T[3]	-	PR3A	2	T[3]	-
C22	PR2B	2	-	-	PR2B	2	-	-
F20	TDO	-	-	-	TDO	-	-	-
E20	VCCJ	-	-	-	VCCJ	-	-	-
D19	TDI	-	-	-	TDI	-	-	-
E19	TMS	-	-	-	TMS	-	-	-
D20	TCK	-	-	-	TCK	-	-	-
C20	-	-	-	-	PT56A	1	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following located on the Lattice website at www.latticesemi.com.

- Thermal Management document
- Technical Note TN1052 - Power Estimation and Management for LatticeECP/EC and LatticeXP Devices
- Power Calculator tool included with Lattice's ispLEVER design tool, or as a standalone download from www.latticesemi.com/software