Welcome to E-XFL.COM

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 6000 |
| Total RAM Bits | 73728 |
| Number of I/O | 142 |
| Number of Gates | - |
| Voltage - Supply | 1.71V ~ 3.465V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp6c-4q208c |

# LatticeXP Family Data Sheet Introduction

July 2007 Data Sheet DS1001

## Features

- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on – powers up in microseconds
  - No external configuration memory
  - Excellent design security, no bit stream to intercept
  - Reconfigure SRAM based logic in milliseconds
  - SRAM and non-volatile memory programmable through system configuration and JTAG ports
- **Sleep Mode**
  - Allows up to 1000x static current reduction
- **TransFR™ Reconfiguration (TFR)**
  - In-field logic update while system operates
- **Extensive Density and Package Options**
  - 3.1K to 19.7K LUT4s
  - 62 to 340 I/Os
  - Density migration supported
- **Embedded and Distributed Memory**
  - 54 Kbits to 396 Kbits sysMEM™ Embedded Block RAM
  - Up to 79 Kbits distributed RAM
  - Flexible memory resources:
    - Distributed and block memory
- **Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - SSTL 18 Class I
    - SSTL 3/2 Class I, II
    - HSTL15 Class I, III
    - HSTL 18 Class I, II, III
    - PCI
    - LVDS, Bus-LVDS, LVPECL, RSDS
- **Dedicated DDR Memory Support**
  - Implements interface up to DDR333 (166MHz)
- **sysCLOCK™ PLLs**
  - Up to 4 analog PLLs per device
  - Clock multiply, divide and phase shifting
- **System Level Support**
  - IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
  - Onboard oscillator for configuration
  - Devices operate with 3.3V, 2.5V, 1.8V or 1.2V power supply

***Table 1-1. LatticeXP Family Selection Guide***

| Device | LFXP3 | LFXP6 | LFXP10 | LFXP15 | LFXP20 |
|---|---|---|---|---|---|
| PFU/PFF Rows | 16 | 24 | 32 | 40 | 44 |
| PFU/PFF Columns | 24 | 30 | 38 | 48 | 56 |
| PFU/PFF (Total) | 384 | 720 | 1216 | 1932 | 2464 |
| LUTs (K) | 3 | 6 | 10 | 15 | 20 |
| Distributed RAM (KBits) | 12 | 23 | 39 | 61 | 79 |
| EBR SRAM (KBits) | 54 | 72 | 216 | 324 | 396 |
| EBR SRAM Blocks | 6 | 8 | 24 | 36 | 44 |
| $V_{CC}$ Voltage | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V | 1.2/1.8/2.5/3.3V |
| PLLs | 2 | 2 | 4 | 4 | 4 |
| Max. I/O | 136 | 188 | 244 | 300 | 340 |
| **Packages and I/O Combinations:** | | | | | |
| 100-pin TQFP (14 x 14 mm) | 62 | | | | |
| 144-pin TQFP (20 x 20 mm) | 100 | 100 | | | |
| 208-pin PQFP (28 x 28 mm) | 136 | 142 | | | |
| 256-ball fpBGA (17 x 17 mm) | | 188 | 188 | 188 | 188 |
| 388-ball fpBGA (23 x 23 mm) | | | 244 | 268 | 268 |
| 484-ball fpBGA (23 x 23 mm) | | | | 300 | 340 |

*Table 2-4. PFU Modes of Operation*

| Logic | Ripple | RAM[1] | ROM |
|---|---|---|---|
| LUT 4x8 or MUX 2x1 x 8 | 2-bit Add x 4 | SPR16x2 x 4 DPR16x2 x 2 | ROM16x1 x 8 |
| LUT 5x4 or MUX 4x1 x 4 | 2-bit Sub x 4 | SPR16x4 x 2 DPR16x4 x 1 | ROM16x2 x 4 |
| LUT 6x 2 or MUX 8x1 x 2 | 2-bit Counter x 4 | SPR16x8 x 1 | ROM16x4 x 2 |
| LUT 7x1 or MUX 16x1 x 1 | 2-bit Comp x 4 | | ROM16x8 x 1 |

1. These modes are not available in PFF blocks

### Routing

There are many resources provided in the LatticeXP devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal, vertical and diagonal directions. The x2 and x6 resources are buffered allowing both short and long connections routing between PFUs.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

## Clock Distribution Network

The clock inputs are selected from external I/O, the sysCLOCK™ PLLs or routing. These clock inputs are fed through the chip via a clock distribution system.

### Primary Clock Sources

LatticeXP devices derive clocks from three primary sources: PLL outputs, dedicated clock inputs and routing. LatticeXP devices have two to four sysCLOCK PLLs, located on the left and right sides of the device. There are four dedicated clock inputs, one on each side of the device. Figure 2-5 shows the 20 primary clock sources.

in selected blocks the input to the DQS delay block. If one of the bypass options is not chosen, the signal first passes through an optional delay block. This delay, if selected, ensures no positive input-register hold-time requirement when using a global clock.

The input block allows two modes of operation. In the single data rate (SDR) the data is registered, by one of the registers in the single data rate sync register block, with the system clock. In the DDR Mode two registers are used to sample the data on the positive and negative edges of the DQS signal creating two data streams, D0 and D2. These two data streams are synchronized with the system clock before entering the core. Further discussion on this topic is in the DDR Memory section of this data sheet.

Figure 2-21 shows the input register waveforms for DDR operation and Figure 2-22 shows the design tool primitives. The SDR/SYNC registers have reset and clock enable available.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to the system clock domain. For further discussion of this topic, see the DDR memory section of this data sheet.

***Figure 2-20. Input Register Diagram***

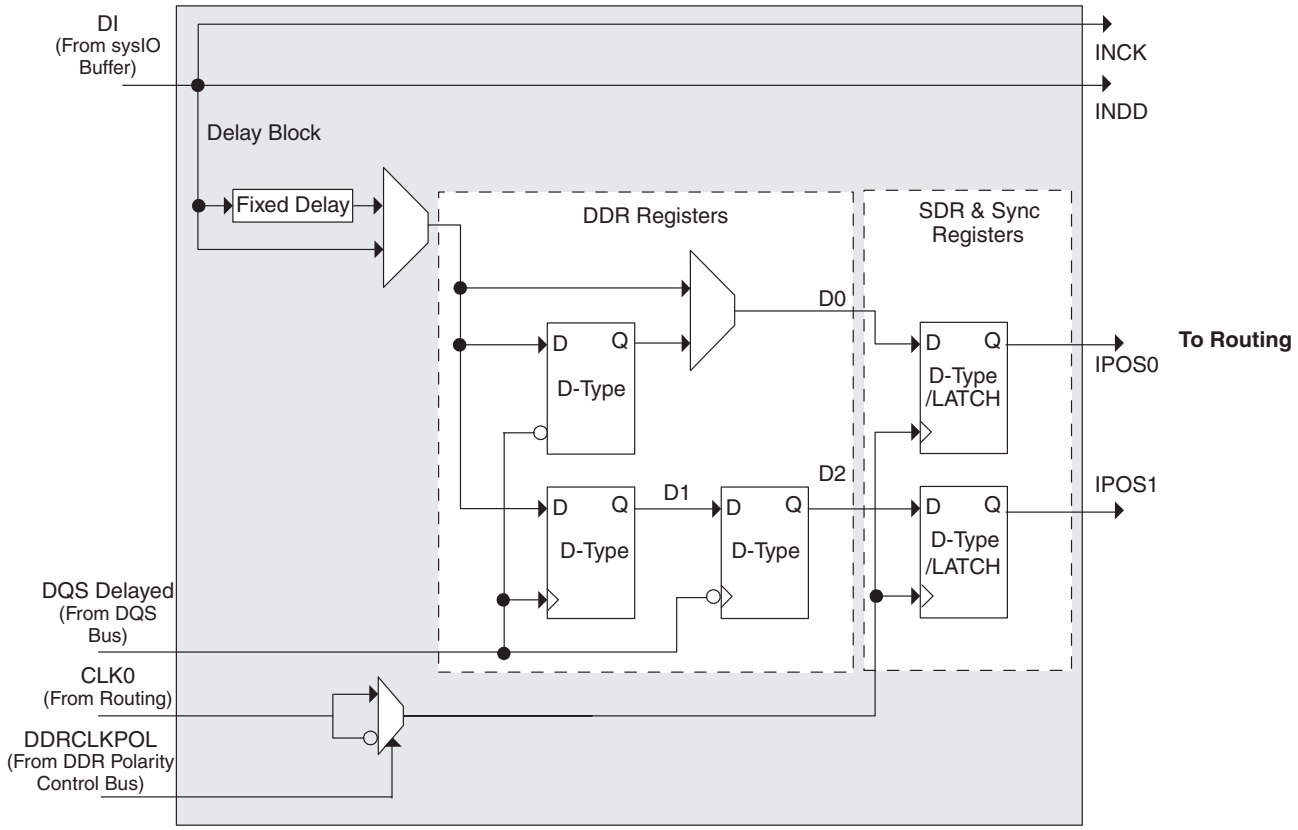


***Figure 2-21. Input Register DDR Waveforms***

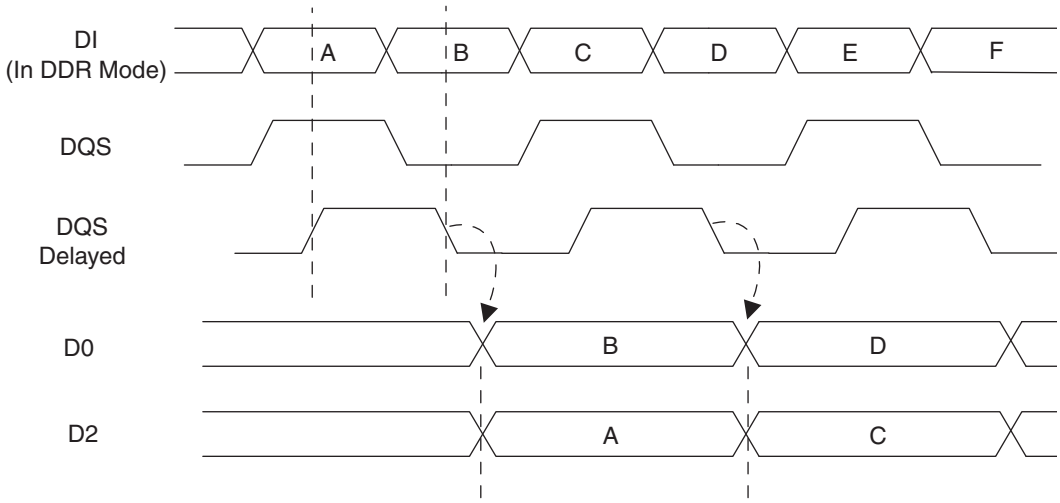
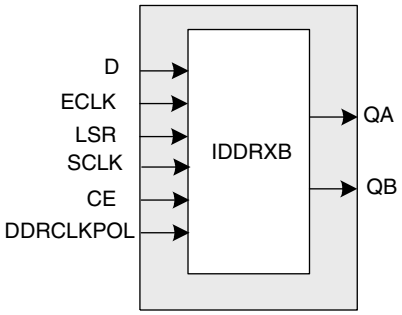



***Figure 2-22. INDDRXB Primitive***




**Output Register Block**

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-23 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or as a latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-24 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

# sysIO Differential Electrical Characteristics

## LVDS

**Over Recommended Operating Conditions**

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{INP}$, $V_{INM}$ | Input Voltage | | 0 | — | 2.4 | V |
| $V_{THD}$ | Differential Input Threshold | | +/-100 | — | — | mV |
| $V_{CM}$ | Input Common Mode Voltage | 100mV ≤ $V_{THD}$ | $V_{THD}$/2 | 1.2 | 1.8 | V |
| | | 200mV ≤ $V_{THD}$ | $V_{THD}$/2 | 1.2 | 1.9 | V |
| | | 350mV ≤ $V_{THD}$ | $V_{THD}$/2 | 1.2 | 2.0 | V |
| $I_{IN}$ | Input current | Power on or power off | — | — | +/-10 | µA |
| $V_{OH}$ | Output high voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 ohms | — | 1.38 | 1.60 | V |
| $V_{OL}$ | Output low voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 ohms | 0.9V | 1.03 | — | V |
| $V_{OD}$ | Output voltage differential | ($V_{OP}$ - $V_{OM}$), $R_T$ = 100 ohms | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ between high and low | | — | — | 50 | mV |
| $V_{OS}$ | Output voltage offset | ($V_{OP}$ - $V_{OM}$)/2, $R_T$ = 100 ohms | 1.125 | 1.25 | 1.375 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ between H and L | | — | — | 50 | mV |
| $I_{OSD}$ | Output short circuit current | $V_{OD}$ = 0V Driver outputs shorted | — | — | 6 | mA |

# LatticeXP Internal Timing Parameters[1]

**Over Recommended Operating Conditions**

| Parameter | Description | -5 | | -4 | | -3 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **PFU/PFF Logic Mode Timing** | | | | | | | | |
| $t_{LUT4\_PFU}$ | LUT4 Delay (A to D Inputs to F Output) | — | 0.28 | — | 0.34 | — | 0.40 | ns |
| $t_{LUT6\_PFU}$ | LUT6 Delay (A to D Inputs to OFX Output) | — | 0.44 | — | 0.53 | — | 0.63 | ns |
| $t_{LSR\_PFU}$ | Set/Reset to Output of PFU | — | 0.90 | — | 1.08 | — | 1.29 | ns |
| $t_{SUM\_PFU}$ | Clock to Mux (M0,M1) Input Setup Time | 0.13 | — | 0.15 | — | 0.19 | — | ns |
| $t_{HM\_PFU}$ | Clock to Mux (M0,M1) Input Hold Time | -0.04 | — | -0.03 | — | -0.03 | — | ns |
| $t_{SUD\_PFU}$ | Clock to D Input Setup Time | 0.13 | — | 0.16 | — | 0.19 | — | ns |
| $t_{HD\_PFU}$ | Clock to D Input Hold Time | -0.03 | — | -0.02 | — | -0.02 | — | ns |
| $t_{CK2Q\_PFU}$ | Clock to Q Delay, D-type Register Configuration | — | 0.40 | — | 0.48 | — | 0.58 | ns |
| $t_{LE2Q\_PFU}$ | Clock to Q Delay Latch Configuration | — | 0.53 | — | 0.64 | — | 0.76 | ns |
| $t_{LD2Q\_PFU}$ | D to Q Throughput Delay when Latch is Enabled | — | 0.55 | — | 0.66 | — | 0.79 | ns |
| **PFU Dual Port Memory Mode Timing** | | | | | | | | |
| $t_{CORAM\_PFU}$ | Clock to Output | — | 0.40 | — | 0.48 | — | 0.58 | ns |
| $t_{SUDATA\_PFU}$ | Data Setup Time | -0.18 | — | -0.14 | — | -0.11 | — | ns |
| $t_{HDATA\_PFU}$ | Data Hold Time | 0.28 | — | 0.34 | — | 0.40 | — | ns |
| $t_{SUADDR\_PFU}$ | Address Setup Time | -0.46 | — | -0.37 | — | -0.30 | — | ns |
| $t_{HADDR\_PFU}$ | Address Hold Time | 0.71 | — | 0.85 | — | 1.02 | — | ns |
| $t_{SUWREN\_PFU}$ | Write/Read Enable Setup Time | -0.22 | — | -0.17 | — | -0.14 | — | ns |
| $t_{HWREN\_PFU}$ | Write/Read Enable Hold Time | 0.33 | — | 0.40 | — | 0.48 | — | ns |
| **PIC Timing** | | | | | | | | |
| **PIO Input/Output Buffer Timing** | | | | | | | | |
| $t_{IN\_PIO}$ | Input Buffer Delay | — | 0.62 | — | 0.72 | — | 0.85 | ns |
| $t_{OUT\_PIO}$ | Output Buffer Delay | — | 2.12 | — | 2.54 | — | 3.05 | ns |
| **IOLOGIC Input/Output Timing** | | | | | | | | |
| $t_{SUI\_PIO}$ | Input Register Setup Time (Data Before Clock) | 1.35 | — | 1.83 | — | 2.37 | — | ns |
| $t_{HI\_PIO}$ | Input Register Hold Time (Data After Clock) | 0.05 | — | 0.05 | — | 0.05 | — | ns |
| $t_{COO\_PIO}$ | Output Register Clock to Output Delay | — | 0.36 | — | 0.44 | — | 0.52 | ns |
| $t_{SUCE\_PIO}$ | Input Register Clock Enable Setup Time | -0.09 | — | -0.07 | — | -0.06 | — | ns |
| $t_{HCE\_PIO}$ | Input Register Clock Enable Hold Time | 0.13 | — | 0.16 | — | 0.19 | — | ns |
| $t_{SULSR\_PIO}$ | Set/Reset Setup Time | 0.19 | — | 0.23 | — | 0.28 | — | ns |
| $t_{HLSR\_PIO}$ | Set/Reset Hold Time | -0.14 | — | -0.11 | — | -0.09 | — | ns |
| **EBR Timing** | | | | | | | | |
| $t_{CO\_EBR}$ | Clock to Output from Address or Data | — | 4.01 | — | 4.81 | — | 5.78 | ns |
| $t_{COO\_EBR}$ | Clock to Output from EBR Output Register | — | 0.81 | — | 0.97 | — | 1.17 | ns |
| $t_{SUDATA\_EBR}$ | Setup Data to EBR Memory | -0.26 | — | -0.21 | — | -0.17 | — | ns |
| $t_{HDATA\_EBR}$ | Hold Data to EBR Memory | 0.41 | — | 0.49 | — | 0.59 | — | ns |
| $t_{SUADDR\_EBR}$ | Setup Address to EBR Memory | -0.26 | — | -0.21 | — | -0.17 | — | ns |
| $t_{HADDR\_EBR}$ | Hold Address to EBR Memory | 0.41 | — | 0.49 | — | 0.59 | — | ns |
| $t_{SUWREN\_EBR}$ | Setup Write/Read Enable to EBR Memory | -0.17 | — | -0.13 | — | -0.11 | — | ns |
| $t_{HWREN\_EBR}$ | Hold Write/Read Enable to EBR Memory | 0.26 | — | 0.31 | — | 0.37 | — | ns |
| $t_{SUCE\_EBR}$ | Clock Enable Setup Time to EBR Output Register | 0.19 | — | 0.23 | — | 0.28 | — | ns |
| $t_{HCE\_EBR}$ | Clock Enable Hold Time to EBR Output Register | -0.13 | — | -0.10 | — | -0.08 | — | ns |

# LatticeXP Internal Timing Parameters[1] (Continued)

**Over Recommended Operating Conditions**

| Parameter | Description | -5 | | -4 | | -3 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RSTO\_EBR}$ | Reset To Output Delay Time from EBR Output Register | — | 1.61 | — | 1.94 | — | 2.32 | ns |
| **PLL Parameters** | | | | | | | | |
| $t_{RSTREC}$ | Reset Recovery to Rising Clock | 1.00 | — | 1.00 | — | 1.00 | — | ns |
| $t_{RSTSU}$ | Reset Signal Setup Time | 1.00 | — | 1.00 | — | 1.00 | — | ns |

1. Internal parameters are characterized but not tested on every device.

Timing v.F0.11

## Signal Descriptions

| Signal Name | I/O | Descriptions |
|---|---|---|
| **General Purpose** | | |
| P[Edge] [Row/Column Number*]_[A/B] | I/O | [Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).<br><br>[Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.<br><br>[A/B] indicates the PIO within the PIC to which the pad is connected.<br><br>Some of these user programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic.<br><br>During configuration, the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration. |
| GSRN | I | Global RESET signal. (Active low). Any I/O pin can be configured to be GSRN. |
| NC | — | No connect. |
| GND | — | GND - Ground. Dedicated Pins. |
| $V_{CC}$ | — | VCC - The power supply pins for core logic. Dedicated Pins. |
| $V_{CCAUX}$ | — | $V_{CCAUX}$ - The Auxiliary power supply pin. It powers all the differential and referenced input buffers. Dedicated Pins. |
| $V_{CCP0}$ | — | Voltage supply pins for ULM0PLL (and LLM1PLL[1]). |
| $V_{CCP1}$ | — | Voltage supply pins for URM0PLL (and LRM1PLL[1]). |
| GNDP0 | — | Ground pins for ULM0PLL (and LLM1PLL[1]). |
| GNDP1 | — | Ground pins for URM0PLL (and LRM1PLL[1]). |
| $V_{CCIOx}$ | — | $V_{CCIO}$ - The power supply pins for I/O bank x. Dedicated Pins. |
| $V_{REF1(x)}$, $V_{REF2(x)}$ | — | Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as $V_{REF}$ inputs. When not used, they may be used as I/O pins. |
| **PLL and Clock Functions** (Used as user programmable I/O pins when not in use for PLL or clock pins) | | |
| [LOC][num]_PLL[T, C]_IN_A | — | Reference clock (PLL) input Pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A, B, C...at each side. |
| [LOC][num]_PLL[T, C]_FB_A | — | Optional feedback (PLL) input Pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A, B, C...at each side. |
| PCLK[T, C]_[n:0]_[3:0] | — | Primary Clock Pads, T = true and C = complement, n per side, indexed by bank and 0,1, 2, 3 within bank. |
| [LOC]DQS[num] | — | DQS input Pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = Ball function number. Any pad can be configured to be DQS output. |

## PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

| PICs Associated with DQS Strobe | PIO within PIC | Polarity | DDR Strobe (DQS) and Data (DQ) Pins |
|---|---|---|---|
| P[Edge] [n-4] | A | True | DQ |
| | B | Complement | DQ |
| P[Edge] [n-3] | A | True | DQ |
| | B | Complement | DQ |
| P[Edge] [n-2] | A | True | DQ |
| | B | Complement | DQ |
| P[Edge] [n-1] | A | True | DQ |
| | | | |
| P[Edge] [n] | | | |
| | B | Complement | DQ |
| P[Edge] [n+1] | A | True | [Edge]DQSn |
| | B | Complement | DQ |
| P[Edge] [n+2] | A | True | DQ |
| | B | Complement | DQ |
| P[Edge] [n+3] | A | True | DQ |
| | B | Complement | DQ |

Notes:
1. “n” is a row/column PIC number.
2. The DDR interface is designed for memories that support one DQS strobe per eight bits of data. In some packages, all the potential DDR data (DQ) pins may not be available.
3. The definition of the PIC numbering is provided in the Signal Names column of the Signal Descriptions table in this data sheet.

## Pin Information Summary[1]

| Pin Type | | XP3 | | | XP6 | | |
|---|---|---|---|---|---|---|---|
| | | 100 TQFP | 144 TQFP | 208 PQFP | 144 TQFP | 208 PQFP | 256 fpBGA |
| Single Ended User I/O | | 62 | 100 | 136 | 100 | 142 | 188 |
| Differential Pair User I/O[2] | | 19 | 35 | 56 | 35 | 58 | 80 |
| Configuration | Dedicated | 11 | 11 | 11 | 11 | 11 | 11 |
| | Muxed | 14 | 14 | 14 | 14 | 14 | 14 |
| TAP | | 5 | 5 | 5 | 5 | 5 | 5 |
| Dedicated (total without supplies) | | 6 | 6 | 6 | 6 | 6 | 6 |
| $V_{CC}$ | | 2 | 4 | 8 | 4 | 8 | 8 |
| $V_{CCAUX}$ | | 2 | 2 | 2 | 2 | 2 | 4 |
| $V_{CCPLL}$ | | 2 | 2 | 2 | 2 | 2 | 2 |
| $V_{CCIO}$ | Bank0 | 1 | 1 | 2 | 1 | 2 | 2 |
| | Bank1 | 1 | 1 | 2 | 1 | 2 | 2 |
| | Bank2 | 1 | 1 | 2 | 1 | 2 | 2 |
| | Bank3 | 1 | 1 | 2 | 1 | 2 | 2 |
| | Bank4 | 1 | 2 | 2 | 2 | 2 | 2 |
| | Bank5 | 1 | 1 | 2 | 1 | 2 | 2 |
| | Bank6 | 1 | 1 | 2 | 1 | 2 | 2 |
| | Bank7 | 1 | 1 | 2 | 1 | 2 | 2 |
| GND | | 10 | 13 | 24 | 13 | 24 | 24 |
| $GND_{PLL}$ | | 2 | 2 | 2 | 2 | 2 | 2 |
| NC | | 0 | 0 | 6 | 0 | 0 | 0 |
| Single Ended/Differential I/O per Bank[2] | Bank0 | 8/2 | 12/3 | 20/8 | 12/3 | 20/8 | 26/11 |
| | Bank1 | 9/0 | 12/2 | 18/6 | 12/2 | 18/6 | 26/11 |
| | Bank2 | 8/3 | 12/5 | 14/6 | 12/5 | 17/7 | 21/9 |
| | Bank3 | 6/2 | 13/5 | 14/6 | 13/5 | 14/6 | 21/9 |
| | Bank4 | 5/2 | 14/6 | 21/9 | 14/6 | 21/9 | 26/11 |
| | Bank5 | 12/4 | 12/4 | 21/9 | 12/4 | 21/9 | 26/11 |
| | Bank6 | 4/2 | 13/5 | 14/6 | 13/5 | 17/7 | 21/9 |
| | Bank7 | 10/4 | 12/5 | 14/6 | 12/5 | 14/6 | 21/9 |
| $V_{CCJ}$ | | 1 | 1 | 1 | 1 | 1 | 1 |

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
2. The differential I/O per bank includes both dedicated LVDS and emulated LVDS pin pairs. Please see the Logic Signal Connections table for more information.

## Power Supply and NC Connections

| Signals | 100 TQFP | 144 TQFP | 208 PQFP | 256 fpBGA | 388 fpBGA | 484 fpBGA |
|---|---|---|---|---|---|---|
| $V_{CC}$ | 28, 77 | 14, 39, 73, 112 | 19, 35, 53, 80, 107, 151, 158, 182 | D4, D13, E5, E12, M5, M12, N4, N13 | H9, J8, J15, K8, K15, L8, L15, M8, M15, N8, N15, P8, P15, R9 | F10, F13, G9, G10, G13, G14, H8, H15, J7, J16, K6, K7, K16, K17, N6, N7, N16, N17, P7, P16, R8, R15, T9, T10, T13, T14, U10, U13 |
| $V_{CCIO0}$ | 94 | 133 | 189, 199 | F7, F8 | G8, G9, G10, G11, H8 | F11, G11, H10, H11 |
| $V_{CCIO1}$ | 82 | 119 | 167, 177 | F9, F10 | G12, G13, G14, G15, H15 | F12, G12, H12, H13 |
| $V_{CCIO2}$ | 65 | 98 | 140, 149 | G11, H11 | H16, J16, K16, L16 | K15, L15, L16, L17 |
| $V_{CCIO3}$ | 58 | 88 | 115, 125 | J11, K11 | M16, N16, P16, R16 | M15, M16, M17, N15 |
| $V_{CCIO4}$ | 47 | 61, 68 | 87, 97 | L9, L10 | R15, T12, T13, T14, T15 | R12, R13, T12, U12 |
| $V_{CCIO5}$ | 38 | 49 | 64, 74 | L7, L8 | R8, T8, T9, T10, T11 | R10, R11, T11, U11 |
| $V_{CCIO6}$ | 22 | 21 | 28, 41 | J6, K6 | M7, N7, P7, R7 | M6, M7, M8, N8 |
| $V_{CCIO7}$ | 7 | 8 | 13, 23 | G6, H6 | H7, J7, K7, L7 | K8, L6, L7, L8 |
| $V_{CCJ}$ | 73 | 108 | 154 | D16 | E20 | E20 |
| $V_{CCP0}$ | 17 | 19 | 25 | H4 | M2 | L5 |
| $V_{CCP1}$ | 60 | 91 | 128 | J12 | M21 | L18 |
| $V_{CCAUX}$ | 25, 71 | 36, 106 | 50, 152 | E4, E13, M4, M13 | G7, G16, T7, T16 | G7, G8, G15, G16, H7, H16, R7, R16, T7, T8, T15, T16 |
| GND[1] | 10, 18, 21, 33, 43, 44, 52, 59, 68, 84, 90, 99 | 3, 11, 20, 28, 44, 54, 56, 64, 75, 85, 90, 101, 121, 127, 136 | 5, 7, 16, 26, 38, 47, 49, 59, 69, 79, 82, 92, 106, 109, 118, 121, 127, 130, 135, 143, 163, 172, 181, 184, 194, 207 | A1, A16, F6, F11, G7, G8, G9, G10, H5, H7, H8, H9, H10, J7, J8, J9, J10, J13, K7, K8, K9, K10, L6, L11, T1, T16 | A1, A22, H10, H11, H12, H13, H14, J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N1, N9, N10, N11, N12, N13, N14, N22, P9, P10, P11, P12, P13, P14, R10, R11, R12, R13, R14, AB1, AB22 | A1, A2, A21, A22, B1, B22, H9, H14, J8, J9, J10, J11, J12, J13, J14, J15, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, M20, N2, N9, N10, N11, N12, N13, N14, P8, P9, P10, P11, P12, P13, P14, P15, R9, R14, AA1, AA22, AB1, AB2, AB21, AB22 |
| NC[2] | — | — | XP3: 27, 33, 34, 129, 133, 134 | — | XP10: C2, C15, C16, C17, D4, D5, D6, D7, D16, D17, E4, E19, W3, W4, W7, W17, W18, W19, W20, Y3, Y15, Y16, AA1, AA2 | XP15: B21, C4, C5, C6, C18, C19, C20, C21, D6, D18, E4, E6, E18, F6, L1, L19, L20, M1, M2, M19, M21, N1, N21, N22, P1, P2, U5, U6, U17, U18, V5, V6, V17, V18, W17, W18, W19, Y3, Y4, Y5 |

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, $V_{CC}$ or GND.

## LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFXP6 | | | | LFXP10 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| E16 | TDO | - | - | - | TDO | - | - | - |
| D16 | VCCJ | - | - | - | VCCJ | - | - | - |
| D14 | TDI | - | - | - | TDI | - | - | - |
| C14 | TMS | - | - | - | TMS | - | - | - |
| B14 | TCK | - | - | - | TCK | - | - | - |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| A15 | PT31B | 1 | C | - | PT35B | 1 | C | - |
| B15 | PT31A | 1 | T | - | PT35A | 1 | T | - |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| D12 | PT28A | 1 | - | VREF1_1 | PT34B | 1 | C | VREF1_1 |
| C11 | PT30A | 1 | T | DQS | PT34A | 1 | T | DQS |
| A14 | PT29B | 1 | - | - | PT33B | 1 | - | - |
| B13 | PT30B | 1 | C | - | PT32A | 1 | - | - |
| F12 | PT27B | 1 | C | - | PT31B | 1 | C | - |
| E11 | PT27A | 1 | T | - | PT31A | 1 | T | - |
| A13 | PT26B | 1 | C | - | PT30B | 1 | C | - |
| C13 | PT26A | 1 | T | D0 | PT30A | 1 | T | D0 |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| C10 | PT25B | 1 | C | D1 | PT29B | 1 | C | D1 |
| E10 | PT25A | 1 | T | VREF2_1 | PT29A | 1 | T | VREF2_1 |
| A12 | PT24B | 1 | C | - | PT28B | 1 | C | - |
| B12 | PT24A | 1 | T | D2 | PT28A | 1 | T | D2 |
| C12 | PT23B | 1 | C | D3 | PT27B | 1 | C | D3 |
| A11 | PT23A | 1 | T | - | PT27A | 1 | T | - |
| B11 | PT22B | 1 | C | - | PT26B | 1 | C | - |
| D11 | PT22A | 1 | T | DQS | PT26A | 1 | T | DQS |
| - | GNDIO1 | 1 | - | - | GNDIO1 | 1 | - | - |
| B9 | PT21B | 1 | - | - | PT25B | 1 | - | - |
| D9 | PT20A | 1 | - | D4 | PT24A | 1 | - | D4 |
| A10 | PT19B | 1 | C | - | PT23B | 1 | C | - |
| B10 | PT19A | 1 | T | D5 | PT23A | 1 | T | D5 |
| D10 | PT18B | 1 | C | D6 | PT22B | 1 | C | D6 |
| A9 | PT18A | 1 | T | - | PT22A | 1 | T | - |
| C9 | PT17B | 1 | C | D7 | PT21B | 1 | C | D7 |
| C8 | PT17A | 1 | T | - | PT21A | 1 | T | - |
| E9 | PT16B | 0 | C | BUSY | PT20B | 0 | C | BUSY |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| B8 | PT16A | 0 | T | CS1N | PT20A | 0 | T | CS1N |
| A8 | PT15B | 0 | C | PCLKC0_0 | PT19B | 0 | C | PCLKC0_0 |
| A7 | PT15A | 0 | T | PCLKT0_0 | PT19A | 0 | T | PCLKT0_0 |
| B7 | PT14B | 0 | C | - | PT18B | 0 | C | - |
| C7 | PT14A | 0 | T | DQS | PT18A | 0 | T | DQS |

## LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| P16 | PR37B | 3 | C[3] | - | PR41B | 3 | C[3] | - |
| R16 | PR37A | 3 | T[3] | DQS | PR41A | 3 | T[3] | DQS |
| M15 | PR36B | 3 | - | - | PR40B | 3 | - | - |
| N14 | PR35A | 3 | - | VREF1_3 | PR39A | 3 | - | VREF1_3 |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| M14 | PR33B | 3 | C | - | PR37B | 3 | C | - |
| L13 | PR33A | 3 | T | - | PR37A | 3 | T | - |
| L15 | PR32B | 3 | C[3] | - | PR36B | 3 | C[3] | - |
| L14 | PR32A | 3 | T[3] | - | PR36A | 3 | T[3] | - |
| L12 | PR30A | 3 | - | - | PR34A | 3 | - | - |
| M16 | PR29B | 3 | C | RLM0_PLLC_IN_A | PR33B | 3 | C | RLM0_PLLC_IN_A |
| N16 | PR29A | 3 | T | RLM0_PLLT_IN_A | PR33A | 3 | T | RLM0_PLLT_IN_A |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| K14 | PR28B | 3 | C[3] | - | PR32B | 3 | C[3] | - |
| K15 | PR28A | 3 | T[3] | DQS | PR32A | 3 | T[3] | DQS |
| K12 | PR27B | 3 | - | - | PR31B | 3 | - | - |
| K13 | PR26A | 3 | - | VREF2_3 | PR30A | 3 | - | VREF2_3 |
| L16 | PR25B | 3 | C[3] | - | PR29B | 3 | C[3] | - |
| K16 | PR25A | 3 | T[3] | - | PR29A | 3 | T[3] | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| J15 | PR23B | 3 | C[3] | - | PR27B | 3 | C[3] | - |
| J14 | PR23A | 3 | T[3] | - | PR27A | 3 | T[3] | - |
| J13 | GNDP1 | - | - | - | GNDP1 | - | - | - |
| J12 | VCCP1 | - | - | - | VCCP1 | - | - | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| J16 | PR21B | 2 | C | PCLKC2_0 | PR21B | 2 | C | PCLKC2_0 |
| H16 | PR21A | 2 | T | PCLKT2_0 | PR21A | 2 | T | PCLKT2_0 |
| H13 | PR20B | 2 | C[3] | - | PR20B | 2 | C[3] | - |
| H12 | PR20A | 2 | T[3] | DQS | PR20A | 2 | T[3] | DQS |
| H15 | PR19B | 2 | - | - | PR19B | 2 | - | - |
| H14 | PR18A | 2 | - | VREF1_2 | PR18A | 2 | - | VREF1_2 |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| G15 | PR17B | 2 | C[3] | - | PR17B | 2 | C[3] | - |
| G14 | PR17A | 2 | T[3] | - | PR17A | 2 | T[3] | - |
| G16 | PR16B | 2 | C | RUM0_PLLC_IN_A | PR16B | 2 | C | RUM0_PLLC_IN_A |
| F16 | PR16A | 2 | T | RUM0_PLLT_IN_A | PR16A | 2 | T | RUM0_PLLT_IN_A |
| G13 | PR15B | 2 | - | - | PR15B | 2 | - | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| G12 | PR12B | 2 | C | - | PR12B | 2 | C | - |
| F13 | PR12A | 2 | T | - | PR12A | 2 | T | - |
| B16 | PR11B | 2 | C[3] | - | PR11B | 2 | C[3] | - |
| C16 | PR11A | 2 | T[3] | DQS | PR11A | 2 | T[3] | DQS |

## LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| A9 | PT27A | 1 | T | - | PT31A | 1 | T | - |
| C9 | PT26B | 1 | C | D7 | PT30B | 1 | C | D7 |
| C8 | PT26A | 1 | T | - | PT30A | 1 | T | - |
| E9 | PT25B | 0 | C | BUSY | PT29B | 0 | C | BUSY |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| B8 | PT25A | 0 | T | CS1N | PT29A | 0 | T | CS1N |
| A8 | PT24B | 0 | C | PCLKC0_0 | PT28B | 0 | C | PCLKC0_0 |
| A7 | PT24A | 0 | T | PCLKT0_0 | PT28A | 0 | T | PCLKT0_0 |
| B7 | PT23B | 0 | C | - | PT27B | 0 | C | - |
| C7 | PT23A | 0 | T | DQS | PT27A | 0 | T | DQS |
| E8 | PT22B | 0 | - | - | PT26B | 0 | - | - |
| D8 | PT21A | 0 | - | DOUT | PT25A | 0 | - | DOUT |
| A6 | PT20B | 0 | C | - | PT24B | 0 | C | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C6 | PT20A | 0 | T | WRITEN | PT24A | 0 | T | WRITEN |
| E7 | PT19B | 0 | C | - | PT23B | 0 | C | - |
| D7 | PT19A | 0 | T | VREF1_0 | PT23A | 0 | T | VREF1_0 |
| A5 | PT18B | 0 | C | - | PT22B | 0 | C | - |
| B5 | PT18A | 0 | T | DI | PT22A | 0 | T | DI |
| A4 | PT17B | 0 | C | - | PT21B | 0 | C | - |
| B6 | PT17A | 0 | T | CSN | PT21A | 0 | T | CSN |
| E6 | PT16B | 0 | C | - | PT20B | 0 | C | - |
| D6 | PT16A | 0 | T | - | PT20A | 0 | T | - |
| D5 | PT15B | 0 | C | VREF2_0 | PT19B | 0 | C | VREF2_0 |
| A3 | PT15A | 0 | T | DQS | PT19A | 0 | T | DQS |
| B3 | PT14B | 0 | - | - | PT18B | 0 | - | - |
| B2 | PT13A | 0 | - | - | PT17A | 0 | - | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| A2 | PT12B | 0 | C | - | PT16B | 0 | C | - |
| B1 | PT12A | 0 | T | - | PT16A | 0 | T | - |
| F5 | PT11B | 0 | C | - | PT15B | 0 | C | - |
| C5 | PT11A | 0 | T | - | PT15A | 0 | T | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C4 | CFG0 | 0 | - | - | CFG0 | 0 | - | - |
| B4 | CFG1 | 0 | - | - | CFG1 | 0 | - | - |
| C3 | DONE | 0 | - | - | DONE | 0 | - | - |
| A1 | GND | - | - | - | GND | - | - | - |
| A16 | GND | - | - | - | GND | - | - | - |
| F11 | GND | - | - | - | GND | - | - | - |
| F6 | GND | - | - | - | GND | - | - | - |

# LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

| Ball Number | LFXP10 | | | | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function | Ball Function | Bank | Diff. | Dual Function |
| AA20 | PB36B | 4 | C | - | PB41B | 4 | C | - | PB45B | 4 | C | - |
| AB21 | PB37A | 4 | T | - | PB42A | 4 | T | - | PB46A | 4 | T | - |
| AA21 | PB37B | 4 | C | - | PB42B | 4 | C | - | PB46B | 4 | C | - |
| AA22 | PB38A | 4 | T | - | PB43A | 4 | T | - | PB47A | 4 | T | - |
| Y21 | PB38B | 4 | C | - | PB43B | 4 | C | - | PB47B | 4 | C | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| W16 | PB39A | 4 | - | - | PB44A | 4 | T | - | PB48A | 4 | T | - |
| W17 | - | - | - | - | PB44B | 4 | C | - | PB48B | 4 | C | - |
| Y15 | - | - | - | - | PB45A | 4 | - | - | PB49A | 4 | - | - |
| Y16 | - | - | - | - | PB46B | 4 | - | - | PB50B | 4 | - | - |
| W19 | - | - | - | - | PB47A | 4 | T | DQS | PB51A | 4 | T | DQS |
| W18 | - | - | - | - | PB47B | 4 | C | - | PB51B | 4 | C | - |
| W20 | - | - | - | - | PB48A | 4 | - | - | PB52A | 4 | - | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - | GNDIO4 | 4 | - | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| T20 | PR35B | 3 | C[3] | - | PR39B | 3 | C[3] | - | PR43B | 3 | C[3] | - |
| T19 | PR35A | 3 | T[3] | - | PR39A | 3 | T[3] | - | PR43A | 3 | T[3] | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| U19 | PR34B | 3 | C | RLM0_PLLC_FB_A | PR38B | 3 | C | RLM0_PLLC_FB_A | PR42B | 3 | C | RLM0_PLLC_FB_A |
| U20 | PR34A | 3 | T | RLM0_PLLT_FB_A | PR38A | 3 | T | RLM0_PLLT_FB_A | PR42A | 3 | T | RLM0_PLLT_FB_A |
| V19 | PR33B | 3 | C[3] | - | PR37B | 3 | C[3] | - | PR41B | 3 | C[3] | - |
| V20 | PR33A | 3 | T[3] | DQS | PR37A | 3 | T[3] | DQS | PR41A | 3 | T[3] | DQS |
| R19 | PR32B | 3 | - | - | PR36B | 3 | - | - | PR40B | 3 | - | - |
| R20 | PR31A | 3 | - | VREF1_3 | PR35A | 3 | - | VREF1_3 | PR39A | 3 | - | VREF1_3 |
| W21 | PR30B | 3 | C[3] | - | PR34B | 3 | C[3] | - | PR38B | 3 | C[3] | - |
| Y22 | PR30A | 3 | T[3] | - | PR34A | 3 | T[3] | - | PR38A | 3 | T[3] | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| P19 | PR29B | 3 | C | - | PR33B | 3 | C | - | PR37B | 3 | C | - |
| P20 | PR29A | 3 | T | - | PR33A | 3 | T | - | PR37A | 3 | T | - |
| V21 | PR28B | 3 | C[3] | - | PR32B | 3 | C[3] | - | PR36B | 3 | C[3] | - |
| W22 | PR28A | 3 | T[3] | - | PR32A | 3 | T[3] | - | PR36A | 3 | T[3] | - |
| U21 | PR26B | 3 | C[3] | - | PR30B | 3 | C[3] | - | PR34B | 3 | C[3] | - |
| V22 | PR26A | 3 | T[3] | - | PR30A | 3 | T[3] | - | PR34A | 3 | T[3] | - |
| T21 | PR25B | 3 | C | RLM0_PLLC_IN_A | PR29B | 3 | C | RLM0_PLLC_IN_A | PR33B | 3 | C | RLM0_PLLC_IN_A |
| U22 | PR25A | 3 | T | RLM0_PLLT_IN_A | PR29A | 3 | T | RLM0_PLLT_IN_A | PR33A | 3 | T | RLM0_PLLT_IN_A |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| R21 | PR24B | 3 | C[3] | - | PR28B | 3 | C[3] | - | PR32B | 3 | C[3] | - |
| T22 | PR24A | 3 | T[3] | DQS | PR28A | 3 | T[3] | DQS | PR32A | 3 | T[3] | DQS |
| N19 | PR23B | 3 | - | - | PR27B | 3 | - | - | PR31B | 3 | - | - |
| N20 | PR22A | 3 | - | VREF2_3 | PR26A | 3 | - | VREF2_3 | PR30A | 3 | - | VREF2_3 |
| R22 | PR21B | 3 | C[3] | - | PR25B | 3 | C[3] | - | PR29B | 3 | C[3] | - |
| P22 | PR21A | 3 | T[3] | - | PR25A | 3 | T[3] | - | PR29A | 3 | T[3] | - |
| P21 | PR20B | 3 | C | - | PR24B | 3 | C | - | PR28B | 3 | C | - |
| N21 | PR20A | 3 | T | - | PR24A | 3 | T | - | PR28A | 3 | T | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| M20 | PR19B | 3 | C[3] | - | PR23B | 3 | C[3] | - | PR27B | 3 | C[3] | - |
| M19 | PR19A | 3 | T[3] | - | PR23A | 3 | T[3] | - | PR27A | 3 | T[3] | - |
| N22 | GNDP1 | - | - | - | GNDP1 | - | - | - | GNDP1 | - | - | - |

# LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| T6 | PL41A | 6 | T | - | PL45A | 6 | T | - |
| T5 | PL41B | 6 | C | - | PL45B | 6 | C | - |
| - | GNDIO6 | 6 | - | - | GNDIO6 | 6 | - | - |
| U3 | PL42A | 6 | T[3] | - | PL46A | 6 | T[3] | - |
| U4 | PL42B | 6 | C[3] | - | PL46B | 6 | C[3] | - |
| V4 | PL43A | 6 | - | - | PL47A | 6 | - | - |
| W4 | SLEEPN[1]/ TOE[2] | - | - | - | SLEEPN[1]/ TOE[2] | - | - | - |
| W5 | INITN | 5 | - | - | INITN | 5 | - | - |
| Y3 | - | - | - | - | PB3B | 5 | - | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| U5 | - | - | - | - | PB4A | 5 | T | - |
| V5 | - | - | - | - | PB4B | 5 | C | - |
| Y4 | - | - | - | - | PB5A | 5 | T | - |
| Y5 | - | - | - | - | PB5B | 5 | C | - |
| V6 | - | - | - | - | PB6A | 5 | T | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| U6 | - | - | - | - | PB6B | 5 | C | - |
| W6 | PB3A | 5 | T | - | PB7A | 5 | T | - |
| Y6 | PB3B | 5 | C | - | PB7B | 5 | C | - |
| AA2 | PB4A | 5 | T | - | PB8A | 5 | T | - |
| AA3 | PB4B | 5 | C | - | PB8B | 5 | C | - |
| V7 | PB5A | 5 | - | - | PB9A | 5 | - | - |
| U7 | PB6B | 5 | - | - | PB10B | 5 | - | - |
| Y7 | PB7A | 5 | T | DQS | PB11A | 5 | T | DQS |
| W7 | PB7B | 5 | C | - | PB11B | 5 | C | - |
| AA4 | PB8A | 5 | T | - | PB12A | 5 | T | - |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| AA5 | PB8B | 5 | C | - | PB12B | 5 | C | - |
| AB3 | PB9A | 5 | T | - | PB13A | 5 | T | - |
| AB4 | PB9B | 5 | C | - | PB13B | 5 | C | - |
| AA6 | PB10A | 5 | T | - | PB14A | 5 | T | - |
| AA7 | PB10B | 5 | C | - | PB14B | 5 | C | - |
| U8 | PB11A | 5 | T | - | PB15A | 5 | T | - |
| V8 | PB11B | 5 | C | - | PB15B | 5 | C | - |
| Y8 | PB12A | 5 | T | VREF1_5 | PB16A | 5 | T | VREF1_5 |
| - | GNDIO5 | 5 | - | - | GNDIO5 | 5 | - | - |
| W8 | PB12B | 5 | C | - | PB16B | 5 | C | - |
| V9 | PB13A | 5 | - | - | PB17A | 5 | - | - |
| U9 | PB14B | 5 | - | - | PB18B | 5 | - | - |
| Y9 | PB15A | 5 | T | DQS | PB19A | 5 | T | DQS |
| W9 | PB15B | 5 | C | - | PB19B | 5 | C | - |

# LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| R18 | PR38B | 3 | C | RLM0_PLLC_FB_A | PR42B | 3 | C | RLM0_PLLC_FB_A |
| R17 | PR38A | 3 | T | RLM0_PLLT_FB_A | PR42A | 3 | T | RLM0_PLLT_FB_A |
| Y22 | PR37B | 3 | C[3] | - | PR41B | 3 | C[3] | - |
| Y21 | PR37A | 3 | T[3] | DQS | PR41A | 3 | T[3] | DQS |
| W22 | PR36B | 3 | - | - | PR40B | 3 | - | - |
| W21 | PR35A | 3 | - | VREF1_3 | PR39A | 3 | - | VREF1_3 |
| P17 | PR34B | 3 | C[3] | - | PR38B | 3 | C[3] | - |
| P18 | PR34A | 3 | T[3] | - | PR38A | 3 | T[3] | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| R19 | PR33B | 3 | C | - | PR37B | 3 | C | - |
| R20 | PR33A | 3 | T | - | PR37A | 3 | T | - |
| V22 | PR32B | 3 | C[3] | - | PR36B | 3 | C[3] | - |
| V21 | PR32A | 3 | T[3] | - | PR36A | 3 | T[3] | - |
| U22 | PR30B | 3 | C[3] | - | PR34B | 3 | C[3] | - |
| U21 | PR30A | 3 | T[3] | - | PR34A | 3 | T[3] | - |
| P19 | PR29B | 3 | C | RLM0_PLLC_IN_A | PR33B | 3 | C | RLM0_PLLC_IN_A |
| P20 | PR29A | 3 | T | RLM0_PLLT_IN_A | PR33A | 3 | T | RLM0_PLLT_IN_A |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| T22 | PR28B | 3 | C[3] | - | PR32B | 3 | C[3] | - |
| T21 | PR28A | 3 | T[3] | DQS | PR32A | 3 | T[3] | DQS |
| R22 | PR27B | 3 | - | - | PR31B | 3 | - | - |
| R21 | PR26A | 3 | - | VREF2_3 | PR30A | 3 | - | VREF2_3 |
| N19 | PR25B | 3 | C[3] | - | PR29B | 3 | C[3] | - |
| N20 | PR25A | 3 | T[3] | - | PR29A | 3 | T[3] | - |
| N18 | PR24B | 3 | C | - | PR28B | 3 | C | - |
| M18 | PR24A | 3 | T | - | PR28A | 3 | T | - |
| - | GNDIO3 | 3 | - | - | GNDIO3 | 3 | - | - |
| P22 | PR23B | 3 | C[3] | - | PR27B | 3 | C[3] | - |
| P21 | PR23A | 3 | T[3] | - | PR27A | 3 | T[3] | - |
| N22 | - | - | - | - | PR26B | 3 | C[3] | - |
| N21 | - | - | - | - | PR26A | 3 | T[3] | - |
| M19 | - | - | - | - | PR25B | 3 | - | - |
| M20 | GNDP1 | - | - | - | GNDP1 | - | - | - |
| L18 | VCCP1 | - | - | - | VCCP1 | - | - | - |
| M21 | - | - | - | - | PR24A | 2 | - | - |
| M22 | PR22B | 2 | C[3] | - | PR23B | 2 | C[3] | - |
| L22 | PR22A | 2 | T[3] | - | PR23A | 2 | T[3] | - |
| - | GNDIO2 | 2 | - | - | GNDIO2 | 2 | - | - |
| L19 | - | - | - | - | PR22B | 2 | C[3] | - |
| L20 | - | - | - | - | PR22A | 2 | T[3] | - |
| L21 | PR21B | 2 | C | PCLKC2_0 | PR21B | 2 | C | PCLKC2_0 |
| K22 | PR21A | 2 | T | PCLKT2_0 | PR21A | 2 | T | PCLKT2_0 |

## LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

| Ball Number | LFXP15 | | | | LFXP20 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Differential | Dual Function | Ball Function | Bank | Differential | Dual Function |
| B3 | PT8B | 0 | C | - | PT12B | 0 | C | - |
| A3 | PT8A | 0 | T | - | PT12A | 0 | T | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| D7 | PT7B | 0 | C | - | PT11B | 0 | C | - |
| C7 | PT7A | 0 | T | DQS | PT11A | 0 | T | DQS |
| B2 | PT6B | 0 | - | - | PT10B | 0 | - | - |
| C2 | PT5A | 0 | - | - | PT9A | 0 | - | - |
| C3 | PT4B | 0 | C | - | PT8B | 0 | C | - |
| D3 | PT4A | 0 | T | - | PT8A | 0 | T | - |
| F7 | PT3B | 0 | C | - | PT7B | 0 | C | - |
| E7 | PT3A | 0 | T | - | PT7A | 0 | T | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| C6 | - | - | - | - | PT6B | 0 | C | - |
| D6 | - | - | - | - | PT6A | 0 | T | - |
| C5 | - | - | - | - | PT5B | 0 | C | - |
| C4 | - | - | - | - | PT5A | 0 | T | - |
| F6 | - | - | - | - | PT4B | 0 | C | - |
| E6 | - | - | - | - | PT4A | 0 | T | - |
| - | GNDIO0 | 0 | - | - | GNDIO0 | 0 | - | - |
| E4 | - | - | - | - | PT3B | 0 | - | - |
| E5 | CFG0 | 0 | - | - | CFG0 | 0 | - | - |
| D4 | CFG1 | 0 | - | - | CFG1 | 0 | - | - |
| D5 | DONE | 0 | - | - | DONE | 0 | - | - |
| A1 | GND | - | - | - | GND | - | - | - |
| A2 | GND | - | - | - | GND | - | - | - |
| A21 | GND | - | - | - | GND | - | - | - |
| A22 | GND | - | - | - | GND | - | - | - |
| AA1 | GND | - | - | - | GND | - | - | - |
| AA22 | GND | - | - | - | GND | - | - | - |
| AB1 | GND | - | - | - | GND | - | - | - |
| AB2 | GND | - | - | - | GND | - | - | - |
| AB21 | GND | - | - | - | GND | - | - | - |
| AB22 | GND | - | - | - | GND | - | - | - |
| B1 | GND | - | - | - | GND | - | - | - |
| B22 | GND | - | - | - | GND | - | - | - |
| H14 | GND | - | - | - | GND | - | - | - |
| H9 | GND | - | - | - | GND | - | - | - |
| J10 | GND | - | - | - | GND | - | - | - |
| J11 | GND | - | - | - | GND | - | - | - |
| J12 | GND | - | - | - | GND | - | - | - |
| J13 | GND | - | - | - | GND | - | - | - |
| J14 | GND | - | - | - | GND | - | - | - |

**Commercial (Cont.)**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP20E-3F484C | 340 | 1.2V | -3 | fpBGA | 484 | COM | 19.7K |
| LFXP20E-4F484C | 340 | 1.2V | -4 | fpBGA | 484 | COM | 19.7K |
| LFXP20E-5F484C | 340 | 1.2V | -5 | fpBGA | 484 | COM | 19.7K |
| LFXP20E-3F388C | 268 | 1.2V | -3 | fpBGA | 388 | COM | 19.7K |
| LFXP20E-4F388C | 268 | 1.2V | -4 | fpBGA | 388 | COM | 19.7K |
| LFXP20E-5F388C | 268 | 1.2V | -5 | fpBGA | 388 | COM | 19.7K |
| LFXP20E-3F256C | 188 | 1.2V | -3 | fpBGA | 256 | COM | 19.7K |
| LFXP20E-4F256C | 188 | 1.2V | -4 | fpBGA | 256 | COM | 19.7K |
| LFXP20E-5F256C | 188 | 1.2V | -5 | fpBGA | 256 | COM | 19.7K |

**Industrial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP3C-3Q208I | 136 | 1.8/2.5/3.3V | -3 | PQFP | 208 | IND | 3.1K |
| LFXP3C-4Q208I | 136 | 1.8/2.5/3.3V | -4 | PQFP | 208 | IND | 3.1K |
| LFXP3C-3T144I | 100 | 1.8/2.5/3.3V | -3 | TQFP | 144 | IND | 3.1K |
| LFXP3C-4T144I | 100 | 1.8/2.5/3.3V | -4 | TQFP | 144 | IND | 3.1K |
| LFXP3C-3T100I | 62 | 1.8/2.5/3.3V | -3 | TQFP | 100 | IND | 3.1K |
| LFXP3C-4T100I | 62 | 1.8/2.5/3.3V | -4 | TQFP | 100 | IND | 3.1K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP6C-3F256I | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | IND | 5.8K |
| LFXP6C-4F256I | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | IND | 5.8K |
| LFXP6C-3Q208I | 142 | 1.8/2.5/3.3V | -3 | PQFP | 208 | IND | 5.8K |
| LFXP6C-4Q208I | 142 | 1.8/2.5/3.3V | -4 | PQFP | 208 | IND | 5.8K |
| LFXP6C-3T144I | 100 | 1.8/2.5/3.3V | -3 | TQFP | 144 | IND | 5.8K |
| LFXP6C-4T144I | 100 | 1.8/2.5/3.3V | -4 | TQFP | 144 | IND | 5.8K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP10C-3F388I | 244 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | IND | 9.7K |
| LFXP10C-4F388I | 244 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | IND | 9.7K |
| LFXP10C-3F256I | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | IND | 9.7K |
| LFXP10C-4F256I | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | IND | 9.7K |

## Lead-free Packaging

**Commercial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP3C-3QN208C | 136 | 1.8/2.5/3.3V | -3 | PQFP | 208 | COM | 3.1K |
| LFXP3C-4QN208C | 136 | 1.8/2.5/3.3V | -4 | PQFP | 208 | COM | 3.1K |
| LFXP3C-5QN208C | 136 | 1.8/2.5/3.3V | -5 | PQFP | 208 | COM | 3.1K |
| LFXP3C-3TN144C | 100 | 1.8/2.5/3.3V | -3 | TQFP | 144 | COM | 3.1K |
| LFXP3C-4TN144C | 100 | 1.8/2.5/3.3V | -4 | TQFP | 144 | COM | 3.1K |
| LFXP3C-5TN144C | 100 | 1.8/2.5/3.3V | -5 | TQFP | 144 | COM | 3.1K |
| LFXP3C-3TN100C | 62 | 1.8/2.5/3.3V | -3 | TQFP | 100 | COM | 3.1K |
| LFXP3C-4TN100C | 62 | 1.8/2.5/3.3V | -4 | TQFP | 100 | COM | 3.1K |
| LFXP3C-5TN100C | 62 | 1.8/2.5/3.3V | -5 | TQFP | 100 | COM | 3.1K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP6C-3FN256C | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | COM | 5.8K |
| LFXP6C-4FN256C | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | COM | 5.8K |
| LFXP6C-5FN256C | 188 | 1.8/2.5/3.3V | -5 | fpBGA | 256 | COM | 5.8K |
| LFXP6C-3QN208C | 142 | 1.8/2.5/3.3V | -3 | PQFP | 208 | COM | 5.8K |
| LFXP6C-4QN208C | 142 | 1.8/2.5/3.3V | -4 | PQFP | 208 | COM | 5.8K |
| LFXP6C-5QN208C | 142 | 1.8/2.5/3.3V | -5 | PQFP | 208 | COM | 5.8K |
| LFXP6C-3TN144C | 100 | 1.8/2.5/3.3V | -3 | TQFP | 144 | COM | 5.8K |
| LFXP6C-4TN144C | 100 | 1.8/2.5/3.3V | -4 | TQFP | 144 | COM | 5.8K |
| LFXP6C-5TN144C | 100 | 1.8/2.5/3.3V | -5 | TQFP | 144 | COM | 5.8K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP10C-3FN388C | 244 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | COM | 9.7K |
| LFXP10C-4FN388C | 244 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | COM | 9.7K |
| LFXP10C-5FN388C | 244 | 1.8/2.5/3.3V | -5 | fpBGA | 388 | COM | 9.7K |
| LFXP10C-3FN256C | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | COM | 9.7K |
| LFXP10C-4FN256C | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | COM | 9.7K |
| LFXP10C-5FN256C | 188 | 1.8/2.5/3.3V | -5 | fpBGA | 256 | COM | 9.7K |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs |
|---|---|---|---|---|---|---|---|
| LFXP15C-3FN484C | 300 | 1.8/2.5/3.3V | -3 | fpBGA | 484 | COM | 15.5K |
| LFXP15C-4FN484C | 300 | 1.8/2.5/3.3V | -4 | fpBGA | 484 | COM | 15.5K |
| LFXP15C-5FN484C | 300 | 1.8/2.5/3.3V | -5 | fpBGA | 484 | COM | 15.5K |
| LFXP15C-3FN388C | 268 | 1.8/2.5/3.3V | -3 | fpBGA | 388 | COM | 15.5K |
| LFXP15C-4FN388C | 268 | 1.8/2.5/3.3V | -4 | fpBGA | 388 | COM | 15.5K |
| LFXP15C-5FN388C | 268 | 1.8/2.5/3.3V | -5 | fpBGA | 388 | COM | 15.5K |
| LFXP15C-3FN256C | 188 | 1.8/2.5/3.3V | -3 | fpBGA | 256 | COM | 15.5K |
| LFXP15C-4FN256C | 188 | 1.8/2.5/3.3V | -4 | fpBGA | 256 | COM | 15.5K |
| LFXP15C-5FN256C | 188 | 1.8/2.5/3.3V | -5 | fpBGA | 256 | COM | 15.5K |