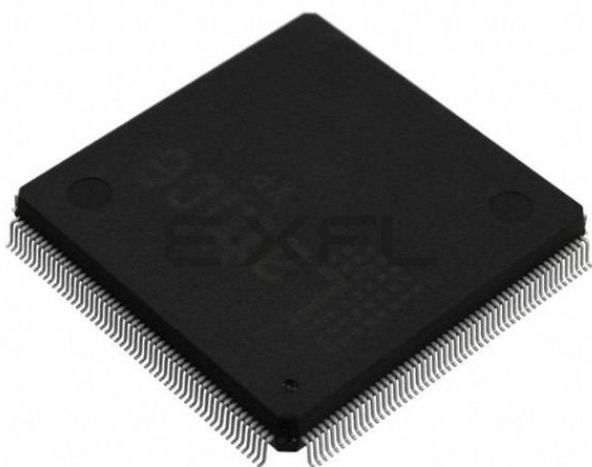




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6000
Total RAM Bits	73728
Number of I/O	142
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp6c-5q208c

Figure 2-21. Input Register DDR Waveforms

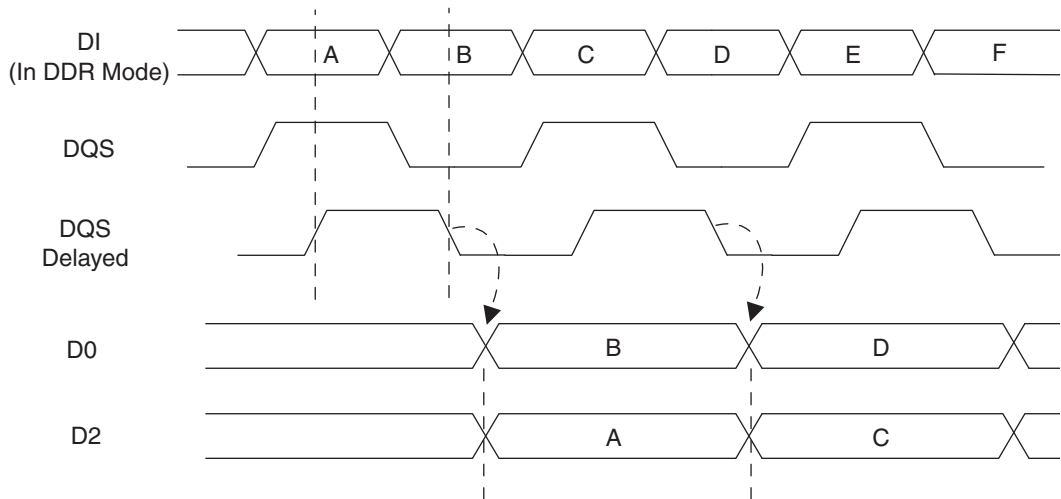
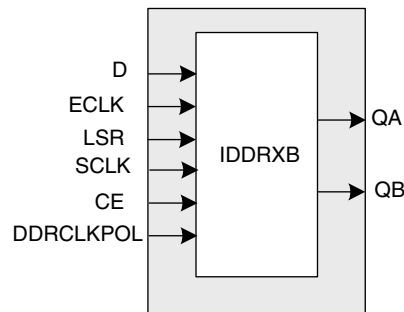


Figure 2-22. INDDRXB Primitive



Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-23 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or as a latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-24 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

Figure 2-26. DQS Local Bus

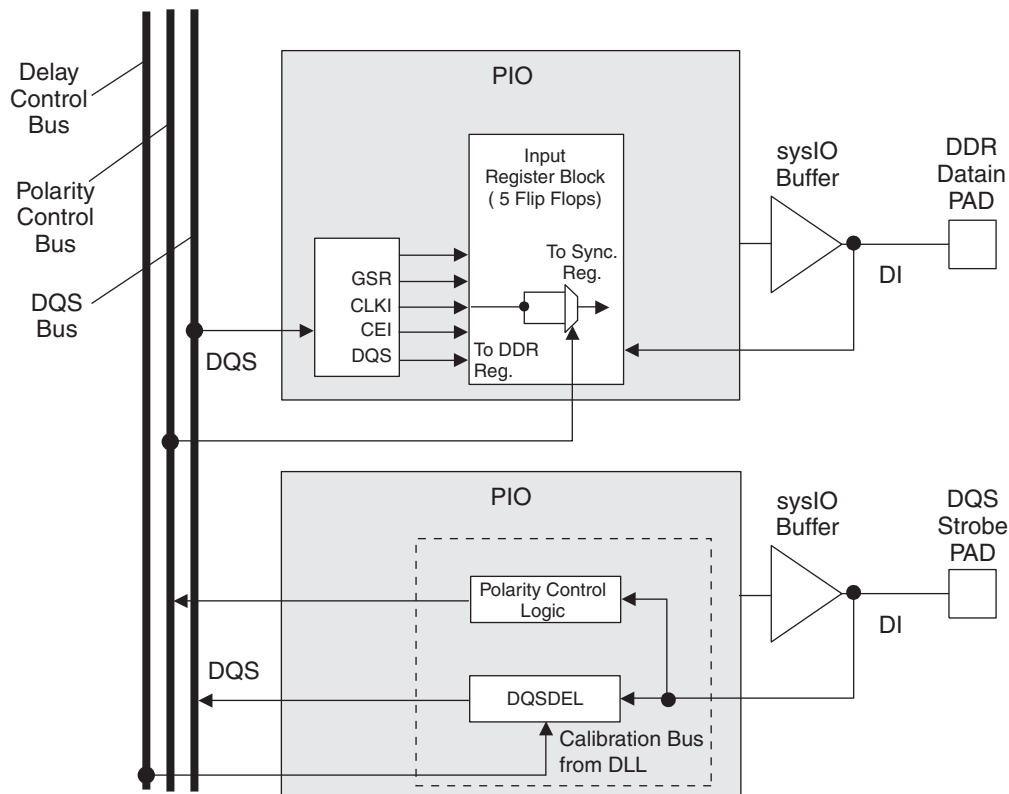
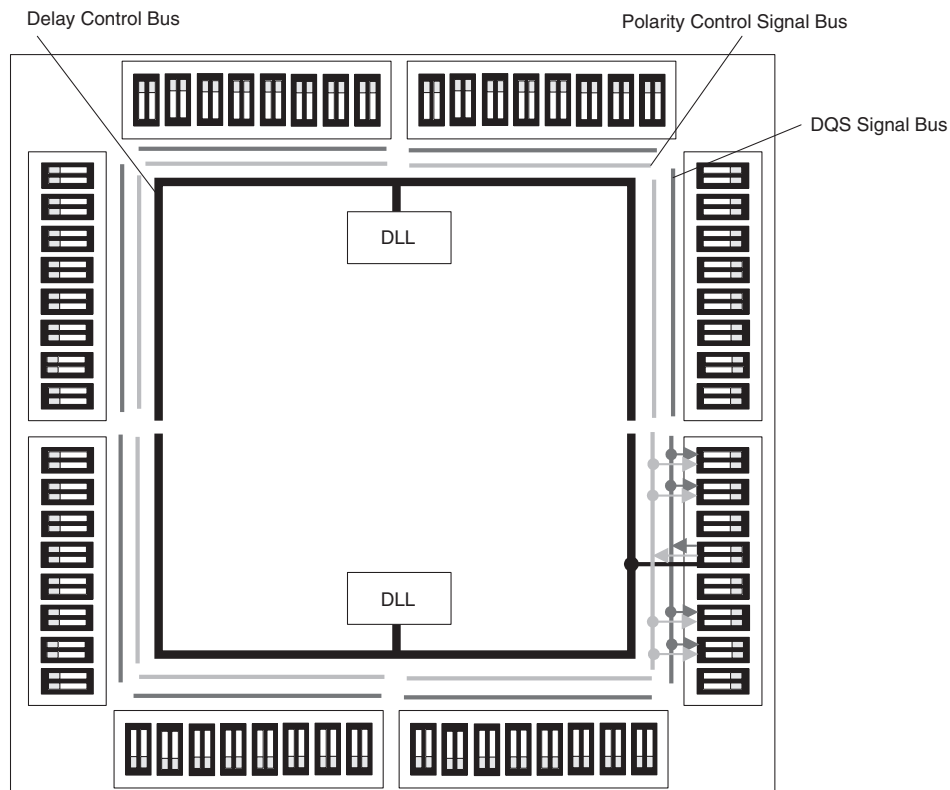


Figure 2-27. DLL Calibration Bus and DQS/DQS Transition Distribution



Initialization Supply Current^{1, 2, 3, 4, 5, 6}**Over Recommended Operating Conditions**

Symbol	Parameter	Device	Typ. ⁷	Units
I_{CC}	Core Power Supply	LFXP3E	40	mA
		LFXP6E	50	mA
		LFXP10E	110	mA
		LFXP15E	140	mA
		LFXP20E	250	mA
		LFXP3C	60	mA
		LFXP6C	70	mA
		LFXP10C	150	mA
		LFXP15C	180	mA
		LFXP20C	290	mA
I_{CCAUX}	Auxiliary Power Supply $V_{CCAUX} = 3.3V$	LFXP3E/C	50	mA
		LFXP6E/C	60	mA
		LFXP10E/C	90	mA
		LFXP15 /C	110	mA
		LFXP20E/C	130	mA
I_{CCJ}	V_{CCJ} Power Supply	All	2	mA

1. Until DONE signal is active.

2. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.

3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

4. Frequency 0MHz.

5. Typical user pattern.

6. Assume normal bypass capacitor/decoupling capacitor across the supply.

7. $T_A=25^{\circ}C$, power supplies at nominal voltage.

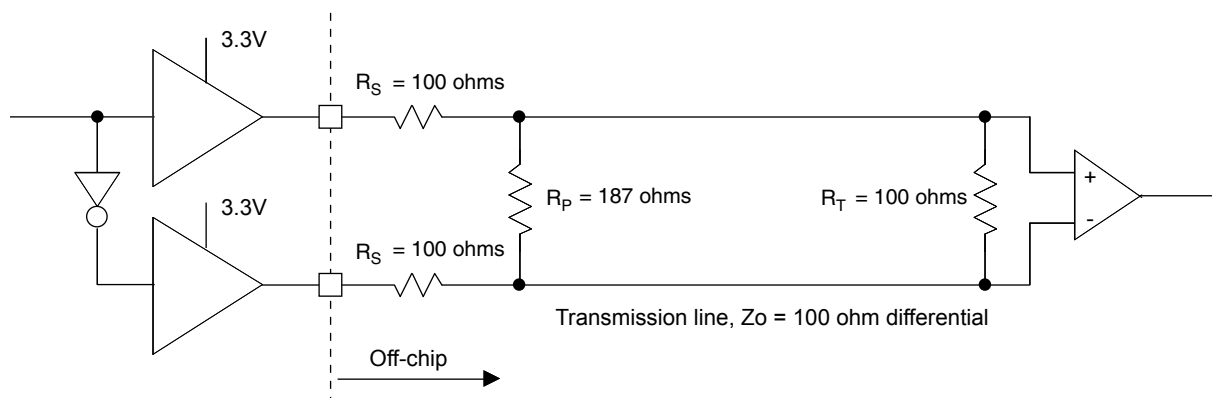
sysIO Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVTTTL	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	16, 12, 8, 4	-16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 1.5	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	8, 4	-8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 1.2 ("C" Version)	-0.3	0.42	0.78	3.6	0.4	$V_{CCIO} - 0.4$	6, 2	-6, -2
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 1.2 ("E" Version)	-0.3	$0.35V_{CC}$	$0.65V_{CC}$	3.6	0.4	$V_{CCIO} - 0.4$	6, 2	-6, -2
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
PCI	-0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	-0.5
SSTL3 class I	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.7	$V_{CCIO} - 1.1$	8	-8
SSTL3 class II	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.5	$V_{CCIO} - 0.9$	16	-16
SSTL2 class I	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.54	$V_{CCIO} - 0.62$	7.6	-7.6
SSTL2 class II	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.35	$V_{CCIO} - 0.43$	15.2	-15.2
SSTL18 class I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	3.6	0.4	$V_{CCIO} - 0.4$	6.7	-6.7
HSTL15 class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL15 class III	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	24	-8
HSTL18 class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	9.6	-9.6
HSTL18 class II	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL18 class III	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	24	-8

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed $n * 8\text{mA}$. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

LVPECL

The LatticeXP devices support differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL**Table 3-3. LVPECL DC Conditions¹****Over Recommended Operating Conditions**

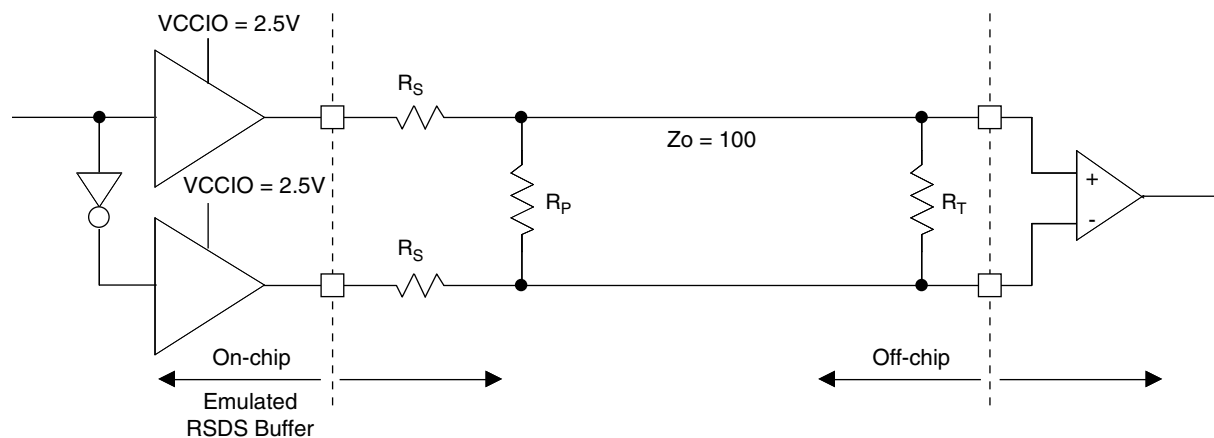
Symbol	Description	Typical	Units
Z_{OUT}	Output impedance	100	ohms
R_P	Driver parallel resistor	187	ohms
R_S	Driver series resistor	100	ohms
R_T	Receiver termination	100	ohms
V_{OH}	Output high voltage	2.03	V
V_{OL}	Output low voltage	1.27	V
V_{OD}	Output differential voltage	0.76	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	85.7	ohms
I_{DC}	DC output current	12.7	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

RSDS

The LatticeXP devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)**Table 3-4. RSDS DC Conditions**

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	ohms
R_S	Driver series resistor	300	ohms
R_P	Driver parallel resistor	121	ohms
R_T	Receiver termination	100	ohms
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	ohms
I_{DC}	DC output current	3.66	mA

Derating Logic Timing

Logic timing provided in the following sections of this data sheet and in the ispLEVER design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best-case process can be much better than the values given in the tables. The ispLEVER design tool from Lattice can provide logic timing numbers at a particular temperature and voltage.

LatticeXP External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Device	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (Using Primary Clock without PLL) ¹									
t _{CO}	Clock to Output - PIO Output Register	LFXP3	—	5.12	—	6.12	—	7.43	ns
		LFXP6	—	5.30	—	6.34	—	7.69	ns
		LFXP10	—	5.52	—	6.60	—	8.00	ns
		LFXP15	—	5.72	—	6.84	—	8.29	ns
		LFXP20	—	5.97	—	7.14	—	8.65	ns
t _{SU}	Clock to Data Setup - PIO Input Register	LFXP3	-0.40	—	-0.28	—	-0.16	—	ns
		LFXP6	-0.33	—	-0.32	—	-0.30	—	ns
		LFXP10	-0.61	—	-0.71	—	-0.81	—	ns
		LFXP15	-0.71	—	-0.77	—	-0.87	—	ns
		LFXP20	-0.95	—	-1.14	—	-1.35	—	ns
t _H	Clock to Data Hold - PIO Input Register	LFXP3	2.10	—	2.50	—	2.98	—	ns
		LFXP6	2.28	—	2.72	—	3.24	—	ns
		LFXP10	3.02	—	3.51	—	3.71	—	ns
		LFXP15	2.70	—	3.22	—	3.85	—	ns
		LFXP20	2.95	—	3.52	—	4.21	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Input Data Delay	LFXP3	2.38	—	2.49	—	2.66	—	ns
		LFXP6	2.92	—	3.18	—	3.42	—	ns
		LFXP10	2.72	—	2.75	—	2.84	—	ns
		LFXP15	2.99	—	3.13	—	3.18	—	ns
		LFXP20	4.47	—	4.56	—	4.80	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFXP3	-0.70	—	-0.80	—	-0.92	—	ns
		LFXP6	-0.47	—	-0.38	—	-0.31	—	ns
		LFXP10	-0.60	—	-0.47	—	-0.32	—	ns
		LFXP15	-1.05	—	-0.98	—	-1.01	—	ns
		LFXP20	-0.80	—	-0.58	—	-0.31	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	All	—	400	—	360	—	320	MHz
DDR I/O Pin Parameters ²									
t _{DVADQ}	Data Valid After DQS (DDR Read)	All	—	0.19	—	0.19	—	0.19	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	All	0.67	—	0.67	—	0.67	—	UI
t _{DQVBS}	Data Valid Before DQS	All	0.20	—	0.20	—	0.20	—	UI
t _{DQVAS}	Data Valid After DQS	All	0.20	—	0.20	—	0.20	—	UI
f _{MAX_DDR}	DDR Clock Frequency	All	95	166	95	133	95	100	MHz
Primary and Secondary Clocks									
f _{MAX_PRI}	Frequency for Primary Clock Tree	All	—	450	—	412	—	375	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	All	1.19	—	1.19	—	1.19	—	ns
t _{SKEW_PRI}	Primary Clock Skew within an I/O Bank	LFXP3/6/10/15	—	250	—	300	—	350	ps
		LFXP20	—	300	—	350	—	400	ps

1. General timing numbers based on LVCMOS 2.5, 12mA.

2. DDR timing numbers based on SSTL I/O.

Timing v.F0.11

LatticeXP Internal Timing Parameters¹

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t _{LUT4_PFU}	LUT4 Delay (A to D Inputs to F Output)	—	0.28	—	0.34	—	0.40	ns
t _{LUT6_PFU}	LUT6 Delay (A to D Inputs to OFX Output)	—	0.44	—	0.53	—	0.63	ns
t _{LSR_PFU}	Set/Reset to Output of PFU	—	0.90	—	1.08	—	1.29	ns
t _{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.13	—	0.15	—	0.19	—	ns
t _{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.04	—	-0.03	—	-0.03	—	ns
t _{SUD_PFU}	Clock to D Input Setup Time	0.13	—	0.16	—	0.19	—	ns
t _{HD_PFU}	Clock to D Input Hold Time	-0.03	—	-0.02	—	-0.02	—	ns
t _{CK2Q_PFU}	Clock to Q Delay, D-type Register Configuration	—	0.40	—	0.48	—	0.58	ns
t _{LE2Q_PFU}	Clock to Q Delay Latch Configuration	—	0.53	—	0.64	—	0.76	ns
t _{LD2Q_PFU}	D to Q Throughput Delay when Latch is Enabled	—	0.55	—	0.66	—	0.79	ns
PFU Dual Port Memory Mode Timing								
t _{CORAM_PFU}	Clock to Output	—	0.40	—	0.48	—	0.58	ns
t _{SUDATA_PFU}	Data Setup Time	-0.18	—	-0.14	—	-0.11	—	ns
t _{HDATA_PFU}	Data Hold Time	0.28	—	0.34	—	0.40	—	ns
t _{SUADDR_PFU}	Address Setup Time	-0.46	—	-0.37	—	-0.30	—	ns
t _{HADDR_PFU}	Address Hold Time	0.71	—	0.85	—	1.02	—	ns
t _{SUWREN_PFU}	Write/Read Enable Setup Time	-0.22	—	-0.17	—	-0.14	—	ns
t _{HWREN_PFU}	Write/Read Enable Hold Time	0.33	—	0.40	—	0.48	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t _{IN_PIO}	Input Buffer Delay	—	0.62	—	0.72	—	0.85	ns
t _{OUT_PIO}	Output Buffer Delay	—	2.12	—	2.54	—	3.05	ns
IOLOGIC Input/Output Timing								
t _{SUI_PIO}	Input Register Setup Time (Data Before Clock)	1.35	—	1.83	—	2.37	—	ns
t _{HI_PIO}	Input Register Hold Time (Data After Clock)	0.05	—	0.05	—	0.05	—	ns
t _{COO_PIO}	Output Register Clock to Output Delay	—	0.36	—	0.44	—	0.52	ns
t _{SUCE_PIO}	Input Register Clock Enable Setup Time	-0.09	—	-0.07	—	-0.06	—	ns
t _{HCE_PIO}	Input Register Clock Enable Hold Time	0.13	—	0.16	—	0.19	—	ns
t _{SULSR_PIO}	Set/Reset Setup Time	0.19	—	0.23	—	0.28	—	ns
t _{HLSR_PIO}	Set/Reset Hold Time	-0.14	—	-0.11	—	-0.09	—	ns
EBR Timing								
t _{CO_EBR}	Clock to Output from Address or Data	—	4.01	—	4.81	—	5.78	ns
t _{COO_EBR}	Clock to Output from EBR Output Register	—	0.81	—	0.97	—	1.17	ns
t _{SUDATA_EBR}	Setup Data to EBR Memory	-0.26	—	-0.21	—	-0.17	—	ns
t _{HDATA_EBR}	Hold Data to EBR Memory	0.41	—	0.49	—	0.59	—	ns
t _{SUADDR_EBR}	Setup Address to EBR Memory	-0.26	—	-0.21	—	-0.17	—	ns
t _{HADDR_EBR}	Hold Address to EBR Memory	0.41	—	0.49	—	0.59	—	ns
t _{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory	-0.17	—	-0.13	—	-0.11	—	ns
t _{HWREN_EBR}	Hold Write/Read Enable to EBR Memory	0.26	—	0.31	—	0.37	—	ns
t _{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.19	—	0.23	—	0.28	—	ns
t _{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.13	—	-0.10	—	-0.08	—	ns

LatticeXP Family Timing Adders¹ (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	-5	-4	-3	Units
HSTL15_I	HSTL_15 class I	0.2	0.2	0.2	ns
HSTL15_III	HSTL_15 class III	0.2	0.2	0.2	ns
HSTL15D_I	Differential HSTL 15 class I	0.2	0.2	0.2	ns
HSTL15D_III	Differential HSTL 15 class III	0.2	0.2	0.2	ns
SSTL33_I	SSTL_3 class I	0.1	0.1	0.1	ns
SSTL33_II	SSTL_3 class II	0.3	0.3	0.3	ns
SSTL33D_I	Differential SSTL_3 class I	0.1	0.1	0.1	ns
SSTL33D_II	Differential SSTL_3 class II	0.3	0.3	0.3	ns
SSTL25_I	SSTL_2 class I	-0.1	-0.1	-0.1	ns
SSTL25_II	SSTL_2 class II	0.3	0.3	0.3	ns
SSTL25D_I	Differential SSTL_2 class I	-0.1	-0.1	-0.1	ns
SSTL25D_II	Differential SSTL_2 class II	0.3	0.3	0.3	ns
SSTL18_I	SSTL_1.8 class I	0.1	0.1	0.1	ns
SSTL18D_I	Differential SSTL_1.8 class I	0.1	0.1	0.1	ns
LVTTTL33_4mA	LVTTTL 4mA drive	0.8	0.8	0.8	ns
LVTTTL33_8mA	LVTTTL 8mA drive	0.5	0.5	0.5	ns
LVTTTL33_12mA	LVTTTL 12mA drive	0.3	0.3	0.3	ns
LVTTTL33_16mA	LVTTTL 16mA drive	0.4	0.4	0.4	ns
LVTTTL33_20mA	LVTTTL 20mA drive	0.3	0.3	0.3	ns
LVC MOS33_2mA	LVC MOS 3.3 2mA drive	0.8	0.8	0.8	ns
LVC MOS33_4mA	LVC MOS 3.3 4mA drive	0.8	0.8	0.8	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive	0.5	0.5	0.5	ns
LVC MOS33_12mA	LVC MOS 3.3 12mA drive	0.3	0.3	0.3	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive	0.4	0.4	0.4	ns
LVC MOS33_20mA	LVC MOS 3.3 20mA drive	0.3	0.3	0.3	ns
LVC MOS25_2mA	LVC MOS 2.5 2mA drive	0.7	0.7	0.7	ns
LVC MOS25_4mA	LVC MOS 2.5 4mA drive	0.7	0.7	0.7	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive	0.4	0.4	0.4	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive	0.0	0.0	0.0	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive	0.2	0.2	0.2	ns
LVC MOS25_20mA	LVC MOS 2.5 20mA drive	0.4	0.4	0.4	ns
LVC MOS18_2mA	LVC MOS 1.8 2mA drive	0.6	0.6	0.6	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive	0.6	0.6	0.6	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive	0.4	0.4	0.4	ns
LVC MOS18_12mA	LVC MOS 1.8 12mA drive	0.2	0.2	0.2	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive	0.2	0.2	0.2	ns
LVC MOS15_2mA	LVC MOS 1.5 2mA drive	0.6	0.6	0.6	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive	0.6	0.6	0.6	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive	0.2	0.2	0.2	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive	0.4	0.4	0.4	ns
LVC MOS12_6mA	LVC MOS 1.2 6mA drive	0.4	0.4	0.4	ns
PCI33	PCI33	0.3	0.3	0.3	ns

1. General timing numbers based on LVC MOS 2.5, 12mA.
Timing v.F0.11

Pin Information Summary¹ (Cont.)

Pin Type		XP10		XP15			XP20		
		256 fpBGA	388 fpBGA	256 fpBGA	388 fpBGA	484 fpBGA	256 fpBGA	388 fpBGA	484 fpBGA
Single Ended User I/O		188	244	188	268	300	188	268	340
Differential Pair User I/O ²		76	104	76	112	128	76	112	144
Configuration	Dedicated	11	11	11	11	11	11	11	11
	Muxed	14	14	14	14	14	14	14	14
TAP		5	5	5	5	5	5	5	5
Dedicated (total without supplies)		6	6	6	6	6	6	6	6
V _{CC}		8	14	8	14	28	8	14	28
V _{CCAUX}		4	4	4	4	12	4	4	12
V _{CCPLL}		2	2	2	2	2	2	2	2
V _{CCIO}	Bank0	2	5	2	5	4	2	5	4
	Bank1	2	5	2	5	4	2	5	4
	Bank2	2	4	2	4	4	2	4	4
	Bank3	2	4	2	4	4	2	4	4
	Bank4	2	5	2	5	4	2	5	4
	Bank5	2	5	2	5	4	2	5	4
	Bank6	2	4	2	4	4	2	4	4
	Bank7	2	4	2	4	4	2	4	4
GND		24	50	24	50	56	24	50	56
GND _{PLL}		2	2	2	2	2	2	2	2
NC		0	24	0	0	40	0	0	0
Single Ended/ Differential I/O per Bank ²	Bank0	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank1	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank2	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank3	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank4	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank5	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank6	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank7	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
V _{CCJ}		1	1	1	1	1	1	1	1

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
2. The differential I/O per bank includes both dedicated LVDS and emulated LVDS pin pairs. Please see the Logic Signal Connections table for more information.

LFXP3 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	Pin Function	Bank	Differential	Dual Function
44	GNDIO4	4	-	-
45	PB15A	4	T	PCLKT4_0
46	PB15B	4	C	PCLKC4_0
47	VCCIO4	4	-	-
48	PB19A	4	T	DQS
49	PB19B	4	C	VREF1_4
50	PB24A	4	-	VREF2_4
51	PR18B	3	C ³	-
52	GNDIO3	3	-	-
53	PR18A	3	T ³	-
54	PR15B	3	-	VREF1_3
55	PR14A	3	-	VREF2_3
56	PR13B	3	C	-
57	PR13A	3	T	-
58	VCCIO3	3	-	-
59	GNDP1	-	-	-
60	VCCP1	-	-	-
61	PR9B	2	C	PCLKC2_0
62	PR9A	2	T	PCLKT2_0
63	PR8B	2	C	RUM0_PLLC_IN_A
64	PR8A	2	T	RUM0_PLLT_IN_A
65	VCCIO2	2	-	-
66	PR6B	2	-	VREF1_2
67	PR5A	2	-	VREF2_2
68	GNDIO2	2	-	-
69	PR3B	2	C	RUM0_PLLC_FB_A
70	PR3A	2	T	RUM0_PLLT_FB_A
71	VCCAUX	-	-	-
72	TDO	-	-	-
73	VCCJ	-	-	-
74	TDI	-	-	-
75	TMS	-	-	-
76	TCK	-	-	-
77	VCC	-	-	-
78	PT24A	1	-	-
79	PT23A	1	-	D0
80	PT22B	1	-	D1
81	PT21A	1	-	D2
82	VCCIO1	1	-	-
83	PT20B	1	-	D3
84	GNDIO1	1	-	-
85	PT17A	1	-	D4
86	PT16A	1	-	D5
87	PT15B	1	-	D6

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
P16	PR37B	3	C ³	-	PR41B	3	C ³	-
R16	PR37A	3	T ³	DQS	PR41A	3	T ³	DQS
M15	PR36B	3	-	-	PR40B	3	-	-
N14	PR35A	3	-	VREF1_3	PR39A	3	-	VREF1_3
-	GNDIO3	3	-	-	GNDIO3	3	-	-
M14	PR33B	3	C	-	PR37B	3	C	-
L13	PR33A	3	T	-	PR37A	3	T	-
L15	PR32B	3	C ³	-	PR36B	3	C ³	-
L14	PR32A	3	T ³	-	PR36A	3	T ³	-
L12	PR30A	3	-	-	PR34A	3	-	-
M16	PR29B	3	C	RLM0_PLLC_IN_A	PR33B	3	C	RLM0_PLLC_IN_A
N16	PR29A	3	T	RLM0_PLLT_IN_A	PR33A	3	T	RLM0_PLLT_IN_A
-	GNDIO3	3	-	-	GNDIO3	3	-	-
K14	PR28B	3	C ³	-	PR32B	3	C ³	-
K15	PR28A	3	T ³	DQS	PR32A	3	T ³	DQS
K12	PR27B	3	-	-	PR31B	3	-	-
K13	PR26A	3	-	VREF2_3	PR30A	3	-	VREF2_3
L16	PR25B	3	C ³	-	PR29B	3	C ³	-
K16	PR25A	3	T ³	-	PR29A	3	T ³	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
J15	PR23B	3	C ³	-	PR27B	3	C ³	-
J14	PR23A	3	T ³	-	PR27A	3	T ³	-
J13	GNDP1	-	-	-	GNDP1	-	-	-
J12	VCCP1	-	-	-	VCCP1	-	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
J16	PR21B	2	C	PCLKC2_0	PR21B	2	C	PCLKC2_0
H16	PR21A	2	T	PCLKT2_0	PR21A	2	T	PCLKT2_0
H13	PR20B	2	C ³	-	PR20B	2	C ³	-
H12	PR20A	2	T ³	DQS	PR20A	2	T ³	DQS
H15	PR19B	2	-	-	PR19B	2	-	-
H14	PR18A	2	-	VREF1_2	PR18A	2	-	VREF1_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G15	PR17B	2	C ³	-	PR17B	2	C ³	-
G14	PR17A	2	T ³	-	PR17A	2	T ³	-
G16	PR16B	2	C	RUM0_PLLC_IN_A	PR16B	2	C	RUM0_PLLC_IN_A
F16	PR16A	2	T	RUM0_PLLT_IN_A	PR16A	2	T	RUM0_PLLT_IN_A
G13	PR15B	2	-	-	PR15B	2	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G12	PR12B	2	C	-	PR12B	2	C	-
F13	PR12A	2	T	-	PR12A	2	T	-
B16	PR11B	2	C ³	-	PR11B	2	C ³	-
C16	PR11A	2	T ³	DQS	PR11A	2	T ³	DQS

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
AB5	PB16A	5	T	-	PB20A	5	T	-
AB6	PB16B	5	C	-	PB20B	5	C	-
AA8	PB17A	5	T	-	PB21A	5	T	-
AA9	PB17B	5	C	VREF2_5	PB21B	5	C	VREF2_5
W10	PB18A	5	T	-	PB22A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
V10	PB18B	5	C	-	PB22B	5	C	-
AB7	PB19A	5	T	-	PB23A	5	T	-
AB8	PB19B	5	C	-	PB23B	5	C	-
AB9	PB20A	5	T	-	PB24A	5	T	-
AB10	PB20B	5	C	-	PB24B	5	C	-
Y10	PB21A	5	-	-	PB25A	5	-	-
AA10	PB22B	5	-	-	PB26B	5	-	-
W11	PB23A	5	T	DQS	PB27A	5	T	DQS
V11	PB23B	5	C	-	PB27B	5	C	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y11	PB24A	5	T	-	PB28A	5	T	-
AA11	PB24B	5	C	-	PB28B	5	C	-
AB11	PB25A	5	T	-	PB29A	5	T	-
AB12	PB25B	5	C	-	PB29B	5	C	-
Y12	PB26A	4	T	-	PB30A	4	T	-
AA12	PB26B	4	C	-	PB30B	4	C	-
W12	PB27A	4	T	PCLKT4_0	PB31A	4	T	PCLKT4_0
V12	PB27B	4	C	PCLKC4_0	PB31B	4	C	PCLKC4_0
-	GNDIO4	4	-	-	GNDIO4	4	-	-
AB13	PB28A	4	T	-	PB32A	4	T	-
AB14	PB28B	4	C	-	PB32B	4	C	-
AA13	PB29A	4	-	-	PB33A	4	-	-
Y13	PB30B	4	-	-	PB34B	4	-	-
AB15	PB31A	4	T	DQS	PB35A	4	T	DQS
AB16	PB31B	4	C	VREF1_4	PB35B	4	C	VREF1_4
V13	PB32A	4	T	-	PB36A	4	T	-
W13	PB32B	4	C	-	PB36B	4	C	-
AA14	PB33A	4	T	-	PB37A	4	T	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA15	PB33B	4	C	-	PB37B	4	C	-
AB17	PB34A	4	T	-	PB38A	4	T	-
AB18	PB34B	4	C	-	PB38B	4	C	-
W14	PB35A	4	T	-	PB39A	4	T	-
Y14	PB35B	4	C	-	PB39B	4	C	-
U14	PB36A	4	T	VREF2_4	PB40A	4	T	VREF2_4
V14	PB36B	4	C	-	PB40B	4	C	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
J21	PR20B	2	C ³	-	PR20B	2	C ³	-
J22	PR20A	2	T ³	DQS	PR20A	2	T ³	DQS
K18	PR19B	2	-	-	PR19B	2	-	-
K19	PR18A	2	-	VREF1_2	PR18A	2	-	VREF1_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
K21	PR17B	2	C ³	-	PR17B	2	C ³	-
K20	PR17A	2	T ³	-	PR17A	2	T ³	-
H21	PR16B	2	C	RUM0_PLLC_IN_A	PR16B	2	C	RUM0_PLLC_IN_A
H22	PR16A	2	T	RUM0_PLLT_IN_A	PR16A	2	T	RUM0_PLLT_IN_A
J20	PR15B	2	C ³	-	PR15B	2	C ³	-
J19	PR15A	2	T ³	-	PR15A	2	T ³	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
J17	PR13B	2	C ³	-	PR13B	2	C ³	-
J18	PR13A	2	T ³	-	PR13A	2	T ³	-
G21	PR12B	2	C	-	PR12B	2	C	-
G22	PR12A	2	T	-	PR12A	2	T	-
F21	PR11B	2	C ³	-	PR11B	2	C ³	-
F22	PR11A	2	T ³	DQS	PR11A	2	T ³	DQS
-	GNDIO2	2	-	-	GNDIO2	2	-	-
H20	PR10B	2	-	-	PR10B	2	-	-
H19	PR9A	2	-	VREF2_2	PR9A	2	-	VREF2_2
H17	PR8B	2	C ³	-	PR8B	2	C ³	-
H18	PR8A	2	T ³	-	PR8A	2	T ³	-
E21	PR7B	2	C	RUM0_PLLC_FB_A	PR7B	2	C	RUM0_PLLC_FB_A
E22	PR7A	2	T	RUM0_PLLT_FB_A	PR7A	2	T	RUM0_PLLT_FB_A
D21	PR6B	2	C ³	-	PR6B	2	C ³	-
D22	PR6A	2	T ³	-	PR6A	2	T ³	-
G20	PR5B	2	C ³	-	PR5B	2	C ³	-
G19	PR5A	2	T ³	-	PR5A	2	T ³	-
G17	PR4B	2	C	-	PR4B	2	C	-
G18	PR4A	2	T	-	PR4A	2	T	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
F18	PR3B	2	C ³	-	PR3B	2	C ³	-
F19	PR3A	2	T ³	-	PR3A	2	T ³	-
C22	PR2B	2	-	-	PR2B	2	-	-
F20	TDO	-	-	-	TDO	-	-	-
E20	VCCJ	-	-	-	VCCJ	-	-	-
D19	TDI	-	-	-	TDI	-	-	-
E19	TMS	-	-	-	TMS	-	-	-
D20	TCK	-	-	-	TCK	-	-	-
C20	-	-	-	-	PT56A	1	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
D18	-	-	-	-	PT55B	1	C	-
E18	-	-	-	-	PT55A	1	T	-
C19	-	-	-	-	PT54B	1	C	-
C18	-	-	-	-	PT54A	1	T	-
C21	-	-	-	-	PT53B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B21	-	-	-	-	PT53A	1	T	-
E17	PT48B	1	C	-	PT52B	1	C	-
E16	PT48A	1	T	-	PT52A	1	T	-
C17	PT47B	1	C	-	PT51B	1	C	-
D17	PT47A	1	T	DQS	PT51A	1	T	DQS
F17	PT46B	1	-	-	PT50B	1	-	-
F16	PT45A	1	-	-	PT49A	1	-	-
C16	PT44B	1	C	-	PT48B	1	C	-
D16	PT44A	1	T	-	PT48A	1	T	-
A20	PT43B	1	C	-	PT47B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B20	PT43A	1	T	-	PT47A	1	T	-
A19	PT42B	1	C	-	PT46B	1	C	-
B19	PT42A	1	T	-	PT46A	1	T	-
C15	PT41B	1	C	-	PT45B	1	C	-
D15	PT41A	1	T	-	PT45A	1	T	-
A18	PT40B	1	C	-	PT44B	1	C	-
B18	PT40A	1	T	-	PT44A	1	T	-
F15	PT39B	1	C	VREF1_1	PT43B	1	C	VREF1_1
-	GNDIO1	1	-	-	GNDIO1	1	-	-
E15	PT39A	1	T	DQS	PT43A	1	T	DQS
A17	PT38B	1	-	-	PT42B	1	-	-
B17	PT37A	1	-	-	PT41A	1	-	-
E14	PT36B	1	C	-	PT40B	1	C	-
F14	PT36A	1	T	-	PT40A	1	T	-
D14	PT35B	1	C	-	PT39B	1	C	-
C14	PT35A	1	T	D0	PT39A	1	T	D0
A16	PT34B	1	C	D1	PT38B	1	C	D1
B16	PT34A	1	T	VREF2_1	PT38A	1	T	VREF2_1
A15	PT33B	1	C	-	PT37B	1	C	-
B15	PT33A	1	T	D2	PT37A	1	T	D2
-	GNDIO1	1	-	-	GNDIO1	1	-	-
E13	PT32B	1	C	D3	PT36B	1	C	D3
D13	PT32A	1	T	-	PT36A	1	T	-
C13	PT31B	1	C	-	PT35B	1	C	-
B13	PT31A	1	T	DQS	PT35A	1	T	DQS

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
J15	GND	-	-	-	GND	-	-	-
J8	GND	-	-	-	GND	-	-	-
J9	GND	-	-	-	GND	-	-	-
K10	GND	-	-	-	GND	-	-	-
K11	GND	-	-	-	GND	-	-	-
K12	GND	-	-	-	GND	-	-	-
K13	GND	-	-	-	GND	-	-	-
K14	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-
L10	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-
L12	GND	-	-	-	GND	-	-	-
L13	GND	-	-	-	GND	-	-	-
L14	GND	-	-	-	GND	-	-	-
L9	GND	-	-	-	GND	-	-	-
M10	GND	-	-	-	GND	-	-	-
M11	GND	-	-	-	GND	-	-	-
M12	GND	-	-	-	GND	-	-	-
M13	GND	-	-	-	GND	-	-	-
M14	GND	-	-	-	GND	-	-	-
M9	GND	-	-	-	GND	-	-	-
N10	GND	-	-	-	GND	-	-	-
N11	GND	-	-	-	GND	-	-	-
N12	GND	-	-	-	GND	-	-	-
N13	GND	-	-	-	GND	-	-	-
N14	GND	-	-	-	GND	-	-	-
N9	GND	-	-	-	GND	-	-	-
P10	GND	-	-	-	GND	-	-	-
P11	GND	-	-	-	GND	-	-	-
P12	GND	-	-	-	GND	-	-	-
P13	GND	-	-	-	GND	-	-	-
P14	GND	-	-	-	GND	-	-	-
P15	GND	-	-	-	GND	-	-	-
P8	GND	-	-	-	GND	-	-	-
P9	GND	-	-	-	GND	-	-	-
R14	GND	-	-	-	GND	-	-	-
R9	GND	-	-	-	GND	-	-	-
F10	VCC	-	-	-	VCC	-	-	-
F13	VCC	-	-	-	VCC	-	-	-
G10	VCC	-	-	-	VCC	-	-	-
G13	VCC	-	-	-	VCC	-	-	-
G14	VCC	-	-	-	VCC	-	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
G9	VCC	-	-	-	VCC	-	-	-
H15	VCC	-	-	-	VCC	-	-	-
H8	VCC	-	-	-	VCC	-	-	-
J16	VCC	-	-	-	VCC	-	-	-
J7	VCC	-	-	-	VCC	-	-	-
K16	VCC	-	-	-	VCC	-	-	-
K17	VCC	-	-	-	VCC	-	-	-
K6	VCC	-	-	-	VCC	-	-	-
K7	VCC	-	-	-	VCC	-	-	-
N16	VCC	-	-	-	VCC	-	-	-
N17	VCC	-	-	-	VCC	-	-	-
N6	VCC	-	-	-	VCC	-	-	-
N7	VCC	-	-	-	VCC	-	-	-
P16	VCC	-	-	-	VCC	-	-	-
P7	VCC	-	-	-	VCC	-	-	-
R15	VCC	-	-	-	VCC	-	-	-
R8	VCC	-	-	-	VCC	-	-	-
T10	VCC	-	-	-	VCC	-	-	-
T13	VCC	-	-	-	VCC	-	-	-
T14	VCC	-	-	-	VCC	-	-	-
T9	VCC	-	-	-	VCC	-	-	-
U10	VCC	-	-	-	VCC	-	-	-
U13	VCC	-	-	-	VCC	-	-	-
G15	VCCAUX	-	-	-	VCCAUX	-	-	-
G16	VCCAUX	-	-	-	VCCAUX	-	-	-
G7	VCCAUX	-	-	-	VCCAUX	-	-	-
G8	VCCAUX	-	-	-	VCCAUX	-	-	-
H16	VCCAUX	-	-	-	VCCAUX	-	-	-
H7	VCCAUX	-	-	-	VCCAUX	-	-	-
R16	VCCAUX	-	-	-	VCCAUX	-	-	-
R7	VCCAUX	-	-	-	VCCAUX	-	-	-
T15	VCCAUX	-	-	-	VCCAUX	-	-	-
T16	VCCAUX	-	-	-	VCCAUX	-	-	-
T7	VCCAUX	-	-	-	VCCAUX	-	-	-
T8	VCCAUX	-	-	-	VCCAUX	-	-	-
F11	VCCIO0	0	-	-	VCCIO0	0	-	-
G11	VCCIO0	0	-	-	VCCIO0	0	-	-
H10	VCCIO0	0	-	-	VCCIO0	0	-	-
H11	VCCIO0	0	-	-	VCCIO0	0	-	-
F12	VCCIO1	1	-	-	VCCIO1	1	-	-
G12	VCCIO1	1	-	-	VCCIO1	1	-	-
H12	VCCIO1	1	-	-	VCCIO1	1	-	-

Industrial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15C-3F484I	300	1.8/2.5/3.3V	-3	fpBGA	484	IND	15.5K
LFXP15C-4F484I	300	1.8/2.5/3.3V	-4	fpBGA	484	IND	15.5K
LFXP15C-3F388I	268	1.8/2.5/3.3V	-3	fpBGA	388	IND	15.5K
LFXP15C-4F388I	268	1.8/2.5/3.3V	-4	fpBGA	388	IND	15.5K
LFXP15C-3F256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	15.5K
LFXP15C-4F256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	15.5K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20C-3F484I	340	1.8/2.5/3.3V	-3	fpBGA	484	IND	19.7K
LFXP20C-4F484I	340	1.8/2.5/3.3V	-4	fpBGA	484	IND	19.7K
LFXP20C-3F388I	268	1.8/2.5/3.3V	-3	fpBGA	388	IND	19.7K
LFXP20C-4F388I	268	1.8/2.5/3.3V	-4	fpBGA	388	IND	19.7K
LFXP20C-3F256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	19.7K
LFXP20C-4F256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	19.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3E-3Q208I	136	1.2V	-3	PQFP	208	IND	3.1K
LFXP3E-4Q208I	136	1.2V	-4	PQFP	208	IND	3.1K
LFXP3E-3T144I	100	1.2V	-3	TQFP	144	IND	3.1K
LFXP3E-4T144I	100	1.2V	-4	TQFP	144	IND	3.1K
LFXP3E-3T100I	62	1.2V	-3	TQFP	100	IND	3.1K
LFXP3E-4T100I	62	1.2V	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6E-3F256I	188	1.2V	-3	fpBGA	256	IND	5.8K
LFXP6E-4F256I	188	1.2V	-4	fpBGA	256	IND	5.8K
LFXP6E-3Q208I	142	1.2V	-3	PQFP	208	IND	5.8K
LFXP6E-4Q208I	142	1.2V	-4	PQFP	208	IND	5.8K
LFXP6E-3T144I	100	1.2V	-3	TQFP	144	IND	5.8K
LFXP6E-4T144I	100	1.2V	-4	TQFP	144	IND	5.8K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10E-3F388I	244	1.2V	-3	fpBGA	388	IND	9.7K
LFXP10E-4F388I	244	1.2V	-4	fpBGA	388	IND	9.7K
LFXP10E-3F256I	188	1.2V	-3	fpBGA	256	IND	9.7K
LFXP10E-4F256I	188	1.2V	-4	fpBGA	256	IND	9.7K

Industrial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10C-3FN388I	244	1.8/2.5/3.3V	-3	fpBGA	388	IND	9.7K
LFXP10C-4FN388I	244	1.8/2.5/3.3V	-4	fpBGA	388	IND	9.7K
LFXP10C-3FN256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	9.7K
LFXP10C-4FN256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	9.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15C-3FN484I	300	1.8/2.5/3.3V	-3	fpBGA	484	IND	15.5K
LFXP15C-4FN484I	300	1.8/2.5/3.3V	-4	fpBGA	484	IND	15.5K
LFXP15C-3FN388I	268	1.8/2.5/3.3V	-3	fpBGA	388	IND	15.5K
LFXP15C-4FN388I	268	1.8/2.5/3.3V	-4	fpBGA	388	IND	15.5K
LFXP15C-3FN256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	15.5K
LFXP15C-4FN256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	15.5K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20C-3FN484I	340	1.8/2.5/3.3V	-3	fpBGA	484	IND	19.7K
LFXP20C-4FN484I	340	1.8/2.5/3.3V	-4	fpBGA	484	IND	19.7K
LFXP20C-3FN388I	268	1.8/2.5/3.3V	-3	fpBGA	388	IND	19.7K
LFXP20C-4FN388I	268	1.8/2.5/3.3V	-4	fpBGA	388	IND	19.7K
LFXP20C-3FN256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	19.7K
LFXP20C-4FN256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	19.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3E-3QN208I	136	1.2V	-3	PQFP	208	IND	3.1K
LFXP3E-4QN208I	136	1.2V	-4	PQFP	208	IND	3.1K
LFXP3E-3TN144I	100	1.2V	-3	TQFP	144	IND	3.1K
LFXP3E-4TN144I	100	1.2V	-4	TQFP	144	IND	3.1K
LFXP3E-3TN100I	62	1.2V	-3	TQFP	100	IND	3.1K
LFXP3E-4TN100I	62	1.2V	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6E-3FN256I	188	1.2V	-3	fpBGA	256	IND	5.8K
LFXP6E-4FN256I	188	1.2V	-4	fpBGA	256	IND	5.8K
LFXP6E-3QN208I	142	1.2V	-3	PQFP	208	IND	5.8K
LFXP6E-4QN208I	142	1.2V	-4	PQFP	208	IND	5.8K
LFXP6E-3TN144I	100	1.2V	-3	TQFP	144	IND	5.8K
LFXP6E-4TN144I	100	1.2V	-4	TQFP	144	IND	5.8K