Understanding Embedded - FPGAs (Field Programmable Gate Array)

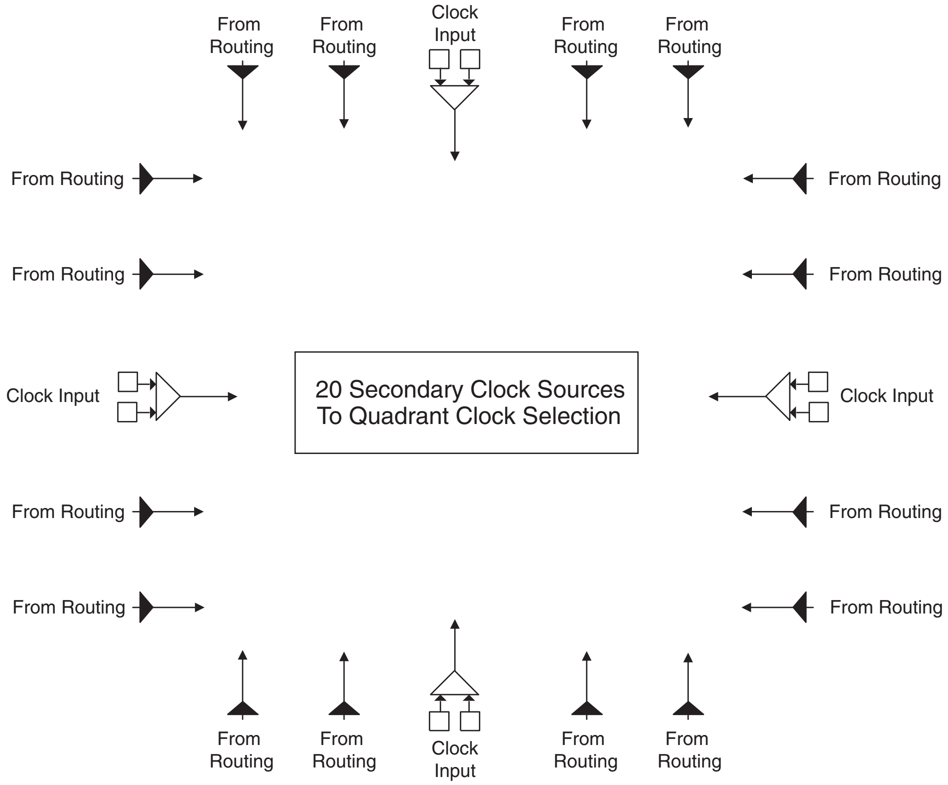
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6000
Total RAM Bits	73728
Number of I/O	100
Number of Gates	-
Voltage - Supply	1.71V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp6c-5t144c

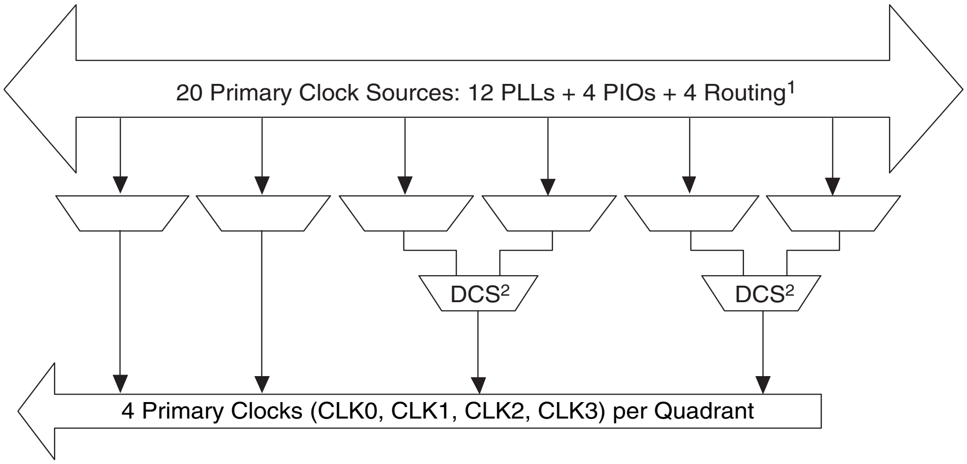
Figure 2-6. Secondary Clock Sources



Clock Routing

The clock routing structure in LatticeXP devices consists of four Primary Clock lines and a Secondary Clock network per quadrant. The primary clocks are generated from MUXs located in each quadrant. Figure 2-7 shows this clock routing. The four secondary clocks are generated from MUXs located in each quadrant as shown in Figure 2-8. Each slice derives its clock from the primary clock lines, secondary clock lines and routing as shown in Figure 2-9.

Figure 2-7. Per Quadrant Primary Clock Selection



1. Smaller devices have fewer PLL related lines.
2. Dynamic clock select.

Figure 2-23. Output Register Block

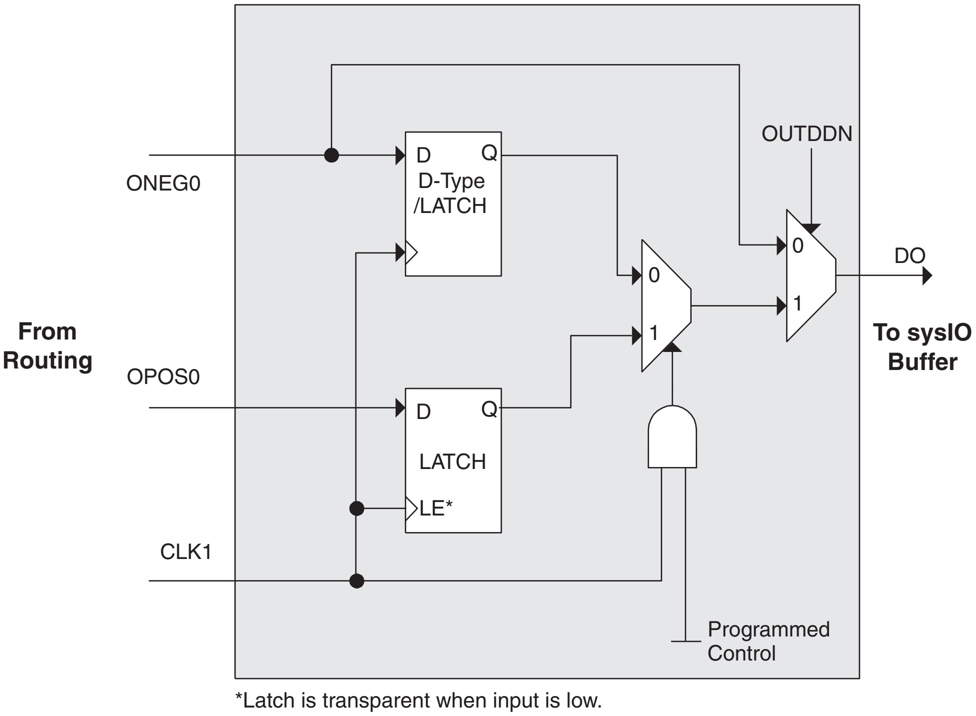
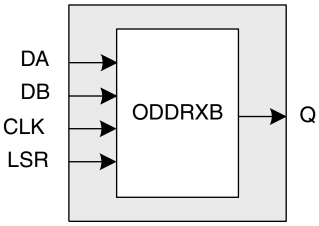


Figure 2-24. ODDRXB Primitive

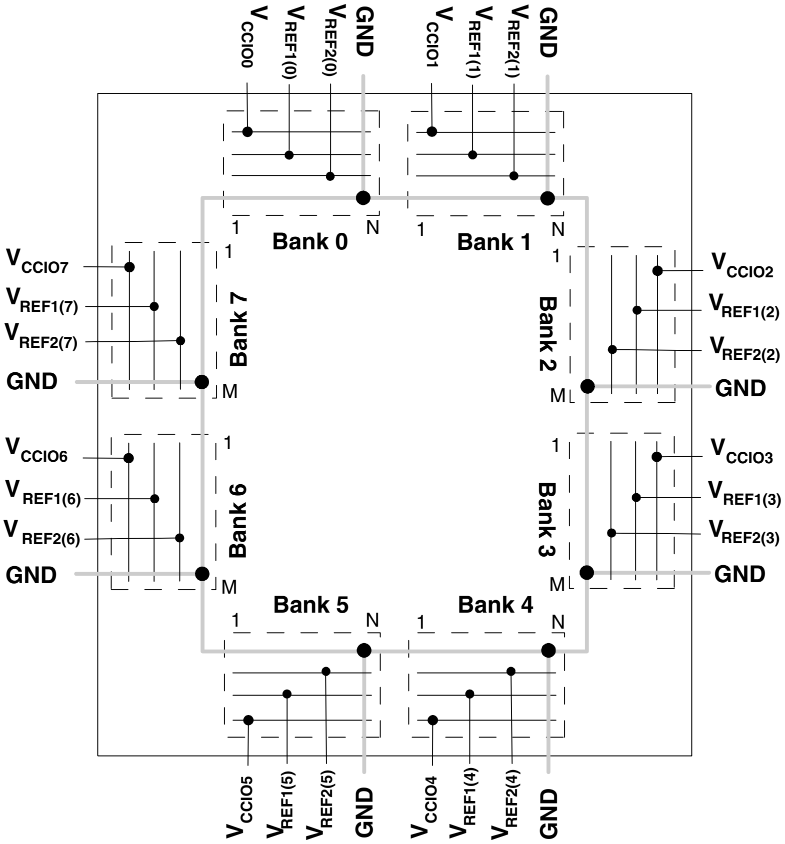


Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-25 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-28. LatticeXP Banks



Note: N and M are the maximum number of I/Os per bank.

LatticeXP devices contain two types of sysIO buffer pairs.

1. **Top and Bottom sysIO Buffer Pair (Single-Ended Outputs Only)**
   The sysIO buffer pairs in the top and bottom banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

   Only the I/Os on the top and bottom banks have PCI clamps. Note that the PCI clamp is enabled after $V_{CC,}$ V_{CCAUX} and V_{CCIO} are at valid operating levels and the device has been configured.

2. **Left and Right sysIO Buffer Pair (Differential and Single-Ended Outputs)**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. The referenced input buffer can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

   Select I/Os in the left and right banks have LVDS differential output drivers. Refer to the Logic Signal Connections tables for more information.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pull-up to VCCIO. The I/O pins will not take on the user configuration until VCC, VCCAUX and VCCIO have reached satisfactory levels at which time the I/Os will take on the user-configured settings.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported Standards

The LatticeXP sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2, 1.5, 1.8, 2.5 and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, differential SSTL and differential HSTL. Tables 2-7 and 2-8 show the I/O standards (together with their supply and reference voltages) supported by the LatticeXP devices. For further information on utilizing the sysIO buffer to support a variety of standards please see the details of additional technical documentation at the end of this data sheet.

Table 2-7. Supported Input Standards

Input Standard	V_{REF} (Nom.)	V_{CCIO}[1] (Nom.)
Single Ended Interfaces		
LVTTL	—	—
LVCMOS33[2]	—	—
LVCMOS25[2]	—	—
LVCMOS18	—	1.8
LVCMOS15	—	1.5
LVCMOS12[2]	—	—
PCI	—	3.3
HSTL18 Class I, II	0.9	—
HSTL18 Class III	1.08	—
HSTL15 Class I	0.75	—
HSTL15 Class III	0.9	—
SSTL3 Class I, II	1.5	—
SSTL2 Class I, II	1.25	—
SSTL18 Class I	0.9	—
Differential Interfaces		
Differential SSTL18 Class I	—	—
Differential SSTL2 Class I, II	—	—
Differential SSTL3 Class I, II	—	—
Differential HSTL15 Class I, III	—	—
Differential HSTL18 Class I, II, III	—	—
LVDS, LVPECL	—	—
BLVDS	—	—

1. When not specified V_{CCIO} can be set anywhere in the valid operating range.
2. JTAG inputs do not have a fixed threshold option and always follow V_{CCJ}.

Hot Socketing Specifications[1, 2, 3, 4, 5, 6]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq V_{IH}$ (MAX.)	—	—	+/-1000	µA

1. Insensitive to sequence of V_{CC}, V_{CCAUX} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC}, V_{CCAUX} and V_{CCIO}.
2. $0 \leq V_{CC} \leq V_{CC}$ (MAX) or $0 \leq V_{CCAUX} \leq V_{CCAUX}$ (MAX).
3. $0 \leq V_{CCIO} \leq V_{CCIO}$ (MAX) for top and bottom I/O banks.
4. $0.2 \leq V_{CCIO} \leq V_{CCIO}$ (MAX) for left and right I/O banks.
5. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.
6. LVCMOS and LVTTL only.

Figure 3-2. BLVDS Multi-point Output Example

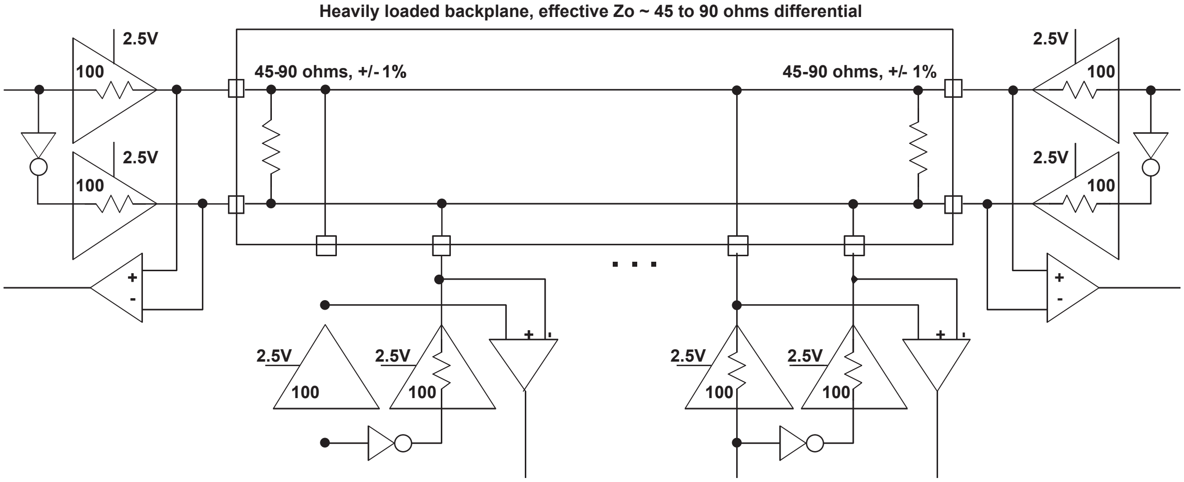


Table 3-2. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Typical		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	100	100	ohms
R_{TLEFT}	Left end termination	45	90	ohms
R_{TRIGHT}	Right end termination	45	90	ohms
V_{OH}	Output high voltage	1.375	1.48	V
V_{OL}	Output low voltage	1.125	1.02	V
V_{OD}	Output differential voltage	0.25	0.46	V
V_{CM}	Output common mode voltage	1.25	1.25	V
I_{DC}	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

LatticeXP External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Device	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (Using Primary Clock without PLL)[1]									
t_{CO}	Clock to Output - PIO Output Register	LFXP3	—	5.12	—	6.12	—	7.43	ns
		LFXP6	—	5.30	—	6.34	—	7.69	ns
		LFXP10	—	5.52	—	6.60	—	8.00	ns
		LFXP15	—	5.72	—	6.84	—	8.29	ns
		LFXP20	—	5.97	—	7.14	—	8.65	ns
t_{SU}	Clock to Data Setup - PIO Input Register	LFXP3	-0.40	—	-0.28	—	-0.16	—	ns
		LFXP6	-0.33	—	-0.32	—	-0.30	—	ns
		LFXP10	-0.61	—	-0.71	—	-0.81	—	ns
		LFXP15	-0.71	—	-0.77	—	-0.87	—	ns
		LFXP20	-0.95	—	-1.14	—	-1.35	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	LFXP3	2.10	—	2.50	—	2.98	—	ns
		LFXP6	2.28	—	2.72	—	3.24	—	ns
		LFXP10	3.02	—	3.51	—	3.71	—	ns
		LFXP15	2.70	—	3.22	—	3.85	—	ns
		LFXP20	2.95	—	3.52	—	4.21	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Input Data Delay	LFXP3	2.38	—	2.49	—	2.66	—	ns
		LFXP6	2.92	—	3.18	—	3.42	—	ns
		LFXP10	2.72	—	2.75	—	2.84	—	ns
		LFXP15	2.99	—	3.13	—	3.18	—	ns
		LFXP20	4.47	—	4.56	—	4.80	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFXP3	-0.70	—	-0.80	—	-0.92	—	ns
		LFXP6	-0.47	—	-0.38	—	-0.31	—	ns
		LFXP10	-0.60	—	-0.47	—	-0.32	—	ns
		LFXP15	-1.05	—	-0.98	—	-1.01	—	ns
		LFXP20	-0.80	—	-0.58	—	-0.31	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All	—	400	—	360	—	320	MHz
DDR I/O Pin Parameters[2]									
t_{DVADQ}	Data Valid After DQS (DDR Read)	All	—	0.19	—	0.19	—	0.19	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	All	0.67	—	0.67	—	0.67	—	UI
t_{DQVBS}	Data Valid Before DQS	All	0.20	—	0.20	—	0.20	—	UI
t_{DQVAS}	Data Valid After DQS	All	0.20	—	0.20	—	0.20	—	UI
f_{MAX_DDR}	DDR Clock Frequency	All	95	166	95	133	95	100	MHz
Primary and Secondary Clocks									
f_{MAX_PRI}	Frequency for Primary Clock Tree	All	—	450	—	412	—	375	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All	1.19	—	1.19	—	1.19	—	ns
t_{SKEW_PRI}	Primary Clock Skew within an I/O Bank	LFXP3/6/10/15	—	250	—	300	—	350	ps
		LFXP20	—	300	—	350	—	400	ps

1. General timing numbers based on LVCMOS 2.5, 12mA.
2. DDR timing numbers based on SSTL I/O.

Timing v.F0.11

LatticeXP Internal Timing Parameters[1] (Continued)

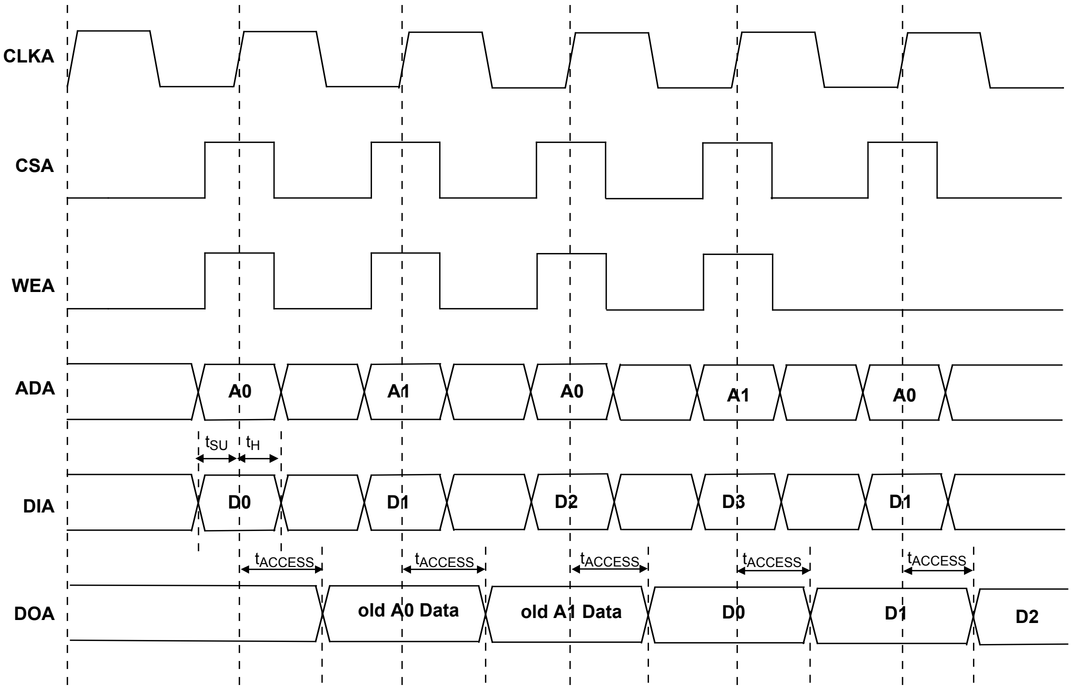
Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register	—	1.61	—	1.94	—	2.32	ns
PLL Parameters								
t_{RSTREC}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
t_{RSTSU}	Reset Signal Setup Time	1.00	—	1.00	—	1.00	—	ns

1. Internal parameters are characterized but not tested on every device.

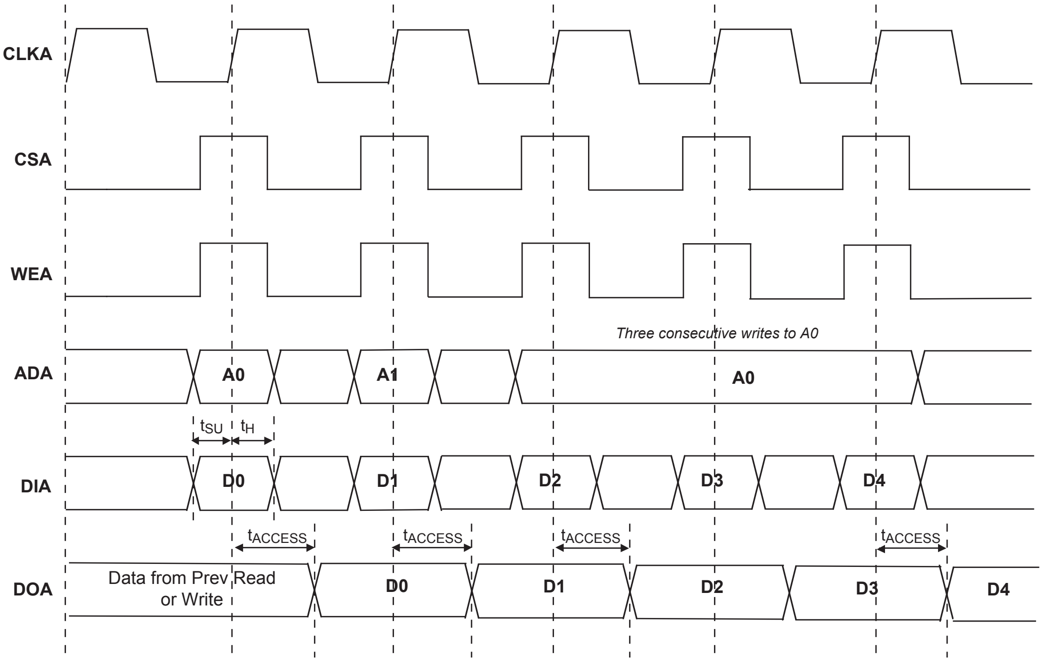
Timing v.F0.11

Figure 3-10. Read Before Write (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

Figure 3-11. Write Through (SP Read/Write On Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

LatticeXP Family Data Sheet
Pinout Information

November 2007 **Data Sheet DS1001**

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
P[Edge] [Row/Column Number*]_[A/B]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic. During configuration, the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
GSRN	I	Global RESET signal. (Active low). Any I/O pin can be configured to be GSRN.
NC	—	No connect.
GND	—	GND - Ground. Dedicated Pins.
V_{CC}	—	VCC - The power supply pins for core logic. Dedicated Pins.
V_{CCAUX}	—	V_{CCAUX} - The Auxiliary power supply pin. It powers all the differential and referenced input buffers. Dedicated Pins.
V_{CCP0}	—	Voltage supply pins for ULM0PLL (and LLM1PLL[1]).
V_{CCP1}	—	Voltage supply pins for URM0PLL (and LRM1PLL[1]).
GNDP0	—	Ground pins for ULM0PLL (and LLM1PLL[1]).
GNDP1	—	Ground pins for URM0PLL (and LRM1PLL[1]).
V_{CCIOx}	—	V_{CCIO} - The power supply pins for I/O bank x. Dedicated Pins.
$V_{REF1(x)}$, $V_{REF2(x)}$	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V_{REF} inputs. When not used, they may be used as I/O pins.
PLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_PLL[T, C]_IN_A	—	Reference clock (PLL) input Pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A, B, C...at each side.
[LOC][num]_PLL[T, C]_FB_A	—	Optional feedback (PLL) input Pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A, B, C...at each side.
PCLK[T, C]_[n:0]_[3:0]	—	Primary Clock Pads, T = true and C = complement, n per side, indexed by bank and 0,1, 2, 3 within bank.
[LOC]DQS[num]	—	DQS input Pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = Ball function number. Any pad can be configured to be DQS output.

Pin Information Summary[1]

Pin Type		XP3			XP6		
		100 TQFP	144 TQFP	208 PQFP	144 TQFP	208 PQFP	256 fpBGA
Single Ended User I/O		62	100	136	100	142	188
Differential Pair User I/O[2]		19	35	56	35	58	80
Configuration	Dedicated	11	11	11	11	11	11
	Muxed	14	14	14	14	14	14
TAP		5	5	5	5	5	5
Dedicated (total without supplies)		6	6	6	6	6	6
V_{CC}		2	4	8	4	8	8
V_{CCAUX}		2	2	2	2	2	4
V_{CCPLL}		2	2	2	2	2	2
V_{CCIO}	Bank0	1	1	2	1	2	2
	Bank1	1	1	2	1	2	2
	Bank2	1	1	2	1	2	2
	Bank3	1	1	2	1	2	2
	Bank4	1	2	2	2	2	2
	Bank5	1	1	2	1	2	2
	Bank6	1	1	2	1	2	2
	Bank7	1	1	2	1	2	2
GND		10	13	24	13	24	24
GND_{PLL}		2	2	2	2	2	2
NC		0	0	6	0	0	0
Single Ended/Differential I/O per Bank[2]	Bank0	8/2	12/3	20/8	12/3	20/8	26/11
	Bank1	9/0	12/2	18/6	12/2	18/6	26/11
	Bank2	8/3	12/5	14/6	12/5	17/7	21/9
	Bank3	6/2	13/5	14/6	13/5	14/6	21/9
	Bank4	5/2	14/6	21/9	14/6	21/9	26/11
	Bank5	12/4	12/4	21/9	12/4	21/9	26/11
	Bank6	4/2	13/5	14/6	13/5	17/7	21/9
	Bank7	10/4	12/5	14/6	12/5	14/6	21/9
V_{CCJ}		1	1	1	1	1	1

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
2. The differential I/O per bank includes both dedicated LVDS and emulated LVDS pin pairs. Please see the Logic Signal Connections table for more information.

Pin Information Summary[1] (Cont.)

Pin Type		XP10		XP15			XP20		
		256 fpBGA	388 fpBGA	256 fpBGA	388 fpBGA	484 fpBGA	256 fpBGA	388 fpBGA	484 fpBGA
Single Ended User I/O		188	244	188	268	300	188	268	340
Differential Pair User I/O[2]		76	104	76	112	128	76	112	144
Configuration	Dedicated	11	11	11	11	11	11	11	11
	Muxed	14	14	14	14	14	14	14	14
TAP		5	5	5	5	5	5	5	5
Dedicated (total without supplies)		6	6	6	6	6	6	6	6
V_{CC}		8	14	8	14	28	8	14	28
V_{CCAUX}		4	4	4	4	12	4	4	12
V_{CCPLL}		2	2	2	2	2	2	2	2
V_{CCIO}	Bank0	2	5	2	5	4	2	5	4
	Bank1	2	5	2	5	4	2	5	4
	Bank2	2	4	2	4	4	2	4	4
	Bank3	2	4	2	4	4	2	4	4
	Bank4	2	5	2	5	4	2	5	4
	Bank5	2	5	2	5	4	2	5	4
	Bank6	2	4	2	4	4	2	4	4
	Bank7	2	4	2	4	4	2	4	4
GND		24	50	24	50	56	24	50	56
GND_{PLL}		2	2	2	2	2	2	2	2
NC		0	24	0	0	40	0	0	0
Single Ended/ Differential I/O per Bank[2]	Bank0	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank1	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank2	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank3	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank4	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank5	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank6	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank7	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
V_{CCJ}		1	1	1	1	1	1	1	1

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
2. The differential I/O per bank includes both dedicated LVDS and emulated LVDS pin pairs. Please see the Logic Signal Connections table for more information.

LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
139	PT6A	0	-	DI	PT9A	0	-	DI
140	PT5A	0	-	CSN	PT8A	0	-	CSN
141	PT3B	0	-	VREF2_0	PT6B	0	-	VREF2_0
142	CFG0	0	-	-	CFG0	0	-	-
143	CFG1	0	-	-	CFG1	0	-	-
144	DONE	0	-	-	DONE	0	-	-

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

	LFXP6				LFXP10			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L15	PR21B	3	C[3]	-	PR28B	3	C[3]	-
L14	PR21A	3	T[3]	-	PR28A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
L12	PR17B	3	C	-	PR26A	3	-	-
M16	PR20B	3	C	-	PR25B	3	C	RLM0_PLLC_IN_A
N16	PR20A	3	T	-	PR25A	3	T	RLM0_PLLT_IN_A
K14	PR19B	3	C[3]	-	PR24B	3	C[3]	-
K15	PR19A	3	T[3]	-	PR24A	3	T[3]	DQS
K12	PR17A	3	T	-	PR23B	3	-	-
K13	PR22A	3	-	VREF2_3	PR22A	3	-	VREF2_3
-	GNDIO3	3	-	-	GNDIO3	3	-	-
L16	PR18B	3	C[3]	-	PR21B	3	C[3]	-
K16	PR18A	3	T[3]	-	PR21A	3	T[3]	-
J15	PR16B	3	C[3]	-	PR19B	3	C[3]	-
J14	PR16A	3	T[3]	-	PR19A	3	T[3]	-
J13	GNDP1	-	-	-	GNDP1	-	-	-
J12	VCCP1	-	-	-	VCCP1	-	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
J16	PR12B	2	C	PCLKC2_0	PR17B	2	C	PCLKC2_0
H16	PR12A	2	T	PCLKT2_0	PR17A	2	T	PCLKT2_0
H13	PR13B	2	C[3]	-	PR16B	2	C[3]	-
H12	PR13A	2	T[3]	-	PR16A	2	T[3]	DQS
H15	PR2B	2	C[3]	-	PR15B	2	-	-
H14	PR6B	2	-	VREF1_2	PR14A	2	-	VREF1_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G15	PR11B	2	C[3]	-	PR13B	2	C[3]	-
G14	PR11A	2	T[3]	-	PR13A	2	T[3]	-
G16	PR8B	2	C	RUM0_PLLC_IN_A	PR12B	2	C	RUM0_PLLC_IN_A
F16	PR8A	2	T	RUM0_PLLT_IN_A	PR12A	2	T	RUM0_PLLT_IN_A
G13	PR2A	2	T[3]	-	PR11B	2	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G12	PR9B	2	C[3]	-	PR8B	2	C	-
F13	PR9A	2	T[3]	-	PR8A	2	T	-
B16	PR7B	2	C[3]	-	PR7B	2	C[3]	-
C16	PR7A	2	T[3]	DQS	PR7A	2	T[3]	DQS
F15	PR14A	2	-	-	PR6B	2	-	-
E15	PR5A	2	-	VREF2_2	PR5A	2	-	VREF2_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
F14	PR4B	2	C[3]	-	PR4B	2	C[3]	-
E14	PR4A	2	T[3]	-	PR4A	2	T[3]	-
D15	PR3B	2	C	RUM0_PLLC_FB_A	PR3B	2	C	RUM0_PLLC_FB_A
C15	PR3A	2	T	RUM0_PLLT_FB_A	PR3A	2	T	RUM0_PLLT_FB_A

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

	LFXP6				LFXP10			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
K10	GND	-	-	-	GND	-	-	-
K7	GND	-	-	-	GND	-	-	-
K8	GND	-	-	-	GND	-	-	-
K9	GND	-	-	-	GND	-	-	-
L11	GND	-	-	-	GND	-	-	-
L6	GND	-	-	-	GND	-	-	-
T1	GND	-	-	-	GND	-	-	-
T16	GND	-	-	-	GND	-	-	-
D13	VCC	-	-	-	VCC	-	-	-
D4	VCC	-	-	-	VCC	-	-	-
E12	VCC	-	-	-	VCC	-	-	-
E5	VCC	-	-	-	VCC	-	-	-
M12	VCC	-	-	-	VCC	-	-	-
M5	VCC	-	-	-	VCC	-	-	-
N13	VCC	-	-	-	VCC	-	-	-
N4	VCC	-	-	-	VCC	-	-	-
E13	VCCAUX	-	-	-	VCCAUX	-	-	-
E4	VCCAUX	-	-	-	VCCAUX	-	-	-
M13	VCCAUX	-	-	-	VCCAUX	-	-	-
M4	VCCAUX	-	-	-	VCCAUX	-	-	-
F7	VCCIO0	0	-	-	VCCIO0	0	-	-
F8	VCCIO0	0	-	-	VCCIO0	0	-	-
F10	VCCIO1	1	-	-	VCCIO1	1	-	-
F9	VCCIO1	1	-	-	VCCIO1	1	-	-
G11	VCCIO2	2	-	-	VCCIO2	2	-	-
H11	VCCIO2	2	-	-	VCCIO2	2	-	-
J11	VCCIO3	3	-	-	VCCIO3	3	-	-
K11	VCCIO3	3	-	-	VCCIO3	3	-	-
L10	VCCIO4	4	-	-	VCCIO4	4	-	-
L9	VCCIO4	4	-	-	VCCIO4	4	-	-
L7	VCCIO5	5	-	-	VCCIO5	5	-	-
L8	VCCIO5	5	-	-	VCCIO5	5	-	-
J6	VCCIO6	6	-	-	VCCIO6	6	-	-
K6	VCCIO6	6	-	-	VCCIO6	6	-	-
G6	VCCIO7	7	-	-	VCCIO7	7	-	-
H6	VCCIO7	7	-	-	VCCIO7	7	-	-

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

	LFXP15				LFXP20			
Ball Number	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
R18	PR38B	3	C	RLM0_PLLC_FB_A	PR42B	3	C	RLM0_PLLC_FB_A
R17	PR38A	3	T	RLM0_PLLT_FB_A	PR42A	3	T	RLM0_PLLT_FB_A
Y22	PR37B	3	C[3]	-	PR41B	3	C[3]	-
Y21	PR37A	3	T[3]	DQS	PR41A	3	T[3]	DQS
W22	PR36B	3	-	-	PR40B	3	-	-
W21	PR35A	3	-	VREF1_3	PR39A	3	-	VREF1_3
P17	PR34B	3	C[3]	-	PR38B	3	C[3]	-
P18	PR34A	3	T[3]	-	PR38A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
R19	PR33B	3	C	-	PR37B	3	C	-
R20	PR33A	3	T	-	PR37A	3	T	-
V22	PR32B	3	C[3]	-	PR36B	3	C[3]	-
V21	PR32A	3	T[3]	-	PR36A	3	T[3]	-
U22	PR30B	3	C[3]	-	PR34B	3	C[3]	-
U21	PR30A	3	T[3]	-	PR34A	3	T[3]	-
P19	PR29B	3	C	RLM0_PLLC_IN_A	PR33B	3	C	RLM0_PLLC_IN_A
P20	PR29A	3	T	RLM0_PLLT_IN_A	PR33A	3	T	RLM0_PLLT_IN_A
-	GNDIO3	3	-	-	GNDIO3	3	-	-
T22	PR28B	3	C[3]	-	PR32B	3	C[3]	-
T21	PR28A	3	T[3]	DQS	PR32A	3	T[3]	DQS
R22	PR27B	3	-	-	PR31B	3	-	-
R21	PR26A	3	-	VREF2_3	PR30A	3	-	VREF2_3
N19	PR25B	3	C[3]	-	PR29B	3	C[3]	-
N20	PR25A	3	T[3]	-	PR29A	3	T[3]	-
N18	PR24B	3	C	-	PR28B	3	C	-
M18	PR24A	3	T	-	PR28A	3	T	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
P22	PR23B	3	C[3]	-	PR27B	3	C[3]	-
P21	PR23A	3	T[3]	-	PR27A	3	T[3]	-
N22	-	-	-	-	PR26B	3	C[3]	-
N21	-	-	-	-	PR26A	3	T[3]	-
M19	-	-	-	-	PR25B	3	-	-
M20	GNDP1	-	-	-	GNDP1	-	-	-
L18	VCCP1	-	-	-	VCCP1	-	-	-
M21	-	-	-	-	PR24A	2	-	-
M22	PR22B	2	C[3]	-	PR23B	2	C[3]	-
L22	PR22A	2	T[3]	-	PR23A	2	T[3]	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
L19	-	-	-	-	PR22B	2	C[3]	-
L20	-	-	-	-	PR22A	2	T[3]	-
L21	PR21B	2	C	PCLKC2_0	PR21B	2	C	PCLKC2_0
K22	PR21A	2	T	PCLKT2_0	PR21A	2	T	PCLKT2_0

Commercial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6E-3F256C	188	1.2V	-3	fpBGA	256	COM	5.8K
LFXP6E-4F256C	188	1.2V	-4	fpBGA	256	COM	5.8K
LFXP6E-5F256C	188	1.2V	-5	fpBGA	256	COM	5.8K
LFXP6E-3Q208C	142	1.2V	-3	PQFP	208	COM	5.8K
LFXP6E-4Q208C	142	1.2V	-4	PQFP	208	COM	5.8K
LFXP6E-5Q208C	142	1.2V	-5	PQFP	208	COM	5.8K
LFXP6E-3T144C	100	1.2V	-3	TQFP	144	COM	5.8K
LFXP6E-4T144C	100	1.2V	-4	TQFP	144	COM	5.8K
LFXP6E-5T144C	100	1.2V	-5	TQFP	144	COM	5.8K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10E-3F388C	244	1.2V	-3	fpBGA	388	COM	9.7K
LFXP10E-4F388C	244	1.2V	-4	fpBGA	388	COM	9.7K
LFXP10E-5F388C	244	1.2V	-5	fpBGA	388	COM	9.7K
LFXP10E-3F256C	188	1.2V	-3	fpBGA	256	COM	9.7K
LFXP10E-4F256C	188	1.2V	-4	fpBGA	256	COM	9.7K
LFXP10E-5F256C	188	1.2V	-5	fpBGA	256	COM	9.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15E-3F484C	300	1.2V	-3	fpBGA	484	COM	15.5K
LFXP15E-4F484C	300	1.2V	-4	fpBGA	484	COM	15.5K
LFXP15E-5F484C	300	1.2V	-5	fpBGA	484	COM	15.5K
LFXP15E-3F388C	268	1.2V	-3	fpBGA	388	COM	15.5K
LFXP15E-4F388C	268	1.2V	-4	fpBGA	388	COM	15.5K
LFXP15E-5F388C	268	1.2V	-5	fpBGA	388	COM	15.5K
LFXP15E-3F256C	188	1.2V	-3	fpBGA	256	COM	15.5K
LFXP15E-4F256C	188	1.2V	-4	fpBGA	256	COM	15.5K
LFXP15E-5F256C	188	1.2V	-5	fpBGA	256	COM	15.5K

Commercial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20E-3F484C	340	1.2V	-3	fpBGA	484	COM	19.7K
LFXP20E-4F484C	340	1.2V	-4	fpBGA	484	COM	19.7K
LFXP20E-5F484C	340	1.2V	-5	fpBGA	484	COM	19.7K
LFXP20E-3F388C	268	1.2V	-3	fpBGA	388	COM	19.7K
LFXP20E-4F388C	268	1.2V	-4	fpBGA	388	COM	19.7K
LFXP20E-5F388C	268	1.2V	-5	fpBGA	388	COM	19.7K
LFXP20E-3F256C	188	1.2V	-3	fpBGA	256	COM	19.7K
LFXP20E-4F256C	188	1.2V	-4	fpBGA	256	COM	19.7K
LFXP20E-5F256C	188	1.2V	-5	fpBGA	256	COM	19.7K

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3C-3Q208I	136	1.8/2.5/3.3V	-3	PQFP	208	IND	3.1K
LFXP3C-4Q208I	136	1.8/2.5/3.3V	-4	PQFP	208	IND	3.1K
LFXP3C-3T144I	100	1.8/2.5/3.3V	-3	TQFP	144	IND	3.1K
LFXP3C-4T144I	100	1.8/2.5/3.3V	-4	TQFP	144	IND	3.1K
LFXP3C-3T100I	62	1.8/2.5/3.3V	-3	TQFP	100	IND	3.1K
LFXP3C-4T100I	62	1.8/2.5/3.3V	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6C-3F256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	5.8K
LFXP6C-4F256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	5.8K
LFXP6C-3Q208I	142	1.8/2.5/3.3V	-3	PQFP	208	IND	5.8K
LFXP6C-4Q208I	142	1.8/2.5/3.3V	-4	PQFP	208	IND	5.8K
LFXP6C-3T144I	100	1.8/2.5/3.3V	-3	TQFP	144	IND	5.8K
LFXP6C-4T144I	100	1.8/2.5/3.3V	-4	TQFP	144	IND	5.8K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10C-3F388I	244	1.8/2.5/3.3V	-3	fpBGA	388	IND	9.7K
LFXP10C-4F388I	244	1.8/2.5/3.3V	-4	fpBGA	388	IND	9.7K
LFXP10C-3F256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	9.7K
LFXP10C-4F256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	9.7K

Commercial (Cont.)

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20C-3FN484C	340	1.8/2.5/3.3V	-3	fpBGA	484	COM	19.7K
LFXP20C-4FN484C	340	1.8/2.5/3.3V	-4	fpBGA	484	COM	19.7K
LFXP20C-5FN484C	340	1.8/2.5/3.3V	-5	fpBGA	484	COM	19.7K
LFXP20C-3FN388C	268	1.8/2.5/3.3V	-3	fpBGA	388	COM	19.7K
LFXP20C-4FN388C	268	1.8/2.5/3.3V	-4	fpBGA	388	COM	19.7K
LFXP20C-5FN388C	268	1.8/2.5/3.3V	-5	fpBGA	388	COM	19.7K
LFXP20C-3FN256C	188	1.8/2.5/3.3V	-3	fpBGA	256	COM	19.7K
LFXP20C-4FN256C	188	1.8/2.5/3.3V	-4	fpBGA	256	COM	19.7K
LFXP20C-5FN256C	188	1.8/2.5/3.3V	-5	fpBGA	256	COM	19.7K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3E-3QN208C	136	1.2V	-3	PQFP	208	COM	3.1K
LFXP3E-4QN208C	136	1.2V	-4	PQFP	208	COM	3.1K
LFXP3E-5QN208C	136	1.2V	-5	PQFP	208	COM	3.1K
LFXP3E-3TN144C	100	1.2V	-3	TQFP	144	COM	3.1K
LFXP3E-4TN144C	100	1.2V	-4	TQFP	144	COM	3.1K
LFXP3E-5TN144C	100	1.2V	-5	TQFP	144	COM	3.1K
LFXP3E-3TN100C	62	1.2V	-3	TQFP	100	COM	3.1K
LFXP3E-4TN100C	62	1.2V	-4	TQFP	100	COM	3.1K
LFXP3E-5TN100C	62	1.2V	-5	TQFP	100	COM	3.1K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6E-3FN256C	188	1.2V	-3	fpBGA	256	COM	5.8K
LFXP6E-4FN256C	188	1.2V	-4	fpBGA	256	COM	5.8K
LFXP6E-5FN256C	188	1.2V	-5	fpBGA	256	COM	5.8K
LFXP6E-3QN208C	142	1.2V	-3	PQFP	208	COM	5.8K
LFXP6E-4QN208C	142	1.2V	-4	PQFP	208	COM	5.8K
LFXP6E-5QN208C	142	1.2V	-5	PQFP	208	COM	5.8K
LFXP6E-3TN144C	100	1.2V	-3	TQFP	144	COM	5.8K
LFXP6E-4TN144C	100	1.2V	-4	TQFP	144	COM	5.8K
LFXP6E-5TN144C	100	1.2V	-5	TQFP	144	COM	5.8K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10E-3FN388C	244	1.2V	-3	fpBGA	388	COM	9.7K
LFXP10E-4FN388C	244	1.2V	-4	fpBGA	388	COM	9.7K
LFXP10E-5FN388C	244	1.2V	-5	fpBGA	388	COM	9.7K
LFXP10E-3FN256C	188	1.2V	-3	fpBGA	256	COM	9.7K
LFXP10E-4FN256C	188	1.2V	-4	fpBGA	256	COM	9.7K
LFXP10E-5FN256C	188	1.2V	-5	fpBGA	256	COM	9.7K

Date	Version	Section	Change Summary
September 2005 (cont.)	03.0 (cont.)	DC and Switching Characteristics (cont.)	Updated Typical Building Block Function Performance timing numbers.
			Updated External Switching Characteristics timing numbers.
			Updated Internal Timing Parameters.
			Updated LatticeXP Family timing adders.
			Updated LatticeXP "C" Sleep Mode timing numbers.
			Updated JTAG Port Timing numbers.
		Pinout Information	Added clarification to SLEEPN and TOE description.
			Clarification of dedicated LVDS outputs.
		Supplemental Information	Updated list of technical notes.
September 2005	03.1	Pinout Information	Power Supply and NC Connections table corrected VCCP1 pin number for 208 PQFP.
December 2005	04.0	Introduction	Moved data sheet from Advance to Final.
		Architecture	Added clarification to Typical I/O Behavior During Power-up section.
		DC and Switching Characteristics	Added clarification to Recommended Operating Conditions.
			Updated timing numbers.
		Pinout Information	Updated Signal Descriptions table.
			Added clarification to Differential I/O Per Bank.
			Updated Differential dedicated LVDS output support.
		Ordering Information	Added 208 PQFP lead-free package and ordering part numbers.
February 2006	04.1	Pinout Information	Corrected description of Signal Names VREF1(x) and VREF2(x).
March 2006	04.2	DC and Switching Characteristics	Corrected condition for IIL and IIH.
March 2006	04.3	DC and Switching Characteristics	Added clarification to Recommended Operating Conditions for VCCAUX.
April 2006	04.4	Pinout Information	Removed Bank designator "5" from SLEEPN/TOE ball function.
May 2006	04.5	DC and Switching Characteristics	Added footnote 2 regarding threshold level for PROGRAMN to sysCONFIG Port Timing Specifications table.
June 2006	04.6	DC and Switching Characteristics	Corrected LVDS25E Output Termination Example.
August 2006	04.7	Architecture	Added clarification to Typical I/O Behavior During Power-Up section.
			Added clarification to Left and Right sysIO Buffer Pair section.
		DC and Switching Characteristics	Changes to LVDS25E Output Termination Example diagram.
December 2006	04.8	Architecture	EBR Asynchronous Reset section added.
February 2007	04.9	Architecture	Updated EBR Asynchronous Reset section.
July 2007	05.0	Introduction	Updated LatticeXP Family Selection Guide table.
		Architecture	Updated Typical I/O Behavior During Power-up text section.
		DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics table. Split out LVCMOS 1.2 by supply voltage.
November 2007	05.1	DC and Switching Characteristics	Added JTAG Port Timing Waveforms diagram.
		Pinout Information	Added Thermal Management text section.
		Supplemental Information	Updated title list.