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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6000
Total RAM Bits	73728
Number of I/O	188
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp6e-3fn256i

Table 2-4. PFU Modes of Operation

Logic	Ripple	RAM[1]	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR16x2 x 4 DPR16x2 x 2	ROM16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR16x4 x 2 DPR16x4 x 1	ROM16x2 x 4
LUT 6x 2 or MUX 8x1 x 2	2-bit Counter x 4	SPR16x8 x 1	ROM16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM16x8 x 1

1. These modes are not available in PFF blocks

Routing

There are many resources provided in the LatticeXP devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal, vertical and diagonal directions. The x2 and x6 resources are buffered allowing both short and long connections routing between PFUs.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

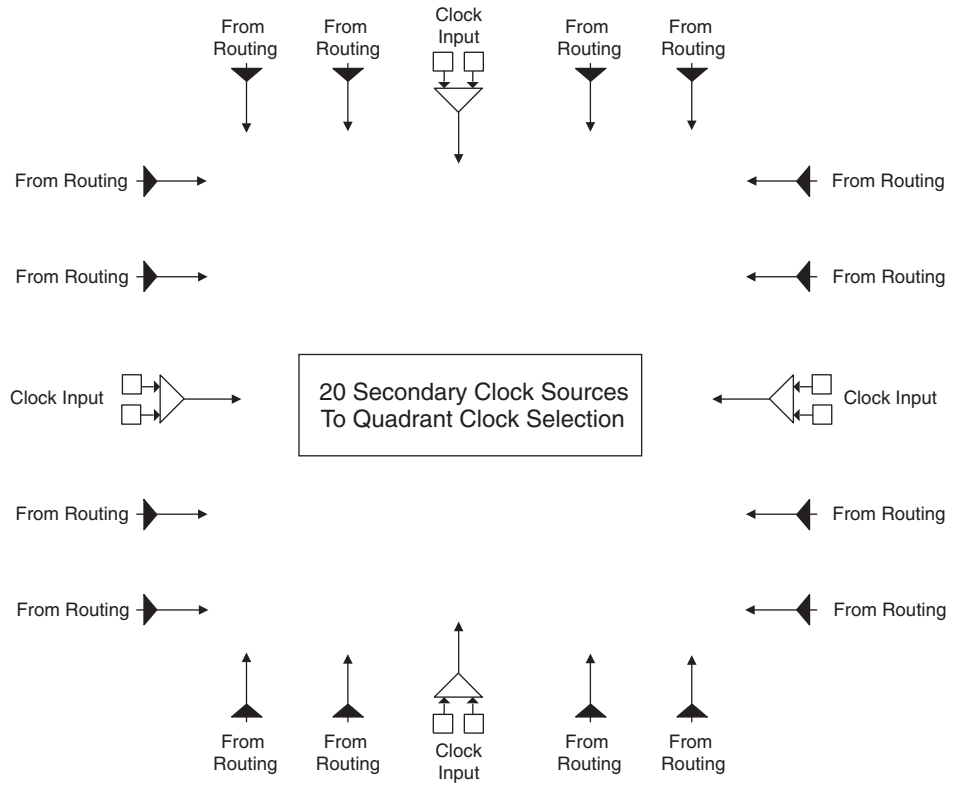
Clock Distribution Network

The clock inputs are selected from external I/O, the sysCLOCK™ PLLs or routing. These clock inputs are fed through the chip via a clock distribution system.

Primary Clock Sources

LatticeXP devices derive clocks from three primary sources: PLL outputs, dedicated clock inputs and routing. LatticeXP devices have two to four sysCLOCK PLLs, located on the left and right sides of the device. There are four dedicated clock inputs, one on each side of the device. Figure 2-5 shows the 20 primary clock sources.

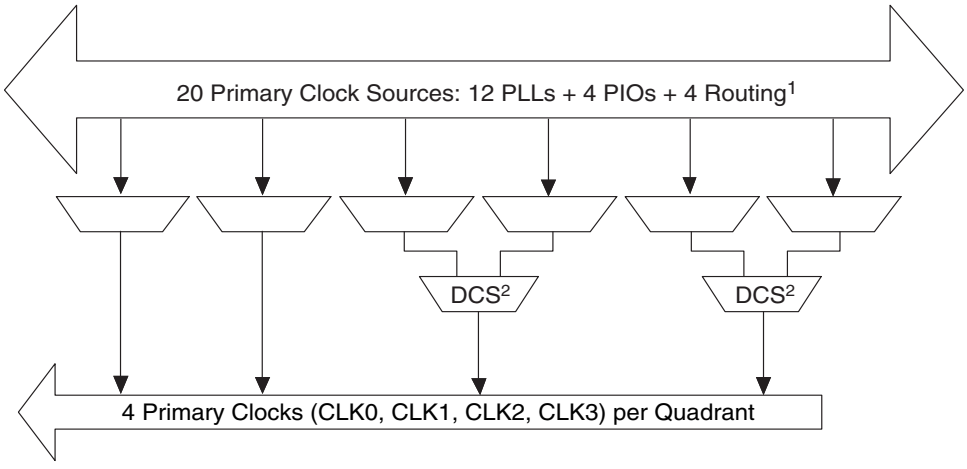
Figure 2-6. Secondary Clock Sources



Clock Routing

The clock routing structure in LatticeXP devices consists of four Primary Clock lines and a Secondary Clock network per quadrant. The primary clocks are generated from MUXs located in each quadrant. Figure 2-7 shows this clock routing. The four secondary clocks are generated from MUXs located in each quadrant as shown in Figure 2-8. Each slice derives its clock from the primary clock lines, secondary clock lines and routing as shown in Figure 2-9.

Figure 2-7. Per Quadrant Primary Clock Selection



1. Smaller devices have fewer PLL related lines.
2. Dynamic clock select.

Table 2-6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

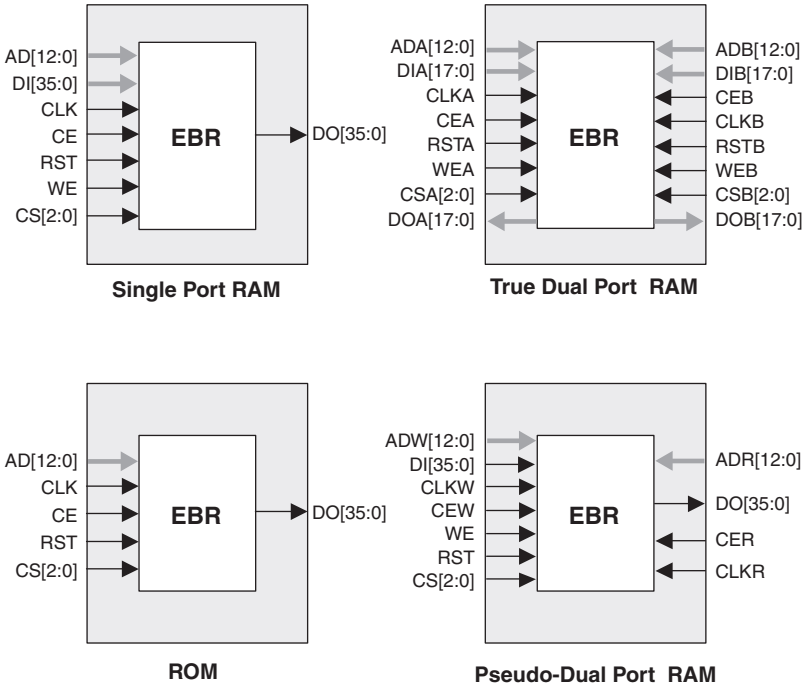
Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

Figure 2-14 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

Figure 2-14. sysMEM Memory Primitives



The EBR memory supports three forms of write behavior for single port or dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** -þa copy of the input data appears at the output of the same port during a write cycle.þThis mode is supported for all data widths.

3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-15.

Polarity Control Logic

In a typical DDR Memory interface design, the phase relation between the incoming delayed DQS strobe and the internal system Clock (during the READ cycle) is unknown.

The LatticeXP family contains dedicated circuits to transfer data between these domains. To prevent setup and hold violations at the domain transfer between DQS (delayed) and the system Clock a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of the each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in eight groups referred to as Banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

sysIO Buffer Banks

LatticeXP devices have eight sysIO buffer banks; each is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCIO}), and two voltage references V_{REF1} and V_{REF2} resources allowing each bank to be completely independent from each other. Figure 2-28 shows the eight banks and their associated supplies.

In the LatticeXP devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS, PCI and PCI-X) are powered using V_{CCIO}. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as a fixed threshold input independent of $V_{CCIO.}$ In addition to the bank V_{CCIO} supplies, the LatticeXP devices have a V_{CC} core logic power supply, and a V_{CCAUX} supply that power all differential and referenced buffers.

Each bank can support up to two separate VREF voltages, VREF1 and VREF2 that set the threshold for the referenced input buffers. In the LatticeXP devices, a dedicated pin in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

LatticeXP Family Data Sheet DC and Switching Characteristics

November 2007 Data Sheet DS1001

Absolute Maximum Ratings[1, 2, 3, 4]

	XPE (1.2V)	XPC (1.8V/2.5V/3.3V)
Supply Voltage V_{CC}	-0.5 to 1.32V	-0.5 to 3.75V
Supply Voltage V_{CCP}	-0.5 to 1.32V	-0.5 to 3.75V
Supply Voltage V_{CCAUX}	-0.5 to 3.75V	-0.5 to 3.75V
Supply Voltage V_{CCJ}	-0.5 to 3.75V	-0.5 to 3.75V
Output Supply Voltage V_{CCIO}	-0.5 to 3.75V	-0.5 to 3.75V
I/O Tristate Voltage Applied[5]	-0.5 to 3.75V	-0.5 to 3.75V
Dedicated Input Voltage Applied [5]	-0.5 to 3.75V	-0.5 to 4.25V
Storage Temperature (Ambient)	-65 to 150°C	-65 to 150°C
Junction Temp. (Tj)	+125°C	+125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions outside of those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. All chip grounds are connected together to a common package GND plane.
5. Overshoot and undershoot of -2V to (V_{IHMAX} + 2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions[3]

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Core Supply Voltage for 1.2V Devices	1.14	1.26	V
	Core Supply Voltage for 1.8V/2.5V/3.3V Devices	1.71	3.465	V
V_{CCP}	Supply Voltage for PLL for 1.2V Devices	1.14	1.26	V
	Supply Voltage for PLL for 1.8V/2.5V/3.3V Devices	1.71	3.465	V
V_{CCAUX}[4]	Auxiliary Supply Voltage	3.135	3.465	V
V_{CCIO}[1, 2]	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}[1]	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	85	C
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	C
$t_{JFLASHCOM}$	Junction Temperature, Flash Programming, Commercial	0	85	C
$t_{JFLASHIND}$	Junction Temperature, Flash Programming, Industrial	0	85	C

1. If V_{CCIO} or V_{CCJ} is set to 3.3V, they must be connected to the same power supply as V_{CCAUX}. For the XPE devices (1.2V V_{CC}), if V_{CCIO} or V_{CCJ} is set to 1.2V, they must be connected to the same power supply as V_{CC}.
2. See recommended voltages by I/O standard in subsequent table.
3. The system designer must ensure that the FPGA design stays within the specified junction temperature and package thermal capabilities of the device based on the expected operating frequency, activity factor and environment conditions of the system.
4. V_{CCAUX} ramp rate must not exceed 30mV/µs during power up when transitioning between 0V and 3.3V.

Supply Current (Standby)[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LFXP3E	15	mA
		LFXP6E	20	mA
		LFXP10E	35	mA
		LFXP15E	45	mA
		LFXP20E	55	mA
		LFXP3C	35	mA
		LFXP6C	40	mA
		LFXP10C	70	mA
		LFXP15C	80	mA
		LFXP20C	90	mA
I_{CCP}	PLL Power Supply (per PLL)	All	8	mA
I_{CCAUX}	Auxiliary Power Supply V_{CCAUX} = 3.3V	LFXP3E/C	22	mA
		LFXP6E/C	22	mA
		LFXP10E/C	30	mA
		LFXP15E/C	30	mA
		LFXP20E/C	30	mA
I_{CCIO}	Bank Power Supply[6]	All	2	mA
I_{CCJ}	V_{CCJ} Power Supply	All	1	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the VCCIO or GND.
3. Frequency 0MHz.
4. User pattern: blank.
5. T_A=25°C, power supplies at nominal voltage.
6. Per bank.

sysIO Differential Electrical Characteristics

LVDS

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage		0	—	2.4	V
V_{THD}	Differential Input Threshold		+/-100	—	—	mV
V_{CM}	Input Common Mode Voltage	100mV ≤ V_{THD}	V_{THD}/2	1.2	1.8	V
		200mV ≤ V_{THD}	V_{THD}/2	1.2	1.9	V
		350mV ≤ V_{THD}	V_{THD}/2	1.2	2.0	V
I_{IN}	Input current	Power on or power off	—	—	+/-10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 ohms	—	1.38	1.60	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 ohms	0.9V	1.03	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 ohms	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} - V_{OM})/2, R_T = 100 ohms	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	V_{OD} = 0V Driver outputs shorted	—	—	6	mA

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

LVDS25E

The top and bottom side of LatticeXP devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

Figure 3-1. LVDS25E Output Termination Example

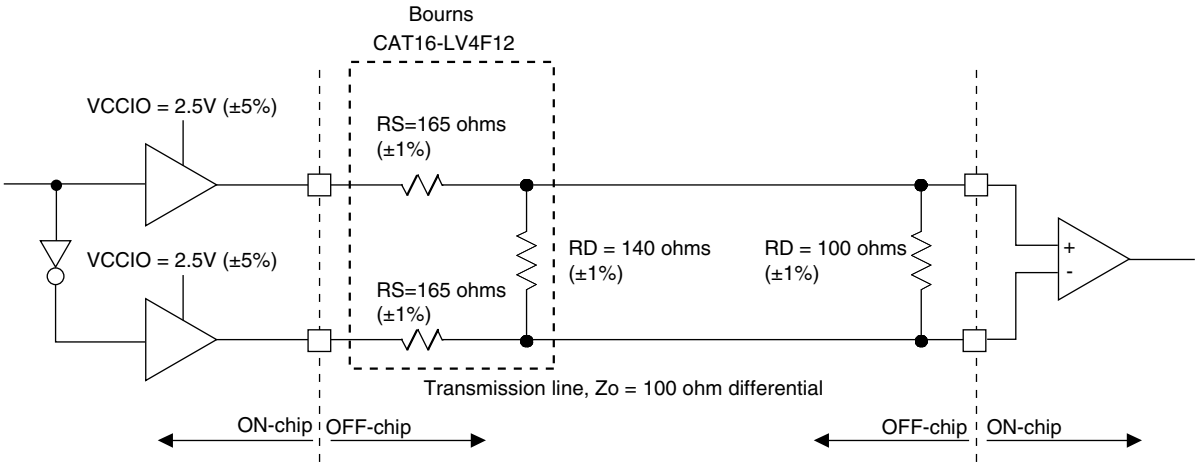


Table 3-1. LVDS25E DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100	ohms
I_{DC}	DC output current	3.66	mA

BLVDS

The LatticeXP devices support BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

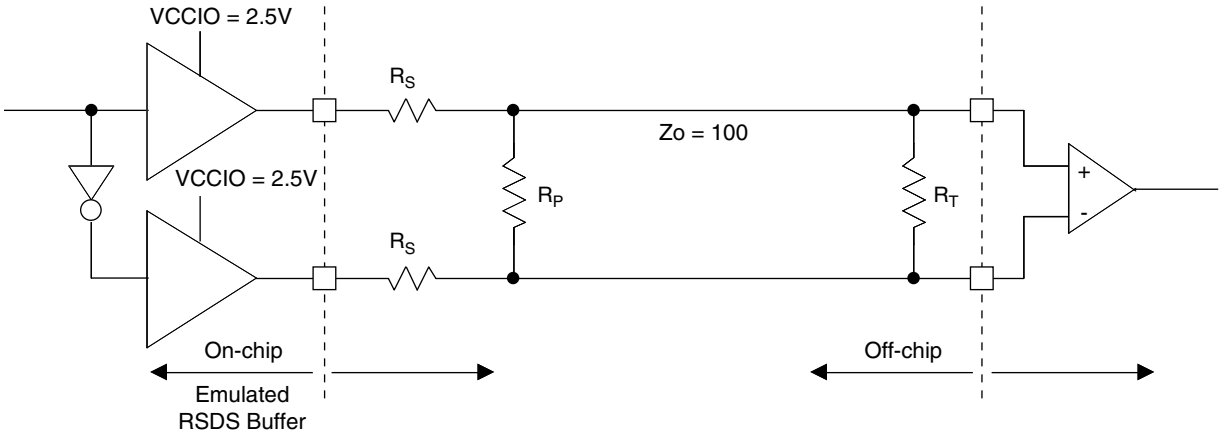


Table 3-4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	ohms
R_S	Driver series resistor	300	ohms
R_P	Driver parallel resistor	121	ohms
R_T	Receiver termination	100	ohms
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	ohms
I_{DC}	DC output current	3.66	mA

LatticeXP External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Device	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (Using Primary Clock without PLL)[1]									
t_{CO}	Clock to Output - PIO Output Register	LFXP3	—	5.12	—	6.12	—	7.43	ns
		LFXP6	—	5.30	—	6.34	—	7.69	ns
		LFXP10	—	5.52	—	6.60	—	8.00	ns
		LFXP15	—	5.72	—	6.84	—	8.29	ns
		LFXP20	—	5.97	—	7.14	—	8.65	ns
t_{SU}	Clock to Data Setup - PIO Input Register	LFXP3	-0.40	—	-0.28	—	-0.16	—	ns
		LFXP6	-0.33	—	-0.32	—	-0.30	—	ns
		LFXP10	-0.61	—	-0.71	—	-0.81	—	ns
		LFXP15	-0.71	—	-0.77	—	-0.87	—	ns
		LFXP20	-0.95	—	-1.14	—	-1.35	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	LFXP3	2.10	—	2.50	—	2.98	—	ns
		LFXP6	2.28	—	2.72	—	3.24	—	ns
		LFXP10	3.02	—	3.51	—	3.71	—	ns
		LFXP15	2.70	—	3.22	—	3.85	—	ns
		LFXP20	2.95	—	3.52	—	4.21	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Input Data Delay	LFXP3	2.38	—	2.49	—	2.66	—	ns
		LFXP6	2.92	—	3.18	—	3.42	—	ns
		LFXP10	2.72	—	2.75	—	2.84	—	ns
		LFXP15	2.99	—	3.13	—	3.18	—	ns
		LFXP20	4.47	—	4.56	—	4.80	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFXP3	-0.70	—	-0.80	—	-0.92	—	ns
		LFXP6	-0.47	—	-0.38	—	-0.31	—	ns
		LFXP10	-0.60	—	-0.47	—	-0.32	—	ns
		LFXP15	-1.05	—	-0.98	—	-1.01	—	ns
		LFXP20	-0.80	—	-0.58	—	-0.31	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All	—	400	—	360	—	320	MHz
DDR I/O Pin Parameters[2]									
t_{DVADQ}	Data Valid After DQS (DDR Read)	All	—	0.19	—	0.19	—	0.19	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	All	0.67	—	0.67	—	0.67	—	UI
t_{DQVBS}	Data Valid Before DQS	All	0.20	—	0.20	—	0.20	—	UI
t_{DQVAS}	Data Valid After DQS	All	0.20	—	0.20	—	0.20	—	UI
f_{MAX_DDR}	DDR Clock Frequency	All	95	166	95	133	95	100	MHz
Primary and Secondary Clocks									
f_{MAX_PRI}	Frequency for Primary Clock Tree	All	—	450	—	412	—	375	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All	1.19	—	1.19	—	1.19	—	ns
t_{SKEW_PRI}	Primary Clock Skew within an I/O Bank	LFXP3/6/10/15	—	250	—	300	—	350	ps
		LFXP20	—	300	—	350	—	400	ps

1. General timing numbers based on LVCMOS 2.5, 12mA.
2. DDR timing numbers based on SSTL I/O.

Timing v.F0.11

LatticeXP Internal Timing Parameters[1]

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t_{LUT4_PFU}	LUT4 Delay (A to D Inputs to F Output)	—	0.28	—	0.34	—	0.40	ns
t_{LUT6_PFU}	LUT6 Delay (A to D Inputs to OFX Output)	—	0.44	—	0.53	—	0.63	ns
t_{LSR_PFU}	Set/Reset to Output of PFU	—	0.90	—	1.08	—	1.29	ns
t_{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.13	—	0.15	—	0.19	—	ns
t_{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.04	—	-0.03	—	-0.03	—	ns
t_{SUD_PFU}	Clock to D Input Setup Time	0.13	—	0.16	—	0.19	—	ns
t_{HD_PFU}	Clock to D Input Hold Time	-0.03	—	-0.02	—	-0.02	—	ns
t_{CK2Q_PFU}	Clock to Q Delay, D-type Register Configuration	—	0.40	—	0.48	—	0.58	ns
t_{LE2Q_PFU}	Clock to Q Delay Latch Configuration	—	0.53	—	0.64	—	0.76	ns
t_{LD2Q_PFU}	D to Q Throughput Delay when Latch is Enabled	—	0.55	—	0.66	—	0.79	ns
PFU Dual Port Memory Mode Timing								
t_{CORAM_PFU}	Clock to Output	—	0.40	—	0.48	—	0.58	ns
t_{SUDATA_PFU}	Data Setup Time	-0.18	—	-0.14	—	-0.11	—	ns
t_{HDATA_PFU}	Data Hold Time	0.28	—	0.34	—	0.40	—	ns
t_{SUADDR_PFU}	Address Setup Time	-0.46	—	-0.37	—	-0.30	—	ns
t_{HADDR_PFU}	Address Hold Time	0.71	—	0.85	—	1.02	—	ns
t_{SUWREN_PFU}	Write/Read Enable Setup Time	-0.22	—	-0.17	—	-0.14	—	ns
t_{HWREN_PFU}	Write/Read Enable Hold Time	0.33	—	0.40	—	0.48	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t_{IN_PIO}	Input Buffer Delay	—	0.62	—	0.72	—	0.85	ns
t_{OUT_PIO}	Output Buffer Delay	—	2.12	—	2.54	—	3.05	ns
IOLOGIC Input/Output Timing								
t_{SUI_PIO}	Input Register Setup Time (Data Before Clock)	1.35	—	1.83	—	2.37	—	ns
t_{HI_PIO}	Input Register Hold Time (Data After Clock)	0.05	—	0.05	—	0.05	—	ns
t_{COO_PIO}	Output Register Clock to Output Delay	—	0.36	—	0.44	—	0.52	ns
t_{SUCE_PIO}	Input Register Clock Enable Setup Time	-0.09	—	-0.07	—	-0.06	—	ns
t_{HCE_PIO}	Input Register Clock Enable Hold Time	0.13	—	0.16	—	0.19	—	ns
t_{SULSR_PIO}	Set/Reset Setup Time	0.19	—	0.23	—	0.28	—	ns
t_{HLSR_PIO}	Set/Reset Hold Time	-0.14	—	-0.11	—	-0.09	—	ns
EBR Timing								
t_{CO_EBR}	Clock to Output from Address or Data	—	4.01	—	4.81	—	5.78	ns
t_{COO_EBR}	Clock to Output from EBR Output Register	—	0.81	—	0.97	—	1.17	ns
t_{SUDATA_EBR}	Setup Data to EBR Memory	-0.26	—	-0.21	—	-0.17	—	ns
t_{HDATA_EBR}	Hold Data to EBR Memory	0.41	—	0.49	—	0.59	—	ns
t_{SUADDR_EBR}	Setup Address to EBR Memory	-0.26	—	-0.21	—	-0.17	—	ns
t_{HADDR_EBR}	Hold Address to EBR Memory	0.41	—	0.49	—	0.59	—	ns
t_{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory	-0.17	—	-0.13	—	-0.11	—	ns
t_{HWREN_EBR}	Hold Write/Read Enable to EBR Memory	0.26	—	0.31	—	0.37	—	ns
t_{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.19	—	0.23	—	0.28	—	ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.13	—	-0.10	—	-0.08	—	ns

LFXP3 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	Pin Function	Bank	Differential	Dual Function
44	GNDIO4	4	-	-
45	PB15A	4	T	PCLKT4_0
46	PB15B	4	C	PCLKC4_0
47	VCCIO4	4	-	-
48	PB19A	4	T	DQS
49	PB19B	4	C	VREF1_4
50	PB24A	4	-	VREF2_4
51	PR18B	3	C[3]	-
52	GNDIO3	3	-	-
53	PR18A	3	T[3]	-
54	PR15B	3	-	VREF1_3
55	PR14A	3	-	VREF2_3
56	PR13B	3	C	-
57	PR13A	3	T	-
58	VCCIO3	3	-	-
59	GNDP1	-	-	-
60	VCCP1	-	-	-
61	PR9B	2	C	PCLKC2_0
62	PR9A	2	T	PCLKT2_0
63	PR8B	2	C	RUM0_PLLC_IN_A
64	PR8A	2	T	RUM0_PLLT_IN_A
65	VCCIO2	2	-	-
66	PR6B	2	-	VREF1_2
67	PR5A	2	-	VREF2_2
68	GNDIO2	2	-	-
69	PR3B	2	C	RUM0_PLLC_FB_A
70	PR3A	2	T	RUM0_PLLT_FB_A
71	VCCAUX	-	-	-
72	TDO	-	-	-
73	VCCJ	-	-	-
74	TDI	-	-	-
75	TMS	-	-	-
76	TCK	-	-	-
77	VCC	-	-	-
78	PT24A	1	-	-
79	PT23A	1	-	D0
80	PT22B	1	-	D1
81	PT21A	1	-	D2
82	VCCIO1	1	-	-
83	PT20B	1	-	D3
84	GNDIO1	1	-	-
85	PT17A	1	-	D4
86	PT16A	1	-	D5
87	PT15B	1	-	D6

LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
93	PR9A	2	T	PCLKT2_0	PR12A	2	T	PCLKT2_0
94	PR8B	2	C	RUM0_PLLC_IN_A	PR8B	2	C	RUM0_PLLC_IN_A
95	PR8A	2	T	RUM0_PLLT_IN_A	PR8A	2	T	RUM0_PLLT_IN_A
96	PR7B	2	C[3]	-	PR7B	2	C[3]	-
97	PR7A	2	T[3]	DQS	PR7A	2	T[3]	DQS
98	VCCIO2	2	-	-	VCCIO2	2	-	-
99	PR6B	2	-	VREF1_2	PR6B	2	-	VREF1_2
100	PR5A	2	-	VREF2_2	PR5A	2	-	VREF2_2
101	GNDIO2	2	-	-	GNDIO2	2	-	-
102	PR3B	2	C	RUM0_PLLC_FB_A	PR3B	2	C	RUM0_PLLC_FB_A
103	PR3A	2	T	RUM0_PLLT_FB_A	PR3A	2	T	RUM0_PLLT_FB_A
104	PR2B	2	C[3]	-	PR2B	2	C[3]	-
105	PR2A	2	T[3]	-	PR2A	2	T[3]	-
106	VCCAUX	-	-	-	VCCAUX	-	-	-
107	TDO	-	-	-	TDO	-	-	-
108	VCCJ	-	-	-	VCCJ	-	-	-
109	TDI	-	-	-	TDI	-	-	-
110	TMS	-	-	-	TMS	-	-	-
111	TCK	-	-	-	TCK	-	-	-
112	VCC	-	-	-	VCC	-	-	-
113	PT25A	1	-	VREF1_1	PT28A	1	-	VREF1_1
114	PT24A	1	-	-	PT27A	1	-	-
115	PT23A	1	-	D0	PT26A	1	-	D0
116	PT22B	1	C	D1	PT25B	1	C	D1
117	PT22A	1	T	VREF2_1	PT25A	1	T	VREF2_1
118	PT21A	1	-	D2	PT24A	1	-	D2
119	VCCIO1	1	-	-	VCCIO1	1	-	-
120	PT20B	1	-	D3	PT23B	1	-	D3
121	GNDIO1	1	-	-	GNDIO1	1	-	-
122	PT17A	1	-	D4	PT20A	1	-	D4
123	PT16A	1	-	D5	PT19A	1	-	D5
124	PT15B	1	C	D6	PT18B	1	C	D6
125	PT15A	1	T	-	PT18A	1	T	-
126	PT14B	1	-	D7	PT17B	1	-	D7
127	GND	-	-	-	GND	-	-	-
128	PT13B	0	C	BUSY	PT16B	0	C	BUSY
129	PT13A	0	T	CS1N	PT16A	0	T	CS1N
130	PT12B	0	C	PCLKC0_0	PT15B	0	C	PCLKC0_0
131	PT12A	0	T	PCLKT0_0	PT15A	0	T	PCLKT0_0
132	PT11B	0	C	-	PT14B	0	C	-
133	VCCIO0	0	-	-	VCCIO0	0	-	-
134	PT11A	0	T	DQS	PT14A	0	T	DQS
135	PT9A	0	-	DOUT	PT12A	0	-	DOUT
136	GNDIO0	0	-	-	GNDIO0	0	-	-
137	PT8A	0	-	WRITEN	PT11A	0	-	WRITEN
138	PT7A	0	-	VREF1_0	PT10A	0	-	VREF1_0

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
139	PR7A	2	T[3]	DQS	PR7A	2	T[3]	DQS
140	VCCIO2	2	-	-	VCCIO2	2	-	-
141	PR6B	2	-	VREF1_2	PR6B	2	-	VREF1_2
142	PR5A	2	-	VREF2_2	PR5A	2	-	VREF2_2
143	GNDIO2	2	-	-	GNDIO2	2	-	-
144	PR4B	2	C[3]	-	PR4B	2	C[3]	-
145	PR4A	2	T[3]	-	PR4A	2	T[3]	-
146	PR3B	2	C	RUM0_PLLC_FB_A	PR3B	2	C	RUM0_PLLC_FB_A
147	PR3A	2	T	RUM0_PLLT_FB_A	PR3A	2	T	RUM0_PLLT_FB_A
148	PR2B	2	C[3]	-	PR2B	2	C[3]	-
149	VCCIO2	2	-	-	VCCIO2	2	-	-
150	PR2A	2	T[3]	-	PR2A	2	T[3]	-
151	VCC	-	-	-	VCC	-	-	-
152	VCCAUX	-	-	-	VCCAUX	-	-	-
153	TDO	-	-	-	TDO	-	-	-
154	VCCJ	-	-	-	VCCJ	-	-	-
155	TDI	-	-	-	TDI	-	-	-
156	TMS	-	-	-	TMS	-	-	-
157	TCK	-	-	-	TCK	-	-	-
158	VCC	-	-	-	VCC	-	-	-
159	PT25A	1	-	VREF1_1	PT28A	1	-	VREF1_1
160	PT24B	1	C	-	PT27B	1	C	-
161	PT24A	1	T	-	PT27A	1	T	-
162	PT23A	1	-	D0	PT26A	1	-	D0
163	GNDIO1	1	-	-	GNDIO1	1	-	-
164	PT22B	1	C	D1	PT25B	1	C	D1
165	PT22A	1	T	VREF2_1	PT25A	1	T	VREF2_1
166	PT21A	1	-	D2	PT24A	1	-	D2
167	VCCIO1	1	-	-	VCCIO1	1	-	-
168	PT20B	1	C	D3	PT23B	1	C	D3
169	PT20A	1	T	-	PT23A	1	T	-
170	PT19B	1	C	-	PT22B	1	C	-
171	PT19A	1	T	DQS	PT22A	1	T	DQS
172	GNDIO1	1	-	-	GNDIO1	1	-	-
173	PT18B	1	-	-	PT21B	1	-	-
174	PT17A	1	-	D4	PT20A	1	-	D4
175	PT16B	1	C	-	PT19B	1	C	-
176	PT16A	1	T	D5	PT19A	1	T	D5
177	VCCIO1	1	-	-	VCCIO1	1	-	-
178	PT15B	1	C	D6	PT18B	1	C	D6
179	PT15A	1	T	-	PT18A	1	T	-
180	PT14B	1	-	D7	PT17B	1	-	D7
181	GND	-	-	-	GND	-	-	-
182	VCC	-	-	-	VCC	-	-	-
183	PT13B	0	C	BUSY	PT16B	0	C	BUSY
184	GNDIO0	0	-	-	GNDIO0	0	-	-

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
185	PT13A	0	T	CS1N	PT16A	0	T	CS1N
186	PT12B	0	C	PCLKC0_0	PT15B	0	C	PCLKC0_0
187	PT12A	0	T	PCLKT0_0	PT15A	0	T	PCLKT0_0
188	PT11B	0	C	-	PT14B	0	C	-
189	VCCIO0	0	-	-	VCCIO0	0	-	-
190	PT11A	0	T	DQS	PT14A	0	T	DQS
191	PT10B	0	-	-	PT13B	0	-	-
192	PT9A	0	-	DOUT	PT12A	0	-	DOUT
193	PT8B	0	C	-	PT11B	0	C	-
194	GNDIO0	0	-	-	GNDIO0	0	-	-
195	PT8A	0	T	WRITEN	PT11A	0	T	WRITEN
196	PT7B	0	C	-	PT10B	0	C	-
197	PT7A	0	T	VREF1_0	PT10A	0	T	VREF1_0
198	PT6B	0	C	-	PT9B	0	C	-
199	VCCIO0	0	-	-	VCCIO0	0	-	-
200	PT6A	0	T	DI	PT9A	0	T	DI
201	PT5B	0	C	-	PT8B	0	C	-
202	PT5A	0	T	CSN	PT8A	0	T	CSN
203	PT4B	0	C	-	PT7B	0	C	-
204	PT4A	0	T	-	PT7A	0	T	-
205	PT3B	0	-	VREF2_0	PT6B	0	-	VREF2_0
206	PT2B	0	-	-	PT5B	0	-	-
207	GND	-	-	-	GND	-	-	-
208	CFG0	0	-	-	CFG0	0	-	-

1. Applies to LFXP “C” only.
2. Applies to LFXP “E” only.
3. Supports dedicated LVDS outputs.

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
A9	PT27A	1	T	-	PT31A	1	T	-
C9	PT26B	1	C	D7	PT30B	1	C	D7
C8	PT26A	1	T	-	PT30A	1	T	-
E9	PT25B	0	C	BUSY	PT29B	0	C	BUSY
-	GNDIO0	0	-	-	GNDIO0	0	-	-
B8	PT25A	0	T	CS1N	PT29A	0	T	CS1N
A8	PT24B	0	C	PCLKC0_0	PT28B	0	C	PCLKC0_0
A7	PT24A	0	T	PCLKT0_0	PT28A	0	T	PCLKT0_0
B7	PT23B	0	C	-	PT27B	0	C	-
C7	PT23A	0	T	DQS	PT27A	0	T	DQS
E8	PT22B	0	-	-	PT26B	0	-	-
D8	PT21A	0	-	DOUT	PT25A	0	-	DOUT
A6	PT20B	0	C	-	PT24B	0	C	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
C6	PT20A	0	T	WRITEN	PT24A	0	T	WRITEN
E7	PT19B	0	C	-	PT23B	0	C	-
D7	PT19A	0	T	VREF1_0	PT23A	0	T	VREF1_0
A5	PT18B	0	C	-	PT22B	0	C	-
B5	PT18A	0	T	DI	PT22A	0	T	DI
A4	PT17B	0	C	-	PT21B	0	C	-
B6	PT17A	0	T	CSN	PT21A	0	T	CSN
E6	PT16B	0	C	-	PT20B	0	C	-
D6	PT16A	0	T	-	PT20A	0	T	-
D5	PT15B	0	C	VREF2_0	PT19B	0	C	VREF2_0
A3	PT15A	0	T	DQS	PT19A	0	T	DQS
B3	PT14B	0	-	-	PT18B	0	-	-
B2	PT13A	0	-	-	PT17A	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
A2	PT12B	0	C	-	PT16B	0	C	-
B1	PT12A	0	T	-	PT16A	0	T	-
F5	PT11B	0	C	-	PT15B	0	C	-
C5	PT11A	0	T	-	PT15A	0	T	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
C4	CFG0	0	-	-	CFG0	0	-	-
B4	CFG1	0	-	-	CFG1	0	-	-
C3	DONE	0	-	-	DONE	0	-	-
A1	GND	-	-	-	GND	-	-	-
A16	GND	-	-	-	GND	-	-	-
F11	GND	-	-	-	GND	-	-	-
F6	GND	-	-	-	GND	-	-	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
F4	PROGRAMN	7	-	-	PROGRAMN	7	-	-	PROGRAMN	7	-	-
G4	CCLK	7	-	-	CCLK	7	-	-	CCLK	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
D2	PL2A	7	T[3]	-	PL6A	7	T[3]	-	PL6A	7	T[3]	-
D1	PL2B	7	C[3]	-	PL6B	7	C[3]	-	PL6B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
E2	PL3A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A
E3	PL3B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A
F3	PL4A	7	T[3]	-	PL8A	7	T[3]	-	PL8A	7	T[3]	-
F2	PL4B	7	C[3]	-	PL8B	7	C[3]	-	PL8B	7	C[3]	-
H4	PL5A	7	-	-	PL9A	7	-	-	PL9A	7	-	-
H3	PL6B	7	-	VREF1_7	PL10B	7	-	VREF1_7	PL10B	7	-	VREF1_7
G3	PL7A	7	T[3]	DQS	PL11A	7	T[3]	DQS	PL11A	7	T[3]	DQS
G2	PL7B	7	C[3]	-	PL11B	7	C[3]	-	PL11B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
F1	PL8A	7	T	-	PL12A	7	T	-	PL12A	7	T	-
E1	PL8B	7	C	-	PL12B	7	C	-	PL12B	7	C	-
J4	PL9A	7	T[3]	-	PL13A	7	T[3]	-	PL13A	7	T[3]	-
K4	PL9B	7	C[3]	-	PL13B	7	C[3]	-	PL13B	7	C[3]	-
G1	PL11A	7	T[3]	-	PL15A	7	T[3]	-	PL15A	7	T[3]	-
H2	PL11B	7	C[3]	-	PL15B	7	C[3]	-	PL15B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
J2	PL12A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A
H1	PL12B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A
J1	PL13A	7	T[3]	-	PL17A	7	T[3]	-	PL17A	7	T[3]	-
K2	PL13B	7	C[3]	-	PL17B	7	C[3]	-	PL17B	7	C[3]	-
K3	PL14A	7	-	VREF2_7	PL18A	7	-	VREF2_7	PL18A	7	-	VREF2_7
J3	PL15B	7	-	-	PL19B	7	-	-	PL19B	7	-	-
K1	PL16A	7	T[3]	DQS	PL20A	7	T[3]	DQS	PL20A	7	T[3]	DQS
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
L2	PL16B	7	C[3]	-	PL20B	7	C[3]	-	PL20B	7	C[3]	-
L3	PL17A	7	T	-	PL21A	7	T	-	PL21A	7	T	-
L4	PL17B	7	C	-	PL21B	7	C	-	PL21B	7	C	-
L1	PL18A	7	T[3]	-	PL22A	7	T[3]	-	PL22A	7	T[3]	-
M1	PL18B	7	C[3]	-	PL22B	7	C[3]	-	PL22B	7	C[3]	-
M2	VCCP0	-	-	-	VCCP0	-	-	-	VCCP0	-	-	-
N1	GNDP0	-	-	-	GNDP0	-	-	-	GNDP0	-	-	-
M3	PL19A	6	T[3]	-	PL23A	6	T[3]	-	PL27A	6	T[3]	-
M4	PL19B	6	C[3]	-	PL23B	6	C[3]	-	PL27B	6	C[3]	-
P1	PL20A	6	T	PCLKT6_0	PL24A	6	T	PCLKT6_0	PL28A	6	T	PCLKT6_0
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
N2	PL20B	6	C	PCLKC6_0	PL24B	6	C	PCLKC6_0	PL28B	6	C	PCLKC6_0
R1	PL21A	6	T[3]	-	PL25A	6	T[3]	-	PL29A	6	T[3]	-
P2	PL21B	6	C[3]	-	PL25B	6	C[3]	-	PL29B	6	C[3]	-
N3	PL22A	6	-	-	PL26A	6	-	-	PL30A	6	-	-
N4	PL23B	6	-	VREF1_6	PL27B	6	-	VREF1_6	PL31B	6	-	VREF1_6
T1	PL24A	6	T[3]	DQS	PL28A	6	T[3]	DQS	PL32A	6	T[3]	DQS
R2	PL24B	6	C[3]	-	PL28B	6	C[3]	-	PL32B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
C20	PT38A	1	T	-	PT43A	1	T	-	PT47A	1	T	-
C21	PT37B	1	C	-	PT42B	1	C	-	PT46B	1	C	-
C22	PT37A	1	T	-	PT42A	1	T	-	PT46A	1	T	-
B22	PT36B	1	C	-	PT41B	1	C	-	PT45B	1	C	-
A21	PT36A	1	T	-	PT41A	1	T	-	PT45A	1	T	-
D15	PT35B	1	C	-	PT40B	1	C	-	PT44B	1	C	-
D14	PT35A	1	T	-	PT40A	1	T	-	PT44A	1	T	-
B21	PT34B	1	C	VREF1_1	PT39B	1	C	VREF1_1	PT43B	1	C	VREF1_1
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
A20	PT34A	1	T	DQS	PT39A	1	T	DQS	PT43A	1	T	DQS
B20	PT33B	1	-	-	PT38B	1	-	-	PT42B	1	-	-
A19	PT32A	1	-	-	PT37A	1	-	-	PT41A	1	-	-
B19	PT31B	1	C	-	PT36B	1	C	-	PT40B	1	C	-
A18	PT31A	1	T	-	PT36A	1	T	-	PT40A	1	T	-
C14	PT30B	1	C	-	PT35B	1	C	-	PT39B	1	C	-
C13	PT30A	1	T	D0	PT35A	1	T	D0	PT39A	1	T	D0
B18	PT29B	1	C	D1	PT34B	1	C	D1	PT38B	1	C	D1
A17	PT29A	1	T	VREF2_1	PT34A	1	T	VREF2_1	PT38A	1	T	VREF2_1
B17	PT28B	1	C	-	PT33B	1	C	-	PT37B	1	C	-
A16	PT28A	1	T	D2	PT33A	1	T	D2	PT37A	1	T	D2
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
B16	PT27B	1	C	D3	PT32B	1	C	D3	PT36B	1	C	D3
A15	PT27A	1	T	-	PT32A	1	T	-	PT36A	1	T	-
B15	PT26B	1	C	-	PT31B	1	C	-	PT35B	1	C	-
A14	PT26A	1	T	DQS	PT31A	1	T	DQS	PT35A	1	T	DQS
D13	PT25B	1	-	-	PT30B	1	-	-	PT34B	1	-	-
D12	PT24A	1	-	D4	PT29A	1	-	D4	PT33A	1	-	D4
B14	PT23B	1	C	-	PT28B	1	C	-	PT32B	1	C	-
A13	PT23A	1	T	D5	PT28A	1	T	D5	PT32A	1	T	D5
-	GNDIO1	1	-	-	GNDIO1	1	-	-	GNDIO1	1	-	-
B13	PT22B	1	C	D6	PT27B	1	C	D6	PT31B	1	C	D6
A12	PT22A	1	T	-	PT27A	1	T	-	PT31A	1	T	-
B12	PT21B	1	C	D7	PT26B	1	C	D7	PT30B	1	C	D7
C12	PT21A	1	T	-	PT26A	1	T	-	PT30A	1	T	-
C11	PT20B	0	C	BUSY	PT25B	0	C	BUSY	PT29B	0	C	BUSY
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
B11	PT20A	0	T	CS1N	PT25A	0	T	CS1N	PT29A	0	T	CS1N
A11	PT19B	0	C	PCLKC0_0	PT24B	0	C	PCLKC0_0	PT28B	0	C	PCLKC0_0
A10	PT19A	0	T	PCLKT0_0	PT24A	0	T	PCLKT0_0	PT28A	0	T	PCLKT0_0
B10	PT18B	0	C	-	PT23B	0	C	-	PT27B	0	C	-
B9	PT18A	0	T	DQS	PT23A	0	T	DQS	PT27A	0	T	DQS
D11	PT17B	0	-	-	PT22B	0	-	-	PT26B	0	-	-
D10	PT16A	0	-	DOUT	PT21A	0	-	DOUT	PT25A	0	-	DOUT
A9	PT15B	0	C	-	PT20B	0	C	-	PT24B	0	C	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-	GNDIO0	0	-	-
C8	PT15A	0	T	WRITEN	PT20A	0	T	WRITEN	PT24A	0	T	WRITEN
B8	PT14B	0	C	-	PT19B	0	C	-	PT23B	0	C	-
A8	PT14A	0	T	VREF1_0	PT19A	0	T	VREF1_0	PT23A	0	T	VREF1_0
C7	PT13B	0	C	-	PT18B	0	C	-	PT22B	0	C	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
AB19	PB37A	4	-	-	PB41A	4	-	-
AB20	PB38B	4	-	-	PB42B	4	-	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
V15	PB39A	4	T	DQS	PB43A	4	T	DQS
U15	PB39B	4	C	-	PB43B	4	C	-
Y15	PB40A	4	T	-	PB44A	4	T	-
W15	PB40B	4	C	-	PB44B	4	C	-
AA16	PB41A	4	T	-	PB45A	4	T	-
AA17	PB41B	4	C	-	PB45B	4	C	-
AA18	PB42A	4	T	-	PB46A	4	T	-
AA19	PB42B	4	C	-	PB46B	4	C	-
Y16	PB43A	4	T	-	PB47A	4	T	-
W16	PB43B	4	C	-	PB47B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
AA20	PB44A	4	T	-	PB48A	4	T	-
AA21	PB44B	4	C	-	PB48B	4	C	-
Y17	PB45A	4	-	-	PB49A	4	-	-
Y18	PB46B	4	-	-	PB50B	4	-	-
Y19	PB47A	4	T	DQS	PB51A	4	T	DQS
Y20	PB47B	4	C	-	PB51B	4	C	-
V16	PB48A	4	T	-	PB52A	4	T	-
U16	PB48B	4	C	-	PB52B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
U18	-	-	-	-	PB53A	4	T	-
V18	-	-	-	-	PB53B	4	C	-
W19	-	-	-	-	PB54A	4	T	-
W18	-	-	-	-	PB54B	4	C	-
U17	-	-	-	-	PB55A	4	T	-
V17	-	-	-	-	PB55B	4	C	-
-	GNDIO4	4	-	-	GNDIO4	4	-	-
W17	-	-	-	-	PB56A	4	-	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
V19	PR43A	3	-	-	PR47A	3	-	-
U20	PR42B	3	C[3]	-	PR46B	3	C[3]	-
U19	PR42A	3	T[3]	-	PR46A	3	T[3]	-
V20	PR41B	3	C	-	PR45B	3	C	-
W20	PR41A	3	T	-	PR45A	3	T	-
T17	PR40B	3	C[3]	-	PR44B	3	C[3]	-
T18	PR40A	3	T[3]	-	PR44A	3	T[3]	-
T19	PR39B	3	C[3]	-	PR43B	3	C[3]	-
T20	PR39A	3	T[3]	-	PR43A	3	T[3]	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-