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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6000
Total RAM Bits	73728
Number of I/O	100
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp6e-3t144i

Table 2-6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

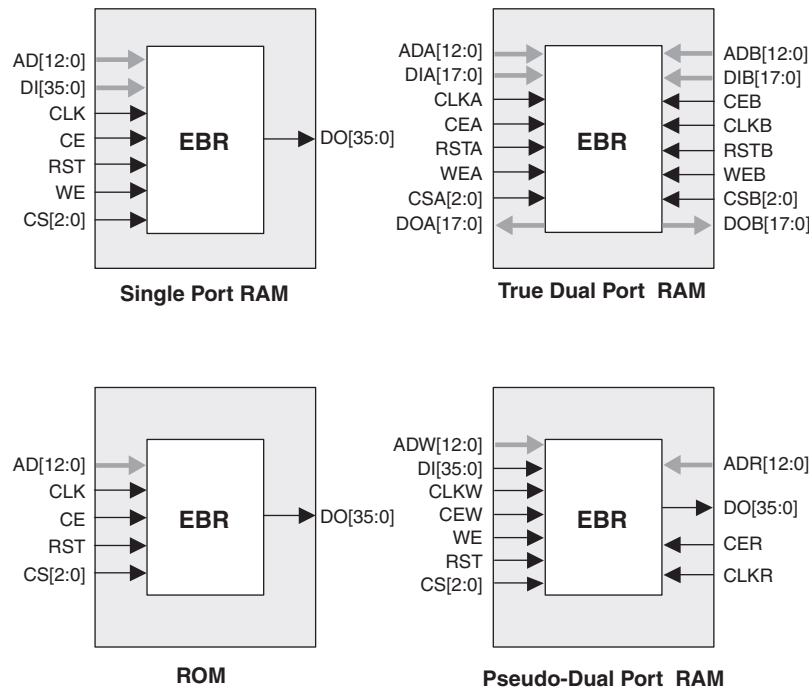
If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

Figure 2-14 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

Figure 2-14. sysMEM Memory Primitives

The EBR memory supports three forms of write behavior for single port or dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – a copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-15.

in selected blocks the input to the DQS delay block. If one of the bypass options is not chosen, the signal first passes through an optional delay block. This delay, if selected, ensures no positive input-register hold-time requirement when using a global clock.

The input block allows two modes of operation. In the single data rate (SDR) the data is registered, by one of the registers in the single data rate sync register block, with the system clock. In the DDR Mode two registers are used to sample the data on the positive and negative edges of the DQS signal creating two data streams, D0 and D2. These two data streams are synchronized with the system clock before entering the core. Further discussion on this topic is in the DDR Memory section of this data sheet.

Figure 2-21 shows the input register waveforms for DDR operation and Figure 2-22 shows the design tool primitives. The SDR/SYNC registers have reset and clock enable available.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to the system clock domain. For further discussion of this topic, see the DDR memory section of this data sheet.

Figure 2-20. Input Register Diagram

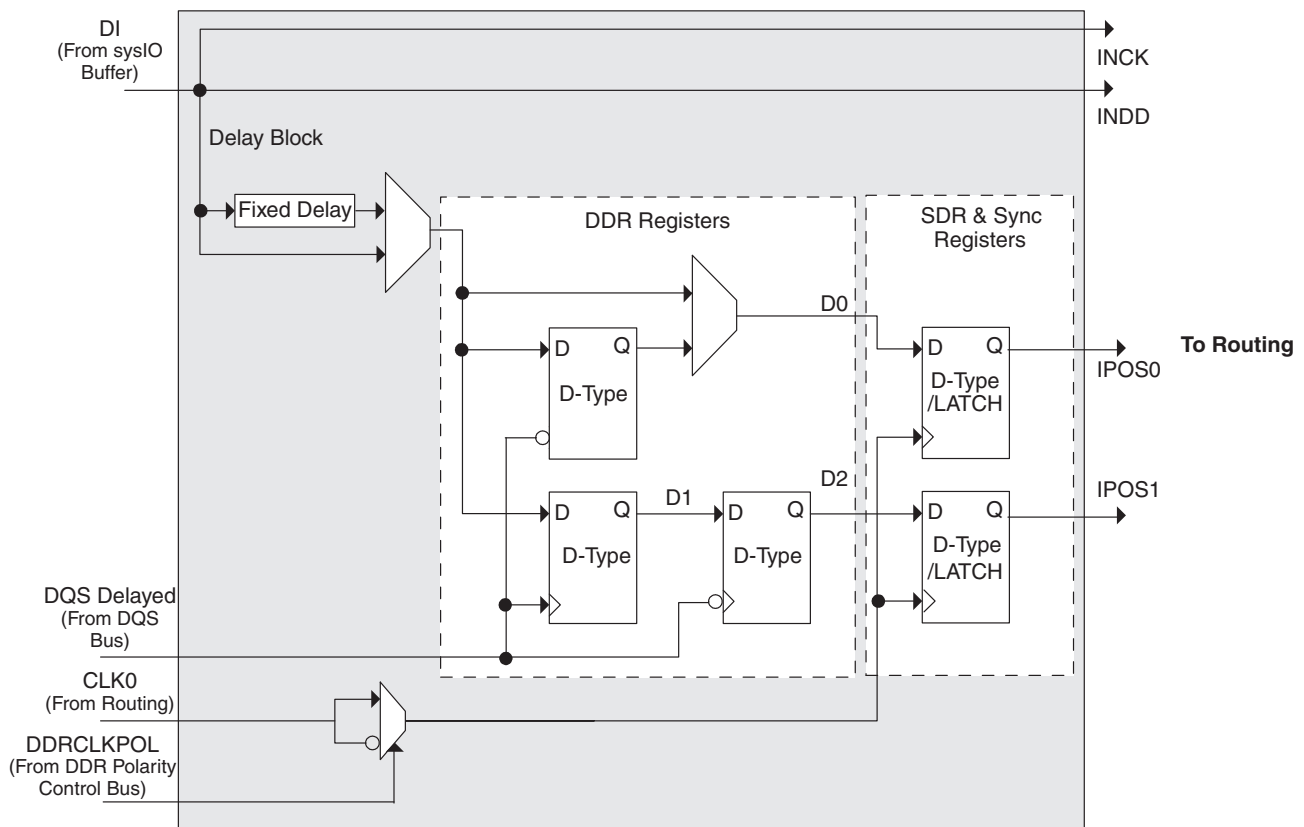


Table 2-8. Supported Output Standards

Output Standard	Drive	V _{CCIO} (Nom.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVC MOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVC MOS25	4mA, 8mA, 12mA 16mA, 20mA	2.5
LVC MOS18	4mA, 8mA, 12mA 16mA	1.8
LVC MOS15	4mA, 8mA	1.5
LVC MOS12	2mA, 6mA	1.2
LVC MOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVC MOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVC MOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVC MOS15, Open Drain	4mA, 8mA	—
LVC MOS12, Open Drain	2mA, 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II, III	N/A	1.8
HSTL15 Class I, III	N/A	1.5
SSTL3 Class I, II	N/A	3.3
SSTL2 Class I, II	N/A	2.5
SSTL18 Class I	N/A	1.8
Differential Interfaces		
Differential SSTL3, Class I, II	N/A	3.3
Differential SSTL2, Class I, II	N/A	2.5
Differential SSTL18, Class I	N/A	1.8
Differential HSTL18, Class I, II, III	N/A	1.8
Differential HSTL15, Class I, III	N/A	1.5
LVDS	N/A	2.5
BLVDS ¹	N/A	2.5
LVPECL ¹	N/A	3.3

1. Emulated with external resistors.

Hot Socketing

The LatticeXP devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits, which allows easy integration with the rest of the system. These capabilities make the LatticeXP ideal for many multiple power supply and hot-swap applications.

Sleep Mode

The LatticeXP “C” devices (V_{CC} = 1.8/2.5/3.3V) have a sleep mode that allows standby current to be reduced by up to three orders of magnitude during periods of system inactivity. Entry and exit to Sleep Mode is controlled by the SLEEPN pin.

During Sleep Mode, the FPGA logic is non-operational, registers and EBR contents are not maintained and I/Os are tri-stated. Do not enter Sleep Mode during device programming or configuration operation. In Sleep Mode, power supplies can be maintained in their normal operating range, eliminating the need for external switching of power supplies. Table 2-9 compares the characteristics of Normal, Off and Sleep Modes.

master serial clock is 2.5MHz. Table 2-10 lists all the available Master Serial Clock frequencies. When a different Master Serial Clock is selected during the design process, the following sequence takes place:

1. User selects a different Master Serial Clock frequency for configuration.
2. During configuration the device starts with the default (2.5MHz) Master Serial Clock frequency.
3. The clock configuration settings are contained in the early configuration bit stream.
4. The Master Serial Clock frequency changes to the selected frequency once the clock configuration bits are received.

For further information on the use of this oscillator for configuration, please see details of additional technical documentation at the end of this data sheet.

Table 2-10. Selectable Master Serial Clock (CCLK) Frequencies During Configuration

CCLK (MHz)	CCLK (MHz)	CCLK (MHz)
2.5 ¹	13	45
4.3	15	51
5.4	20	55
6.9	26	60
8.1	30	130
9.2	34	—
10.0	41	—

1. Default

Density Shifting

The LatticeXP family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

Initialization Supply Current^{1, 2, 3, 4, 5, 6}**Over Recommended Operating Conditions**

Symbol	Parameter	Device	Typ. ⁷	Units
I_{CC}	Core Power Supply	LFXP3E	40	mA
		LFXP6E	50	mA
		LFXP10E	110	mA
		LFXP15E	140	mA
		LFXP20E	250	mA
		LFXP3C	60	mA
		LFXP6C	70	mA
		LFXP10C	150	mA
		LFXP15C	180	mA
		LFXP20C	290	mA
I_{CCAUX}	Auxiliary Power Supply $V_{CCAUX} = 3.3V$	LFXP3E/C	50	mA
		LFXP6E/C	60	mA
		LFXP10E/C	90	mA
		LFXP15 /C	110	mA
		LFXP20E/C	130	mA
I_{CCJ}	V_{CCJ} Power Supply	All	2	mA

1. Until DONE signal is active.

2. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.

3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

4. Frequency 0MHz.

5. Typical user pattern.

6. Assume normal bypass capacitor/decoupling capacitor across the supply.

7. $T_A=25^{\circ}C$, power supplies at nominal voltage.

LatticeXP Family Timing Adders¹

Over Recommended Operating Conditions

Buffer Type	Description	-5	-4	-3	Units
Input Adjusters					
LVDS25E	LVDS 2.5 Emulated	0.5	0.5	0.5	ns
LVDS25	LVDS	0.4	0.4	0.4	ns
BLVDS25	BLVDS	0.5	0.5	0.5	ns
LVPECL33	LVPECL	0.6	0.6	0.6	ns
HSTL18_I	HSTL_18 class I	0.4	0.4	0.4	ns
HSTL18_II	HSTL_18 class II	0.4	0.4	0.4	ns
HSTL18_III	HSTL_18 class III	0.4	0.4	0.4	ns
HSTL18D_I	Differential HSTL 18 class I	0.4	0.4	0.4	ns
HSTL18D_II	Differential HSTL 18 class II	0.4	0.4	0.4	ns
HSTL18D_III	Differential HSTL 18 class III	0.4	0.4	0.4	ns
HSTL15_I	HSTL_15 class I	0.5	0.5	0.5	ns
HSTL15_III	HSTL_15 class III	0.5	0.5	0.5	ns
HSTL15D_I	Differential HSTL 15 class I	0.5	0.5	0.5	ns
HSTL15D_III	Differential HSTL 15 class III	0.5	0.5	0.5	ns
SSTL33_I	SSTL_3 class I	0.6	0.6	0.6	ns
SSTL33_II	SSTL_3 class II	0.6	0.6	0.6	ns
SSTL33D_I	Differential SSTL_3 class I	0.6	0.6	0.6	ns
SSTL33D_II	Differential SSTL_3 class II	0.6	0.6	0.6	ns
SSTL25_I	SSTL_2 class I	0.5	0.5	0.5	ns
SSTL25_II	SSTL_2 class II	0.5	0.5	0.5	ns
SSTL25D_I	Differential SSTL_2 class I	0.5	0.5	0.5	ns
SSTL25D_II	Differential SSTL_2 class II	0.5	0.5	0.5	ns
SSTL18_I	SSTL_18 class I	0.5	0.5	0.5	ns
SSTL18D_I	Differential SSTL_18 class I	0.5	0.5	0.5	ns
LVTTTL33	LVTTTL	0.2	0.2	0.2	ns
LVC MOS33	LVC MOS 3.3	0.2	0.2	0.2	ns
LVC MOS25	LVC MOS 2.5	0.0	0.0	0.0	ns
LVC MOS18	LVC MOS 1.8	0.1	0.1	0.1	ns
LVC MOS15	LVC MOS 1.5	0.1	0.1	0.1	ns
LVC MOS12	LVC MOS 1.2	0.1	0.1	0.1	ns
PCI33	PCI	0.2	0.2	0.2	ns
Output Adjusters					
LVDS25E	LVDS 2.5 Emulated	0.3	0.3	0.3	ns
LVDS25	LVDS 2.5	0.3	0.3	0.3	ns
BLVDS25	BLVDS 2.5	0.3	0.3	0.3	ns
LVPECL33	LVPECL 3.3	0.1	0.1	0.1	ns
HSTL18_I	HSTL_18 class I	0.1	0.1	0.1	ns
HSTL18_II	HSTL_18 class II	0.1	0.1	0.1	ns
HSTL18_III	HSTL_18 class III	0.2	0.2	0.2	ns
HSTL18D_I	Differential HSTL 18 class I	0.1	0.1	0.1	ns
HSTL18D_II	Differential HSTL 18 class II	-0.1	-0.1	-0.1	ns
HSTL18D_III	Differential HSTL 18 class III	0.2	0.2	0.2	ns

LatticeXP Family Timing Adders¹ (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	-5	-4	-3	Units
HSTL15_I	HSTL_15 class I	0.2	0.2	0.2	ns
HSTL15_III	HSTL_15 class III	0.2	0.2	0.2	ns
HSTL15D_I	Differential HSTL 15 class I	0.2	0.2	0.2	ns
HSTL15D_III	Differential HSTL 15 class III	0.2	0.2	0.2	ns
SSTL33_I	SSTL_3 class I	0.1	0.1	0.1	ns
SSTL33_II	SSTL_3 class II	0.3	0.3	0.3	ns
SSTL33D_I	Differential SSTL_3 class I	0.1	0.1	0.1	ns
SSTL33D_II	Differential SSTL_3 class II	0.3	0.3	0.3	ns
SSTL25_I	SSTL_2 class I	-0.1	-0.1	-0.1	ns
SSTL25_II	SSTL_2 class II	0.3	0.3	0.3	ns
SSTL25D_I	Differential SSTL_2 class I	-0.1	-0.1	-0.1	ns
SSTL25D_II	Differential SSTL_2 class II	0.3	0.3	0.3	ns
SSTL18_I	SSTL_1.8 class I	0.1	0.1	0.1	ns
SSTL18D_I	Differential SSTL_1.8 class I	0.1	0.1	0.1	ns
LVTTTL33_4mA	LVTTTL 4mA drive	0.8	0.8	0.8	ns
LVTTTL33_8mA	LVTTTL 8mA drive	0.5	0.5	0.5	ns
LVTTTL33_12mA	LVTTTL 12mA drive	0.3	0.3	0.3	ns
LVTTTL33_16mA	LVTTTL 16mA drive	0.4	0.4	0.4	ns
LVTTTL33_20mA	LVTTTL 20mA drive	0.3	0.3	0.3	ns
LVC MOS33_2mA	LVC MOS 3.3 2mA drive	0.8	0.8	0.8	ns
LVC MOS33_4mA	LVC MOS 3.3 4mA drive	0.8	0.8	0.8	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive	0.5	0.5	0.5	ns
LVC MOS33_12mA	LVC MOS 3.3 12mA drive	0.3	0.3	0.3	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive	0.4	0.4	0.4	ns
LVC MOS33_20mA	LVC MOS 3.3 20mA drive	0.3	0.3	0.3	ns
LVC MOS25_2mA	LVC MOS 2.5 2mA drive	0.7	0.7	0.7	ns
LVC MOS25_4mA	LVC MOS 2.5 4mA drive	0.7	0.7	0.7	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive	0.4	0.4	0.4	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive	0.0	0.0	0.0	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive	0.2	0.2	0.2	ns
LVC MOS25_20mA	LVC MOS 2.5 20mA drive	0.4	0.4	0.4	ns
LVC MOS18_2mA	LVC MOS 1.8 2mA drive	0.6	0.6	0.6	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive	0.6	0.6	0.6	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive	0.4	0.4	0.4	ns
LVC MOS18_12mA	LVC MOS 1.8 12mA drive	0.2	0.2	0.2	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive	0.2	0.2	0.2	ns
LVC MOS15_2mA	LVC MOS 1.5 2mA drive	0.6	0.6	0.6	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive	0.6	0.6	0.6	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive	0.2	0.2	0.2	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive	0.4	0.4	0.4	ns
LVC MOS12_6mA	LVC MOS 1.2 6mA drive	0.4	0.4	0.4	ns
PCI33	PCI33	0.3	0.3	0.3	ns

1. General timing numbers based on LVC MOS 2.5, 12mA.
Timing v.F0.11

Flash Download Time

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{REFRESH}	PROGRAMN Low-to-High. Transition to Done High.	—	1.1	1.7	ms
	LFXP3	—	1.1	1.7	ms
	LFXP6	—	1.4	2.0	ms
	LFXP10	—	0.9	1.5	ms
	LFXP15	—	1.1	1.7	ms
	LFXP20	—	1.3	1.9	ms

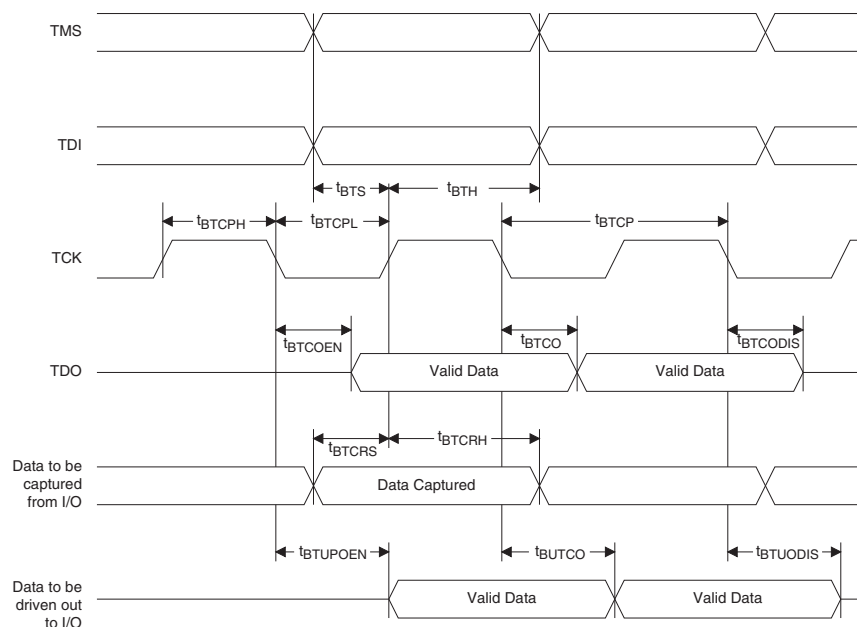
JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f_{MAX}		—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t_{BTCODIS}	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
t_{BTUODIS}	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
t_{BTUPOEN}	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Timing v.F0.11

Figure 3-12. JTAG Port Timing Waveforms



Pin Information Summary¹

Pin Type		XP3			XP6		
		100 TQFP	144 TQFP	208 PQFP	144 TQFP	208 PQFP	256 fpBGA
Single Ended User I/O		62	100	136	100	142	188
Differential Pair User I/O ²		19	35	56	35	58	80
Configuration	Dedicated	11	11	11	11	11	11
	Muxed	14	14	14	14	14	14
TAP		5	5	5	5	5	5
Dedicated (total without supplies)		6	6	6	6	6	6
V _{CC}		2	4	8	4	8	8
V _{CCAUX}		2	2	2	2	2	4
V _{CCPLL}		2	2	2	2	2	2
V _{CCIO}	Bank0	1	1	2	1	2	2
	Bank1	1	1	2	1	2	2
	Bank2	1	1	2	1	2	2
	Bank3	1	1	2	1	2	2
	Bank4	1	2	2	2	2	2
	Bank5	1	1	2	1	2	2
	Bank6	1	1	2	1	2	2
	Bank7	1	1	2	1	2	2
GND		10	13	24	13	24	24
GND _{PLL}		2	2	2	2	2	2
NC		0	0	6	0	0	0
Single Ended/Differential I/O per Bank ²	Bank0	8/2	12/3	20/8	12/3	20/8	26/11
	Bank1	9/0	12/2	18/6	12/2	18/6	26/11
	Bank2	8/3	12/5	14/6	12/5	17/7	21/9
	Bank3	6/2	13/5	14/6	13/5	14/6	21/9
	Bank4	5/2	14/6	21/9	14/6	21/9	26/11
	Bank5	12/4	12/4	21/9	12/4	21/9	26/11
	Bank6	4/2	13/5	14/6	13/5	17/7	21/9
	Bank7	10/4	12/5	14/6	12/5	14/6	21/9
V _{CCJ}		1	1	1	1	1	1

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.

2. The differential I/O per bank includes both dedicated LVDS and emulated LVDS pin pairs. Please see the Logic Signal Connections table for more information.

LFXP3 Logic Signal Connections: 100 TQFP

Pin Number	Pin Function	Bank	Differential	Dual Function
1	CFG1	0	-	-
2	DONE	0	-	-
3	PROGRAMN	7	-	-
4	CCLK	7	-	-
5	PL3A	7	T	LUM0_PLLT_FB_A
6	PL3B	7	C	LUM0_PLLC_FB_A
7	VCCIO7	7	-	-
8	PL5A	7	-	VREF1_7
9	PL6B	7	-	VREF2_7
10	GNDIO7	7	-	-
11	PL7A	7	T ³	DQS
12	PL7B	7	C ³	-
13	PL8A	7	T	LUM0_PLLT_IN_A
14	PL8B	7	C	LUM0_PLLC_IN_A
15	PL9A	7	T ³	-
16	PL9B	7	C ³	-
17	VCCP0	-	-	-
18	GNDP0	-	-	-
19	PL12A	6	T	PCLKT6_0
20	PL12B	6	C	PCLKC6_0
21	GNDIO6	6	-	-
22	VCCIO6	6	-	-
23	PL18A	6	T ³	-
24	PL18B	6	C ³	-
25	VCCAUX	-	-	-
26	SLEEPN ¹ /TOE ²	-	-	-
27	INITN	5	-	-
28	VCC	-	-	-
29	PB2B	5	-	VREF1_5
30	PB5B	5	-	VREF2_5
31	PB8A	5	T	-
32	PB8B	5	C	-
33	GNDIO5	5	-	-
34	PB9A	5	-	-
35	PB10B	5	-	-
36	PB11A	5	T	DQS
37	PB11B	5	C	-
38	VCCIO5	5	-	-
39	PB12A	5	T	-
40	PB12B	5	C	-
41	PB13A	5	T	-
42	PB13B	5	C	-
43	GND	-	-	-

LFXP3 Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	Pin Function	Bank	Differential	Dual Function
44	GNDIO4	4	-	-
45	PB15A	4	T	PCLKT4_0
46	PB15B	4	C	PCLKC4_0
47	VCCIO4	4	-	-
48	PB19A	4	T	DQS
49	PB19B	4	C	VREF1_4
50	PB24A	4	-	VREF2_4
51	PR18B	3	C ³	-
52	GNDIO3	3	-	-
53	PR18A	3	T ³	-
54	PR15B	3	-	VREF1_3
55	PR14A	3	-	VREF2_3
56	PR13B	3	C	-
57	PR13A	3	T	-
58	VCCIO3	3	-	-
59	GNDP1	-	-	-
60	VCCP1	-	-	-
61	PR9B	2	C	PCLKC2_0
62	PR9A	2	T	PCLKT2_0
63	PR8B	2	C	RUM0_PLLC_IN_A
64	PR8A	2	T	RUM0_PLLT_IN_A
65	VCCIO2	2	-	-
66	PR6B	2	-	VREF1_2
67	PR5A	2	-	VREF2_2
68	GNDIO2	2	-	-
69	PR3B	2	C	RUM0_PLLC_FB_A
70	PR3A	2	T	RUM0_PLLT_FB_A
71	VCCAUX	-	-	-
72	TDO	-	-	-
73	VCCJ	-	-	-
74	TDI	-	-	-
75	TMS	-	-	-
76	TCK	-	-	-
77	VCC	-	-	-
78	PT24A	1	-	-
79	PT23A	1	-	D0
80	PT22B	1	-	D1
81	PT21A	1	-	D2
82	VCCIO1	1	-	-
83	PT20B	1	-	D3
84	GNDIO1	1	-	-
85	PT17A	1	-	D4
86	PT16A	1	-	D5
87	PT15B	1	-	D6

LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
139	PT6A	0	-	DI	PT9A	0	-	DI
140	PT5A	0	-	CSN	PT8A	0	-	CSN
141	PT3B	0	-	VREF2_0	PT6B	0	-	VREF2_0
142	CFG0	0	-	-	CFG0	0	-	-
143	CFG1	0	-	-	CFG1	0	-	-
144	DONE	0	-	-	DONE	0	-	-

1. Applies to LFXP "C" only.
2. Applies to LFXP "E" only.
3. Supports dedicated LVDS outputs.

LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP6				LFXP10			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
E16	TDO	-	-	-	TDO	-	-	-
D16	VCCJ	-	-	-	VCCJ	-	-	-
D14	TDI	-	-	-	TDI	-	-	-
C14	TMS	-	-	-	TMS	-	-	-
B14	TCK	-	-	-	TCK	-	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
A15	PT31B	1	C	-	PT35B	1	C	-
B15	PT31A	1	T	-	PT35A	1	T	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
D12	PT28A	1	-	VREF1_1	PT34B	1	C	VREF1_1
C11	PT30A	1	T	DQS	PT34A	1	T	DQS
A14	PT29B	1	-	-	PT33B	1	-	-
B13	PT30B	1	C	-	PT32A	1	-	-
F12	PT27B	1	C	-	PT31B	1	C	-
E11	PT27A	1	T	-	PT31A	1	T	-
A13	PT26B	1	C	-	PT30B	1	C	-
C13	PT26A	1	T	D0	PT30A	1	T	D0
-	GNDIO1	1	-	-	GNDIO1	1	-	-
C10	PT25B	1	C	D1	PT29B	1	C	D1
E10	PT25A	1	T	VREF2_1	PT29A	1	T	VREF2_1
A12	PT24B	1	C	-	PT28B	1	C	-
B12	PT24A	1	T	D2	PT28A	1	T	D2
C12	PT23B	1	C	D3	PT27B	1	C	D3
A11	PT23A	1	T	-	PT27A	1	T	-
B11	PT22B	1	C	-	PT26B	1	C	-
D11	PT22A	1	T	DQS	PT26A	1	T	DQS
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B9	PT21B	1	-	-	PT25B	1	-	-
D9	PT20A	1	-	D4	PT24A	1	-	D4
A10	PT19B	1	C	-	PT23B	1	C	-
B10	PT19A	1	T	D5	PT23A	1	T	D5
D10	PT18B	1	C	D6	PT22B	1	C	D6
A9	PT18A	1	T	-	PT22A	1	T	-
C9	PT17B	1	C	D7	PT21B	1	C	D7
C8	PT17A	1	T	-	PT21A	1	T	-
E9	PT16B	0	C	BUSY	PT20B	0	C	BUSY
-	GNDIO0	0	-	-	GNDIO0	0	-	-
B8	PT16A	0	T	CS1N	PT20A	0	T	CS1N
A8	PT15B	0	C	PCLKC0_0	PT19B	0	C	PCLKC0_0
A7	PT15A	0	T	PCLKT0_0	PT19A	0	T	PCLKT0_0
B7	PT14B	0	C	-	PT18B	0	C	-
C7	PT14A	0	T	DQS	PT18A	0	T	DQS

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
G7	VCCAUX	-	-	-	VCCAUX	-	-	-	VCCAUX	-	-	-
T16	VCCAUX	-	-	-	VCCAUX	-	-	-	VCCAUX	-	-	-
T7	VCCAUX	-	-	-	VCCAUX	-	-	-	VCCAUX	-	-	-
G10	VCCIO0	0	-	-	VCCIO0	0	-	-	VCCIO0	0	-	-
G11	VCCIO0	0	-	-	VCCIO0	0	-	-	VCCIO0	0	-	-
G8	VCCIO0	0	-	-	VCCIO0	0	-	-	VCCIO0	0	-	-
G9	VCCIO0	0	-	-	VCCIO0	0	-	-	VCCIO0	0	-	-
H8	VCCIO0	0	-	-	VCCIO0	0	-	-	VCCIO0	0	-	-
G12	VCCIO1	1	-	-	VCCIO1	1	-	-	VCCIO1	1	-	-
G13	VCCIO1	1	-	-	VCCIO1	1	-	-	VCCIO1	1	-	-
G14	VCCIO1	1	-	-	VCCIO1	1	-	-	VCCIO1	1	-	-
G15	VCCIO1	1	-	-	VCCIO1	1	-	-	VCCIO1	1	-	-
H15	VCCIO1	1	-	-	VCCIO1	1	-	-	VCCIO1	1	-	-
H16	VCCIO2	2	-	-	VCCIO2	2	-	-	VCCIO2	2	-	-
J16	VCCIO2	2	-	-	VCCIO2	2	-	-	VCCIO2	2	-	-
K16	VCCIO2	2	-	-	VCCIO2	2	-	-	VCCIO2	2	-	-
L16	VCCIO2	2	-	-	VCCIO2	2	-	-	VCCIO2	2	-	-
M16	VCCIO3	3	-	-	VCCIO3	3	-	-	VCCIO3	3	-	-
N16	VCCIO3	3	-	-	VCCIO3	3	-	-	VCCIO3	3	-	-
P16	VCCIO3	3	-	-	VCCIO3	3	-	-	VCCIO3	3	-	-
R16	VCCIO3	3	-	-	VCCIO3	3	-	-	VCCIO3	3	-	-
R15	VCCIO4	4	-	-	VCCIO4	4	-	-	VCCIO4	4	-	-
T12	VCCIO4	4	-	-	VCCIO4	4	-	-	VCCIO4	4	-	-
T13	VCCIO4	4	-	-	VCCIO4	4	-	-	VCCIO4	4	-	-
T14	VCCIO4	4	-	-	VCCIO4	4	-	-	VCCIO4	4	-	-
T15	VCCIO4	4	-	-	VCCIO4	4	-	-	VCCIO4	4	-	-
R8	VCCIO5	5	-	-	VCCIO5	5	-	-	VCCIO5	5	-	-
T10	VCCIO5	5	-	-	VCCIO5	5	-	-	VCCIO5	5	-	-
T11	VCCIO5	5	-	-	VCCIO5	5	-	-	VCCIO5	5	-	-
T8	VCCIO5	5	-	-	VCCIO5	5	-	-	VCCIO5	5	-	-
T9	VCCIO5	5	-	-	VCCIO5	5	-	-	VCCIO5	5	-	-
M7	VCCIO6	6	-	-	VCCIO6	6	-	-	VCCIO6	6	-	-
N7	VCCIO6	6	-	-	VCCIO6	6	-	-	VCCIO6	6	-	-
P7	VCCIO6	6	-	-	VCCIO6	6	-	-	VCCIO6	6	-	-
R7	VCCIO6	6	-	-	VCCIO6	6	-	-	VCCIO6	6	-	-
H7	VCCIO7	7	-	-	VCCIO7	7	-	-	VCCIO7	7	-	-
J7	VCCIO7	7	-	-	VCCIO7	7	-	-	VCCIO7	7	-	-
K7	VCCIO7	7	-	-	VCCIO7	7	-	-	VCCIO7	7	-	-
L7	VCCIO7	7	-	-	VCCIO7	7	-	-	VCCIO7	7	-	-

1. Applies to LFXP "C" only.
2. Applies to LFXP "E" only.
3. Supports dedicated LVDS outputs.

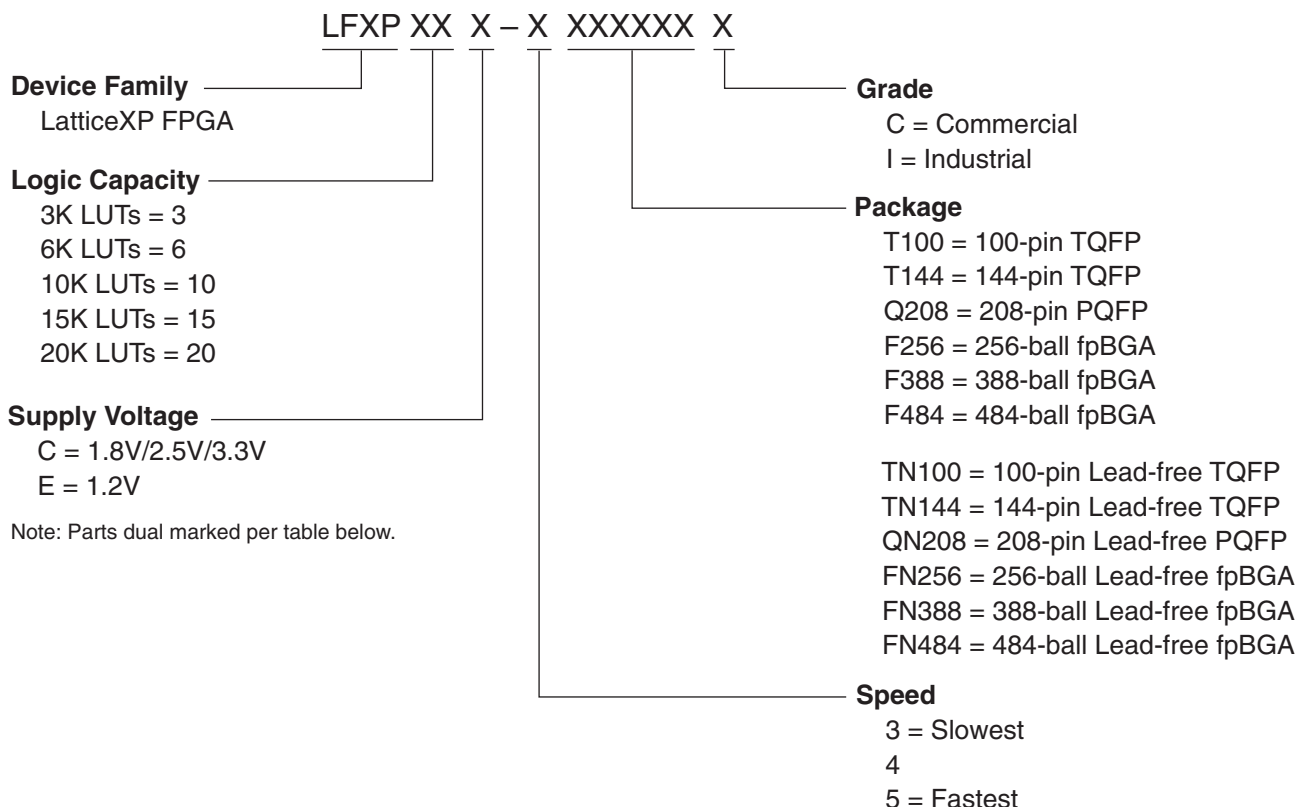
LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
T6	PL41A	6	T	-	PL45A	6	T	-
T5	PL41B	6	C	-	PL45B	6	C	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
U3	PL42A	6	T ³	-	PL46A	6	T ³	-
U4	PL42B	6	C ³	-	PL46B	6	C ³	-
V4	PL43A	6	-	-	PL47A	6	-	-
W4	SLEEPN ¹ / TOE ²	-	-	-	SLEEPN ¹ / TOE ²	-	-	-
W5	INITN	5	-	-	INITN	5	-	-
Y3	-	-	-	-	PB3B	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
U5	-	-	-	-	PB4A	5	T	-
V5	-	-	-	-	PB4B	5	C	-
Y4	-	-	-	-	PB5A	5	T	-
Y5	-	-	-	-	PB5B	5	C	-
V6	-	-	-	-	PB6A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
U6	-	-	-	-	PB6B	5	C	-
W6	PB3A	5	T	-	PB7A	5	T	-
Y6	PB3B	5	C	-	PB7B	5	C	-
AA2	PB4A	5	T	-	PB8A	5	T	-
AA3	PB4B	5	C	-	PB8B	5	C	-
V7	PB5A	5	-	-	PB9A	5	-	-
U7	PB6B	5	-	-	PB10B	5	-	-
Y7	PB7A	5	T	DQS	PB11A	5	T	DQS
W7	PB7B	5	C	-	PB11B	5	C	-
AA4	PB8A	5	T	-	PB12A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
AA5	PB8B	5	C	-	PB12B	5	C	-
AB3	PB9A	5	T	-	PB13A	5	T	-
AB4	PB9B	5	C	-	PB13B	5	C	-
AA6	PB10A	5	T	-	PB14A	5	T	-
AA7	PB10B	5	C	-	PB14B	5	C	-
U8	PB11A	5	T	-	PB15A	5	T	-
V8	PB11B	5	C	-	PB15B	5	C	-
Y8	PB12A	5	T	VREF1_5	PB16A	5	T	VREF1_5
-	GNDIO5	5	-	-	GNDIO5	5	-	-
W8	PB12B	5	C	-	PB16B	5	C	-
V9	PB13A	5	-	-	PB17A	5	-	-
U9	PB14B	5	-	-	PB18B	5	-	-
Y9	PB15A	5	T	DQS	PB19A	5	T	DQS
W9	PB15B	5	C	-	PB19B	5	C	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

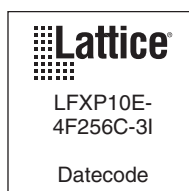
Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
R18	PR38B	3	C	RLM0_PLLC_FB_A	PR42B	3	C	RLM0_PLLC_FB_A
R17	PR38A	3	T	RLM0_PLLT_FB_A	PR42A	3	T	RLM0_PLLT_FB_A
Y22	PR37B	3	C ³	-	PR41B	3	C ³	-
Y21	PR37A	3	T ³	DQS	PR41A	3	T ³	DQS
W22	PR36B	3	-	-	PR40B	3	-	-
W21	PR35A	3	-	VREF1_3	PR39A	3	-	VREF1_3
P17	PR34B	3	C ³	-	PR38B	3	C ³	-
P18	PR34A	3	T ³	-	PR38A	3	T ³	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
R19	PR33B	3	C	-	PR37B	3	C	-
R20	PR33A	3	T	-	PR37A	3	T	-
V22	PR32B	3	C ³	-	PR36B	3	C ³	-
V21	PR32A	3	T ³	-	PR36A	3	T ³	-
U22	PR30B	3	C ³	-	PR34B	3	C ³	-
U21	PR30A	3	T ³	-	PR34A	3	T ³	-
P19	PR29B	3	C	RLM0_PLLC_IN_A	PR33B	3	C	RLM0_PLLC_IN_A
P20	PR29A	3	T	RLM0_PLLT_IN_A	PR33A	3	T	RLM0_PLLT_IN_A
-	GNDIO3	3	-	-	GNDIO3	3	-	-
T22	PR28B	3	C ³	-	PR32B	3	C ³	-
T21	PR28A	3	T ³	DQS	PR32A	3	T ³	DQS
R22	PR27B	3	-	-	PR31B	3	-	-
R21	PR26A	3	-	VREF2_3	PR30A	3	-	VREF2_3
N19	PR25B	3	C ³	-	PR29B	3	C ³	-
N20	PR25A	3	T ³	-	PR29A	3	T ³	-
N18	PR24B	3	C	-	PR28B	3	C	-
M18	PR24A	3	T	-	PR28A	3	T	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
P22	PR23B	3	C ³	-	PR27B	3	C ³	-
P21	PR23A	3	T ³	-	PR27A	3	T ³	-
N22	-	-	-	-	PR26B	3	C ³	-
N21	-	-	-	-	PR26A	3	T ³	-
M19	-	-	-	-	PR25B	3	-	-
M20	GNDP1	-	-	-	GNDP1	-	-	-
L18	VCCP1	-	-	-	VCCP1	-	-	-
M21	-	-	-	-	PR24A	2	-	-
M22	PR22B	2	C ³	-	PR23B	2	C ³	-
L22	PR22A	2	T ³	-	PR23A	2	T ³	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
L19	-	-	-	-	PR22B	2	C ³	-
L20	-	-	-	-	PR22A	2	T ³	-
L21	PR21B	2	C	PCLKC2_0	PR21B	2	C	PCLKC2_0
K22	PR21A	2	T	PCLKT2_0	PR21A	2	T	PCLKT2_0

Part Number Description



Ordering Information (Contact Factory for Specific Device Availability)

Note: LatticeXP devices are dual marked. For example, the commercial speed grade LFXP10E-4F256C is also marked with industrial grade -3I (LFXP10E-3F256I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:



Conventional Packaging**Commercial**

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3C-3Q208C	136	1.8/2.5/3.3V	-3	PQFP	208	COM	3.1K
LFXP3C-4Q208C	136	1.8/2.5/3.3V	-4	PQFP	208	COM	3.1K
LFXP3C-5Q208C	136	1.8/2.5/3.3V	-5	PQFP	208	COM	3.1K
LFXP3C-3T144C	100	1.8/2.5/3.3V	-3	TQFP	144	COM	3.1K
LFXP3C-4T144C	100	1.8/2.5/3.3V	-4	TQFP	144	COM	3.1K
LFXP3C-5T144C	100	1.8/2.5/3.3V	-5	TQFP	144	COM	3.1K
LFXP3C-3T100C	62	1.8/2.5/3.3V	-3	TQFP	100	COM	3.1K
LFXP3C-4T100C	62	1.8/2.5/3.3V	-4	TQFP	100	COM	3.1K
LFXP3C-5T100C	62	1.8/2.5/3.3V	-5	TQFP	100	COM	3.1K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6C-3F256C	188	1.8/2.5/3.3V	-3	fpBGA	256	COM	5.8K
LFXP6C-4F256C	188	1.8/2.5/3.3V	-4	fpBGA	256	COM	5.8K
LFXP6C-5F256C	188	1.8/2.5/3.3V	-5	fpBGA	256	COM	5.8K
LFXP6C-3Q208C	142	1.8/2.5/3.3V	-3	PQFP	208	COM	5.8K
LFXP6C-4Q208C	142	1.8/2.5/3.3V	-4	PQFP	208	COM	5.8K
LFXP6C-5Q208C	142	1.8/2.5/3.3V	-5	PQFP	208	COM	5.8K
LFXP6C-3T144C	100	1.8/2.5/3.3V	-3	TQFP	144	COM	5.8K
LFXP6C-4T144C	100	1.8/2.5/3.3V	-4	TQFP	144	COM	5.8K
LFXP6C-5T144C	100	1.8/2.5/3.3V	-5	TQFP	144	COM	5.8K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP10C-3F388C	244	1.8/2.5/3.3V	-3	fpBGA	388	COM	9.7K
LFXP10C-4F388C	244	1.8/2.5/3.3V	-4	fpBGA	388	COM	9.7K
LFXP10C-5F388C	244	1.8/2.5/3.3V	-5	fpBGA	388	COM	9.7K
LFXP10C-3F256C	188	1.8/2.5/3.3V	-3	fpBGA	256	COM	9.7K
LFXP10C-4F256C	188	1.8/2.5/3.3V	-4	fpBGA	256	COM	9.7K
LFXP10C-5F256C	188	1.8/2.5/3.3V	-5	fpBGA	256	COM	9.7K

For Further Information

A variety of technical notes for the LatticeXP family are available on the Lattice website at www.latticesemi.com.

- LatticeECP/EC and LatticeXP sysIO Usage Guide (TN1056)
- Lattice ispTRACY Usage Guide (TN1054)
- LatticeECP/EC and LatticeXP sysCLOCK PLL Design and Usage Guide (TN1049)
- Memory Usage Guide for LatticeECP/EC and LatticeXP Devices (TN1051)
- LatticeECP/EC and XP DDR Usage Guide (TN1050)
- Power Estimation and Management for LatticeECP/EC and LatticeXP Devices (TN1052)
- LatticeXP sysCONFIG Usage Guide (TN1082)

For further information on interface standards refer to the following web sites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com