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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

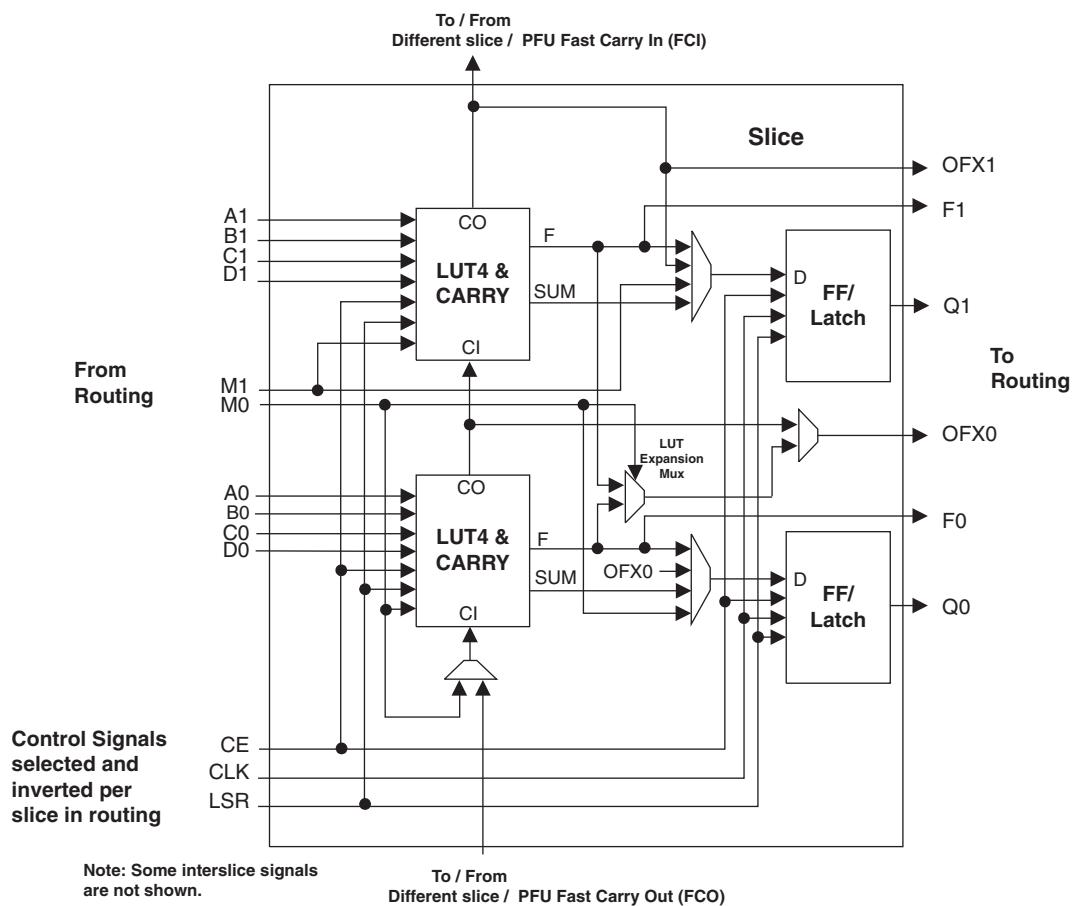
#### **Details**

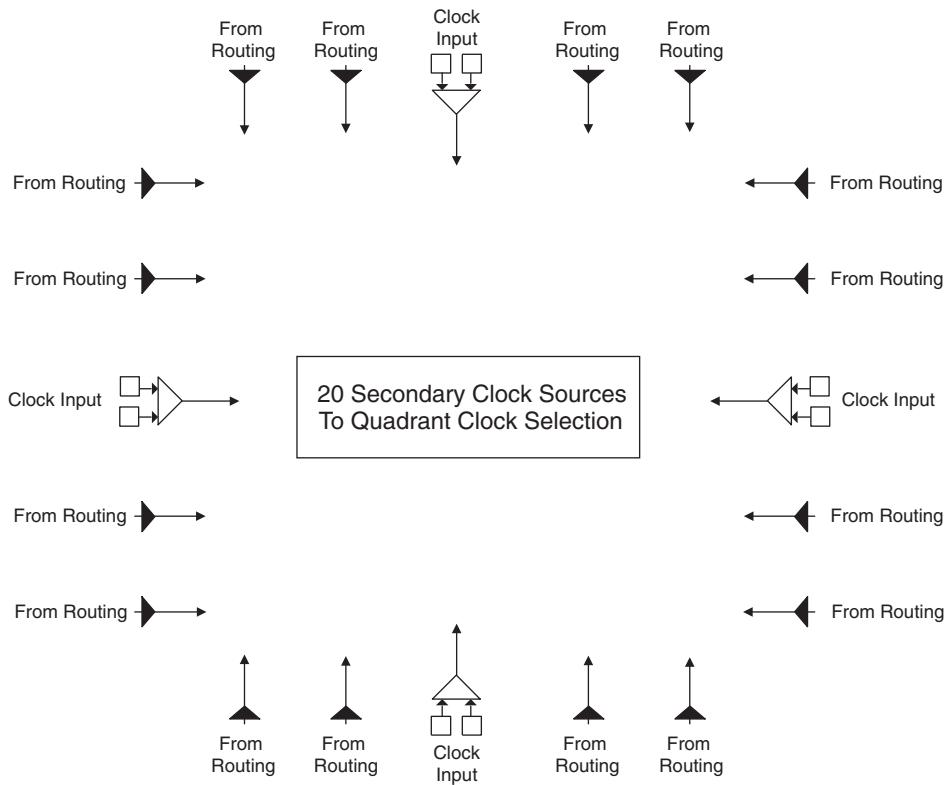
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6000
Total RAM Bits	73728
Number of I/O	188
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp6e-4fn256i">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp6e-4fn256i</a>

**Slice**

Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

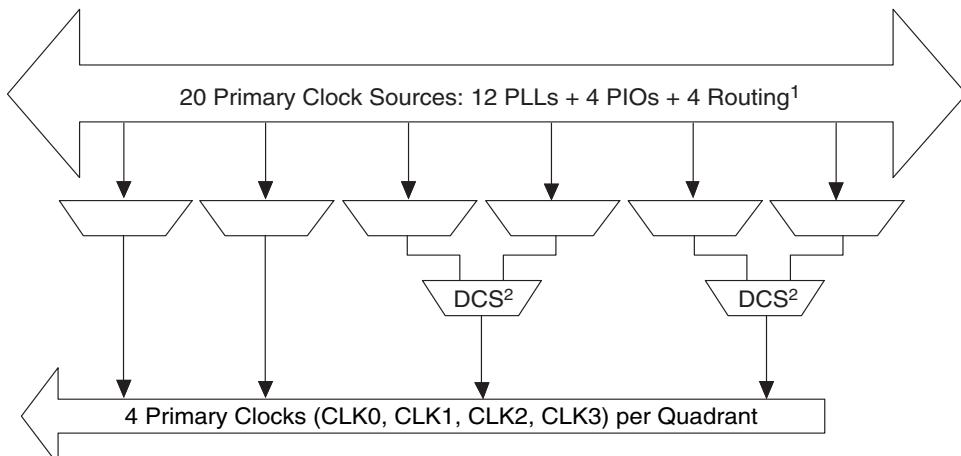
There are 14 input signals: 13 signals from routing and one from the carry-chain (from adjacent slice or PFU). There are 7 outputs: 6 to routing and one to carry-chain (to adjacent PFU). Table 2-1 lists the signals associated with each slice.

**Figure 2-3. Slice Diagram**

**Figure 2-6. Secondary Clock Sources**

## Clock Routing

The clock routing structure in LatticeXP devices consists of four Primary Clock lines and a Secondary Clock network per quadrant. The primary clocks are generated from MUXes located in each quadrant. Figure 2-7 shows this clock routing. The four secondary clocks are generated from MUXes located in each quadrant as shown in Figure 2-8. Each slice derives its clock from the primary clock lines, secondary clock lines and routing as shown in Figure 2-9.

**Figure 2-7. Per Quadrant Primary Clock Selection**

1. Smaller devices have fewer PLL related lines.  
2. Dynamic clock select.

**Hot Socketing Specifications<sup>1, 2, 3, 4, 5, 6</sup>**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{DK}$	Input or I/O Leakage Current	$0 \leq V_{IN} \leq V_{IH}$ (MAX.)	—	—	+/-1000	$\mu A$

1. Insensitive to sequence of  $V_{CC}$ ,  $V_{CCAUX}$  and  $V_{CCIO}$ . However, assumes monotonic rise/fall rates for  $V_{CC}$ ,  $V_{CCAUX}$  and  $V_{CCIO}$ .
2.  $0 \leq V_{CC} \leq V_{CC}$  (MAX) or  $0 \leq V_{CCAUX} \leq V_{CCAUX}$  (MAX).
3.  $0 \leq V_{CCIO} \leq V_{CCIO}$  (MAX) for top and bottom I/O banks.
4.  $0.2 \leq V_{CCIO} \leq V_{CCIO}$  (MAX) for left and right I/O banks.
5.  $I_{DK}$  is additive to  $I_{PU}$ ,  $I_{PW}$  or  $I_{BH}$ .
6. LVCMS and LVTTL only.

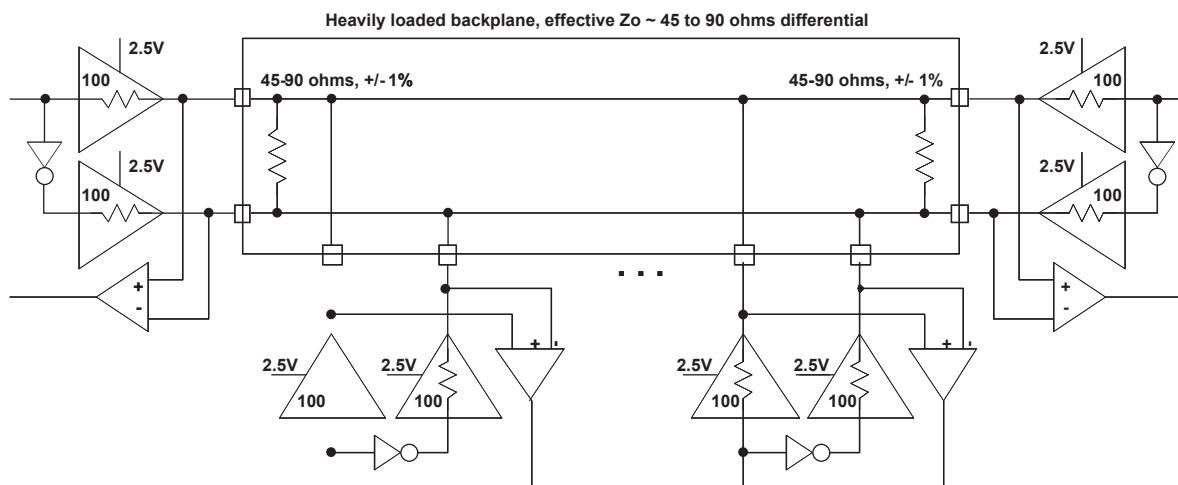
**Programming and Erase Flash Supply Current<sup>1, 2, 3, 4, 5</sup>**

Symbol	Parameter	Device	Typ <sup>6</sup>	Units
I <sub>CC</sub>	Core Power Supply	LFXP3E	30	mA
		LFXP6E	40	mA
		LFXP10E	50	mA
		LFXP15E	60	mA
		LFXP20E	70	mA
		LFXP3C	50	mA
		LFXP6C	60	mA
		LFXP10C	90	mA
		LFXP15C	100	mA
		LFXP20C	110	mA
I <sub>CCAUX</sub>	Auxiliary Power Supply V <sub>CCAUX</sub> = 3.3V	LFXP3E/C	50	mA
		LFXP6E/C	60	mA
		LFXP10E/C	90	mA
		LFXP15E/C	110	mA
		LFXP20E/C	130	mA
I <sub>CCJ</sub>	V <sub>CCJ</sub> Power Supply <sup>7</sup>	All	2	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVC MOS and held at the V<sub>CCIO</sub> or GND.
3. Blank user pattern; typical Flash pattern.
4. Bypass or decoupling capacitor across the supply.
5. JTAG programming is at 1MHz.
6. T<sub>A</sub>=25°C, power supplies at nominal voltage.
7. When programming via JTAG.

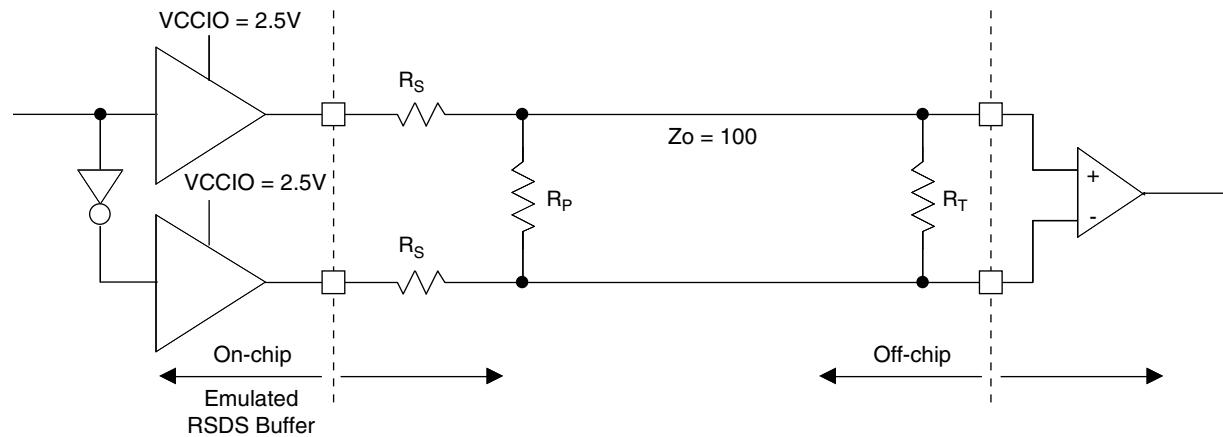
**sysIO Differential Electrical Characteristics****LVDS****Over Recommended Operating Conditions**

<b>Parameter Symbol</b>	<b>Parameter Description</b>	<b>Test Conditions</b>	<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>	<b>Units</b>
$V_{INP}, V_{INM}$	Input Voltage		0	—	2.4	V
$V_{THD}$	Differential Input Threshold		+/-100	—	—	mV
$V_{CM}$	Input Common Mode Voltage	$100\text{mV} \leq V_{THD}$	$V_{THD}/2$	1.2	1.8	V
		$200\text{mV} \leq V_{THD}$	$V_{THD}/2$	1.2	1.9	V
		$350\text{mV} \leq V_{THD}$	$V_{THD}/2$	1.2	2.0	V
$I_{IN}$	Input current	Power on or power off	—	—	+/-10	$\mu\text{A}$
$V_{OH}$	Output high voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100$ ohms	—	1.38	1.60	V
$V_{OL}$	Output low voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100$ ohms	0.9V	1.03	—	V
$V_{OD}$	Output voltage differential	$(V_{OP} - V_{OM}), R_T = 100$ ohms	250	350	450	mV
$\Delta V_{OD}$	Change in $V_{OD}$ between high and low		—	—	50	mV
$V_{OS}$	Output voltage offset	$(V_{OP} - V_{OM})/2, R_T = 100$ ohms	1.125	1.25	1.375	V
$\Delta V_{OS}$	Change in $V_{OS}$ between H and L		—	—	50	mV
$I_{OSD}$	Output short circuit current	$V_{OD} = 0\text{V}$ Driver outputs shorted	—	—	6	mA

**Figure 3-2. BLVDS Multi-point Output Example****Table 3-2. BLVDS DC Conditions<sup>1</sup>****Over Recommended Operating Conditions**

Symbol	Description	Typical		Units
		$Z_o = 45$	$Z_o = 90$	
$Z_{OUT}$	Output impedance	100	100	ohms
$R_{TLEFT}$	Left end termination	45	90	ohms
$R_{TRIGHT}$	Right end termination	45	90	ohms
$V_{OH}$	Output high voltage	1.375	1.48	V
$V_{OL}$	Output low voltage	1.125	1.02	V
$V_{OD}$	Output differential voltage	0.25	0.46	V
$V_{CM}$	Output common mode voltage	1.25	1.25	V
$I_{DC}$	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

**Figure 3-4. RSDS (Reduced Swing Differential Standard)****Table 3-4. RSDS DC Conditions**

Parameter	Description	Typical	Units
$Z_{OUT}$	Output impedance	20	ohms
$R_S$	Driver series resistor	300	ohms
$R_P$	Driver parallel resistor	121	ohms
$R_T$	Receiver termination	100	ohms
$V_{OH}$	Output high voltage	1.35	V
$V_{OL}$	Output low voltage	1.15	V
$V_{OD}$	Output differential voltage	0.20	V
$V_{CM}$	Output common mode voltage	1.25	V
$Z_{BACK}$	Back impedance	101.5	ohms
$I_{DC}$	DC output current	3.66	mA

**LatticeXP Internal Timing Parameters<sup>1</sup> (Continued)**

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RSTO\_EBR}$	Reset To Output Delay Time from EBR Output Register	—	1.61	—	1.94	—	2.32	ns
<b>PLL Parameters</b>								
$t_{RSTREC}$	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
$t_{RSTSU}$	Reset Signal Setup Time	1.00	—	1.00	—	1.00	—	ns

1. Internal parameters are characterized but not tested on every device.

Timing v.F0.11

## sysCLOCK PLL Timing

### Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Typ.	Max.	Units
$f_{IN}$	Input Clock Frequency (CLKI, CLKFB)		25	—	375	MHz
$f_{OUT}$	Output Clock Frequency (CLKOP, CLKOS)		25	—	375	MHz
$f_{OUT2}$	K-Divider Output Frequency (CLKOK)		0.195	—	187.5	MHz
$f_{VCO}$	PLL VCO Frequency		375	—	750	MHz
$f_{PFD}$	Phase Detector Input Frequency		25	—	—	MHz
<b>AC Characteristics</b>						
$t_{DT}$	Output Clock Duty Cycle	Default duty cycle elected <sup>3</sup>	45	50	55	%
$t_{PH}^4$	Output Phase Accuracy		—	—	0.05	UI
$t_{OPJIT}^1$	Output Clock Period Jitter	$f_{OUT} \geq 100\text{MHz}$	—	—	+/- 125	ps
		$f_{OUT} < 100\text{MHz}$	—	—	0.02	UIPP
$t_{SK}$	Input Clock to Output Clock Skew	Divider ratio = integer	—	—	+/- 200	ps
$t_W$	Output Clock Pulse Width	At 90% or 10% <sup>3</sup>	1	—	—	ns
$t_{LOCK}^2$	PLL Lock-in Time		—	—	150	us
$t_{PA}$	Programmable Delay Unit		100	250	400	ps
$t_{IPJIT}$	Input Clock Period Jitter		—	—	+/- 200	ps
$t_{FBKDLY}$	External Feedback Delay		—	—	10	ns
$t_{HI}$	Input Clock High Time	90% to 90%	0.5	—	—	ns
$t_{LO}$	Input Clock Low Time	10% to 10%	0.5	—	—	ns
$t_{RST}$	RST Pulse Width		10	—	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.

2. Output clock is valid after  $t_{LOCK}$  for PLL reset and dynamic delay adjustment.

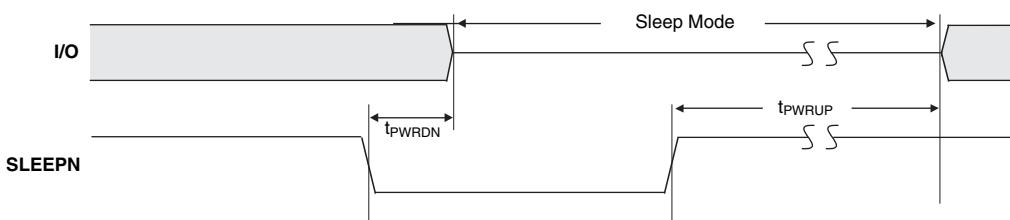
3. Using LVDS output buffers.

4. As compared to CLKOP output.

Timing v.F0.11

## LatticeXP “C” Sleep Mode Timing

Parameter	Descriptions	Min.	Typ.	Max.	Units	
$t_{PWRDN}$	SLEEPN Low to I/O Tristate	—	20	32	ns	
$t_{PWRUP}$	SLEEPN High to Power Up	LFXP3	—	1.4	2.1	ms
		LFXP6	—	1.7	2.4	ms
		LFXP10	—	1.1	1.8	ms
		LFXP15	—	1.4	2.1	ms
		LFXP20	—	1.7	2.4	ms
$t_{WSLEEPN}$	SLEEPN Pulse Width to Initiate Sleep Mode	400	—	—	ns	
$t_{WAWAKE}$	SLEEPN Pulse Rejection	—	—	120	ns	



**LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP (Cont.)**

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
93	PR9A	2	T	PCLKT2_0	PR12A	2	T	PCLKT2_0
94	PR8B	2	C	RUM0_PLLC_IN_A	PR8B	2	C	RUM0_PLLC_IN_A
95	PR8A	2	T	RUM0_PLLT_IN_A	PR8A	2	T	RUM0_PLLT_IN_A
96	PR7B	2	C <sup>3</sup>	-	PR7B	2	C <sup>3</sup>	-
97	PR7A	2	T <sup>3</sup>	DQS	PR7A	2	T <sup>3</sup>	DQS
98	VCCIO2	2	-	-	VCCIO2	2	-	-
99	PR6B	2	-	VREF1_2	PR6B	2	-	VREF1_2
100	PR5A	2	-	VREF2_2	PR5A	2	-	VREF2_2
101	GNDIO2	2	-	-	GNDIO2	2	-	-
102	PR3B	2	C	RUM0_PLLC_FB_A	PR3B	2	C	RUM0_PLLC_FB_A
103	PR3A	2	T	RUM0_PLLT_FB_A	PR3A	2	T	RUM0_PLLT_FB_A
104	PR2B	2	C <sup>3</sup>	-	PR2B	2	C <sup>3</sup>	-
105	PR2A	2	T <sup>3</sup>	-	PR2A	2	T <sup>3</sup>	-
106	VCCAUX	-	-	-	VCCAUX	-	-	-
107	TDO	-	-	-	TDO	-	-	-
108	VCCJ	-	-	-	VCCJ	-	-	-
109	TDI	-	-	-	TDI	-	-	-
110	TMS	-	-	-	TMS	-	-	-
111	TCK	-	-	-	TCK	-	-	-
112	VCC	-	-	-	VCC	-	-	-
113	PT25A	1	-	VREF1_1	PT28A	1	-	VREF1_1
114	PT24A	1	-	-	PT27A	1	-	-
115	PT23A	1	-	D0	PT26A	1	-	D0
116	PT22B	1	C	D1	PT25B	1	C	D1
117	PT22A	1	T	VREF2_1	PT25A	1	T	VREF2_1
118	PT21A	1	-	D2	PT24A	1	-	D2
119	VCCIO1	1	-	-	VCCIO1	1	-	-
120	PT20B	1	-	D3	PT23B	1	-	D3
121	GNDIO1	1	-	-	GNDIO1	1	-	-
122	PT17A	1	-	D4	PT20A	1	-	D4
123	PT16A	1	-	D5	PT19A	1	-	D5
124	PT15B	1	C	D6	PT18B	1	C	D6
125	PT15A	1	T	-	PT18A	1	T	-
126	PT14B	1	-	D7	PT17B	1	-	D7
127	GND	-	-	-	GND	-	-	-
128	PT13B	0	C	BUSY	PT16B	0	C	BUSY
129	PT13A	0	T	CS1N	PT16A	0	T	CS1N
130	PT12B	0	C	PCLKC0_0	PT15B	0	C	PCLKC0_0
131	PT12A	0	T	PCLKT0_0	PT15A	0	T	PCLKT0_0
132	PT11B	0	C	-	PT14B	0	C	-
133	VCCIO0	0	-	-	VCCIO0	0	-	-
134	PT11A	0	T	DQS	PT14A	0	T	DQS
135	PT9A	0	-	DOUT	PT12A	0	-	DOUT
136	GNDIO0	0	-	-	GNDIO0	0	-	-
137	PT8A	0	-	WRITEN	PT11A	0	-	WRITEN
138	PT7A	0	-	VREF1_0	PT10A	0	-	VREF1_0

**LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP (Cont.)**

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
139	PT6A	0	-	DI	PT9A	0	-	DI
140	PT5A	0	-	CSN	PT8A	0	-	CSN
141	PT3B	0	-	VREF2_0	PT6B	0	-	VREF2_0
142	CFG0	0	-	-	CFG0	0	-	-
143	CFG1	0	-	-	CFG1	0	-	-
144	DONE	0	-	-	DONE	0	-	-

1. Applies to LFXP "C" only.
2. Applies to LFXP "E" only.
3. Supports dedicated LVDS outputs.

**LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)**

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
47	GNDIO6	6	-	-	GNDIO6	6	-	-
48	PL18B	6	C <sup>3</sup>	-	PL26B	6	C <sup>3</sup>	-
49	GND	-	-	-	GND	-	-	-
50	VCCAUX	-	-	-	VCCAUX	-	-	-
51	SLEEPN <sup>1</sup> /TOE <sup>2</sup>	-	-	-	SLEEPN <sup>1</sup> /TOE <sup>2</sup>	-	-	-
52	INITN	5	-	-	INITN	5	-	-
53	VCC	-	-	-	VCC	-	-	-
54	PB2B	5	-	VREF1_5	PB5B	5	-	VREF1_5
55	PB3A	5	T	-	PB6A	5	T	DQS
56	PB3B	5	C	-	PB6B	5	C	-
57	PB4A	5	T	-	PB7A	5	T	-
58	PB4B	5	C	-	PB7B	5	C	-
59	GNDIO5	5	-	-	GNDIO5	5	-	-
60	PB5A	5	T	-	PB8A	5	T	-
61	PB5B	5	C	VREF2_5	PB8B	5	C	VREF2_5
62	PB6A	5	T	-	PB9A	5	T	-
63	PB6B	5	C	-	PB9B	5	C	-
64	VCCIO5	5	-	-	VCCIO5	5	-	-
65	PB7A	5	T	-	PB10A	5	T	-
66	PB7B	5	C	-	PB10B	5	C	-
67	PB8A	5	T	-	PB11A	5	T	-
68	PB8B	5	C	-	PB11B	5	C	-
69	GNDIO5	5	-	-	GNDIO5	5	-	-
70	PB9A	5	-	-	PB12A	5	-	-
71	PB10B	5	-	-	PB13B	5	-	-
72	PB11A	5	T	DQS	PB14A	5	T	DQS
73	PB11B	5	C	-	PB14B	5	C	-
74	VCCIO5	5	-	-	VCCIO5	5	-	-
75	PB12A	5	T	-	PB15A	5	T	-
76	PB12B	5	C	-	PB15B	5	C	-
77	PB13A	5	T	-	PB16A	5	T	-
78	PB13B	5	C	-	PB16B	5	C	-
79	GND	-	-	-	GND	-	-	-
80	VCC	-	-	-	VCC	-	-	-
81	PB14A	4	T	-	PB17A	4	T	-
82	GNDIO4	4	-	-	GNDIO4	4	-	-
83	PB14B	4	C	-	PB17B	4	C	-
84	PB15A	4	T	PCLKT4_0	PB18A	4	T	PCLKT4_0
85	PB15B	4	C	PCLKC4_0	PB18B	4	C	PCLKC4_0
86	PB16A	4	T	-	PB19A	4	T	-
87	VCCIO4	4	-	-	VCCIO4	4	-	-
88	PB16B	4	C	-	PB19B	4	C	-
89	PB17A	4	-	-	PB20A	4	-	-
90	PB18B	4	-	-	PB21B	4	-	-
91	PB19A	4	T	DQS	PB22A	4	T	DQS
92	GNDIO4	4	-	-	GNDIO4	4	-	-

**LFXP6 & LFXP10 Logic Signal Connections: 256 fpBGA (Cont.)**

Ball Number	LFXP6				LFXP10			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L15	PR21B	3	C <sup>3</sup>	-	PR28B	3	C <sup>3</sup>	-
L14	PR21A	3	T <sup>3</sup>	-	PR28A	3	T <sup>3</sup>	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
L12	PR17B	3	C	-	PR26A	3	-	-
M16	PR20B	3	C	-	PR25B	3	C	RLM0_PLLC_IN_A
N16	PR20A	3	T	-	PR25A	3	T	RLM0_PLLT_IN_A
K14	PR19B	3	C <sup>3</sup>	-	PR24B	3	C <sup>3</sup>	-
K15	PR19A	3	T <sup>3</sup>	-	PR24A	3	T <sup>3</sup>	DQS
K12	PR17A	3	T	-	PR23B	3	-	-
K13	PR22A	3	-	VREF2_3	PR22A	3	-	VREF2_3
-	GNDIO3	3	-	-	GNDIO3	3	-	-
L16	PR18B	3	C <sup>3</sup>	-	PR21B	3	C <sup>3</sup>	-
K16	PR18A	3	T <sup>3</sup>	-	PR21A	3	T <sup>3</sup>	-
J15	PR16B	3	C <sup>3</sup>	-	PR19B	3	C <sup>3</sup>	-
J14	PR16A	3	T <sup>3</sup>	-	PR19A	3	T <sup>3</sup>	-
J13	GNDP1	-	-	-	GNDP1	-	-	-
J12	VCCP1	-	-	-	VCCP1	-	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
J16	PR12B	2	C	PCLKC2_0	PR17B	2	C	PCLKC2_0
H16	PR12A	2	T	PCLKT2_0	PR17A	2	T	PCLKT2_0
H13	PR13B	2	C <sup>3</sup>	-	PR16B	2	C <sup>3</sup>	-
H12	PR13A	2	T <sup>3</sup>	-	PR16A	2	T <sup>3</sup>	DQS
H15	PR2B	2	C <sup>3</sup>	-	PR15B	2	-	-
H14	PR6B	2	-	VREF1_2	PR14A	2	-	VREF1_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G15	PR11B	2	C <sup>3</sup>	-	PR13B	2	C <sup>3</sup>	-
G14	PR11A	2	T <sup>3</sup>	-	PR13A	2	T <sup>3</sup>	-
G16	PR8B	2	C	RUM0_PLLC_IN_A	PR12B	2	C	RUM0_PLLC_IN_A
F16	PR8A	2	T	RUM0_PLLT_IN_A	PR12A	2	T	RUM0_PLLT_IN_A
G13	PR2A	2	T <sup>3</sup>	-	PR11B	2	-	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
G12	PR9B	2	C <sup>3</sup>	-	PR8B	2	C	-
F13	PR9A	2	T <sup>3</sup>	-	PR8A	2	T	-
B16	PR7B	2	C <sup>3</sup>	-	PR7B	2	C <sup>3</sup>	-
C16	PR7A	2	T <sup>3</sup>	DQS	PR7A	2	T <sup>3</sup>	DQS
F15	PR14A	2	-	-	PR6B	2	-	-
E15	PR5A	2	-	VREF2_2	PR5A	2	-	VREF2_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
F14	PR4B	2	C <sup>3</sup>	-	PR4B	2	C <sup>3</sup>	-
E14	PR4A	2	T <sup>3</sup>	-	PR4A	2	T <sup>3</sup>	-
D15	PR3B	2	C	RUM0_PLLC_FB_A	PR3B	2	C	RUM0_PLLC_FB_A
C15	PR3A	2	T	RUM0_PLLT_FB_A	PR3A	2	T	RUM0_PLLT_FB_A

**LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)**

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
L4	PL32A	6	-	-	PL36A	6	-	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
K4	PL33A	6	T	-	PL37A	6	T	-
K5	PL33B	6	C	-	PL37B	6	C	-
N1	PL35A	6	-	VREF2_6	PL39A	6	-	VREF2_6
N2	PL36B	6	-	-	PL40B	6	-	-
P1	PL37A	6	T <sup>3</sup>	DQS	PL41A	6	T <sup>3</sup>	DQS
P2	PL37B	6	C <sup>3</sup>	-	PL41B	6	C <sup>3</sup>	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
L5	PL38A	6	T	LLM0_PLLT_FB_A	PL42A	6	T	LLM0_PLLT_FB_A
M6	PL38B	6	C	LLM0_PLLC_FB_A	PL42B	6	C	LLM0_PLLC_FB_A
M3	PL39A	6	T <sup>3</sup>	-	PL43A	6	T <sup>3</sup>	-
N3	PL39B	6	C <sup>3</sup>	-	PL43B	6	C <sup>3</sup>	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
P4	SLEEPN <sup>1</sup> /TOE <sup>2</sup>	-	-	-	SLEEPN <sup>1</sup> /TOE <sup>2</sup>	-	-	-
P3	INITN	5	-	-	INITN	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
R4	PB11A	5	T	-	PB15A	5	T	-
N5	PB11B	5	C	-	PB15B	5	C	-
P5	PB12A	5	T	VREF1_5	PB16A	5	T	VREF1_5
-	GNDIO5	5	-	-	GNDIO5	5	-	-
R1	PB12B	5	C	-	PB16B	5	C	-
N6	PB13A	5	-	-	PB17A	5	-	-
M7	PB14B	5	-	-	PB18B	5	-	-
R2	PB15A	5	T	DQS	PB19A	5	T	DQS
T2	PB15B	5	C	-	PB19B	5	C	-
R3	PB16A	5	T	-	PB20A	5	T	-
T3	PB16B	5	C	-	PB20B	5	C	-
T4	PB17A	5	T	-	PB21A	5	T	-
R5	PB17B	5	C	VREF2_5	PB21B	5	C	VREF2_5
N7	PB18A	5	T	-	PB22A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
M8	PB18B	5	C	-	PB22B	5	C	-
T5	PB19A	5	T	-	PB23A	5	T	-
P6	PB19B	5	C	-	PB23B	5	C	-
T6	PB20A	5	T	-	PB24A	5	T	-
R6	PB20B	5	C	-	PB24B	5	C	-
P7	PB21A	5	-	-	PB25A	5	-	-
N8	PB22B	5	-	-	PB26B	5	-	-
R7	PB23A	5	T	DQS	PB27A	5	T	DQS

**LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)**

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
U1	PL25A	6	T	LLM0_PLLT_IN_A	PL29A	6	T	LLM0_PLLT_IN_A	PL33A	6	T	LLM0_PLLT_IN_A
T2	PL25B	6	C	LLM0_PLLC_IN_A	PL29B	6	C	LLM0_PLLC_IN_A	PL33B	6	C	LLM0_PLLC_IN_A
V1	PL26A	6	T <sup>3</sup>	-	PL30A	6	T <sup>3</sup>	-	PL34A	6	T <sup>3</sup>	-
U2	PL26B	6	C <sup>3</sup>	-	PL30B	6	C <sup>3</sup>	-	PL34B	6	C <sup>3</sup>	-
W1	PL28A	6	T <sup>3</sup>	-	PL32A	6	T <sup>3</sup>	-	PL36A	6	T <sup>3</sup>	-
V2	PL28B	6	C <sup>3</sup>	-	PL32B	6	C <sup>3</sup>	-	PL36B	6	C <sup>3</sup>	-
-	GNDIO6	6	-	-	GNDIO6	-	-	-	GNDIO6	6	-	-
P3	PL29A	6	T	-	PL33A	6	T	-	PL37A	6	T	-
P4	PL29B	6	C	-	PL33B	6	C	-	PL37B	6	C	-
Y1	PL30A	6	T <sup>3</sup>	-	PL34A	6	T <sup>3</sup>	-	PL38A	6	T <sup>3</sup>	-
W2	PL30B	6	C <sup>3</sup>	-	PL34B	6	C <sup>3</sup>	-	PL38B	6	C <sup>3</sup>	-
R3	PL31A	6	-	VREF2_6	PL35A	6	-	VREF2_6	PL39A	6	-	VREF2_6
R4	PL32B	6	-	-	PL36B	6	-	-	PL40B	6	-	-
T3	PL33A	6	T <sup>3</sup>	DQS	PL37A	6	T <sup>3</sup>	DQS	PL41A	6	T <sup>3</sup>	DQS
T4	PL33B	6	C <sup>3</sup>	-	PL37B	6	C <sup>3</sup>	-	PL41B	6	C <sup>3</sup>	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
V4	PL34A	6	T	LLM0_PLLT_FB_A	PL38A	6	T	LLM0_PLLT_FB_A	PL42A	6	T	LLM0_PLLT_FB_A
V3	PL34B	6	C	LLM0_PLLC_FB_A	PL38B	6	C	LLM0_PLLC_FB_A	PL42B	6	C	LLM0_PLLC_FB_A
U4	PL35A	6	T <sup>3</sup>	-	PL39A	6	T <sup>3</sup>	-	PL43A	6	T <sup>3</sup>	-
U3	PL35B	6	C <sup>3</sup>	-	PL39B	6	C <sup>3</sup>	-	PL43B	6	C <sup>3</sup>	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
W5	SLEEPN <sup>1</sup> /TOE <sup>2</sup>	-	-	-	SLEEPN <sup>1</sup> /TOE <sup>2</sup>	-	-	-	SLEEPN <sup>1</sup> /TOE <sup>2</sup>	-	-	-
Y2	INITN	5	-	-	INITN	5	-	-	INITN	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y3	-	-	-	-	PB3B	5	-	-	PB7B	5	-	-
W3	-	-	-	-	PB4A	5	T	-	PB8A	5	T	-
W4	-	-	-	-	PB4B	5	C	-	PB8B	5	C	-
AA2	-	-	-	-	PB5A	5	-	-	PB9A	5	-	-
AA1	-	-	-	-	PB6B	5	-	-	PB10B	5	-	-
W6	PB2A	5	-	-	PB7A	5	T	DQS	PB11A	5	T	DQS
W7	-	-	-	-	PB7B	5	C	-	PB11B	5	C	-
Y4	PB3A	5	T	-	PB8A	5	T	-	PB12A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y5	PB3B	5	C	-	PB8B	5	C	-	PB12B	5	C	-
AB2	PB4A	5	T	-	PB9A	5	T	-	PB13A	5	T	-
AA3	PB4B	5	C	-	PB9B	5	C	-	PB13B	5	C	-
AB3	PB5A	5	T	-	PB10A	5	T	-	PB14A	5	T	-
AA4	PB5B	5	C	-	PB10B	5	C	-	PB14B	5	C	-
W8	PB6A	5	T	-	PB11A	5	T	-	PB15A	5	T	-
W9	PB6B	5	C	-	PB11B	5	C	-	PB15B	5	C	-
AB4	PB7A	5	T	VREF1_5	PB12A	5	T	VREF1_5	PB16A	5	T	VREF1_5
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
AA5	PB7B	5	C	-	PB12B	5	C	-	PB16B	5	C	-
AB5	PB8A	5	-	-	PB13A	5	-	-	PB17A	5	-	-
Y6	PB9B	5	-	-	PB14B	5	-	-	PB18B	5	-	-
AA6	PB10A	5	T	DQS	PB15A	5	T	DQS	PB19A	5	T	DQS
AB6	PB10B	5	C	-	PB15B	5	C	-	PB19B	5	C	-
Y9	PB11A	5	T	-	PB16A	5	T	-	PB20A	5	T	-

**LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)**

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
G7	VCCAUX	-	-	-	VCCAUX	-	-	-	VCCAUX	-	-	-
T16	VCCAUX	-	-	-	VCCAUX	-	-	-	VCCAUX	-	-	-
T7	VCCAUX	-	-	-	VCCAUX	-	-	-	VCCAUX	-	-	-
G10	VCCIO0	0	-	-	VCCIO0	0	-	-	VCCIO0	0	-	-
G11	VCCIO0	0	-	-	VCCIO0	0	-	-	VCCIO0	0	-	-
G8	VCCIO0	0	-	-	VCCIO0	0	-	-	VCCIO0	0	-	-
G9	VCCIO0	0	-	-	VCCIO0	0	-	-	VCCIO0	0	-	-
H8	VCCIO0	0	-	-	VCCIO0	0	-	-	VCCIO0	0	-	-
G12	VCCIO1	1	-	-	VCCIO1	1	-	-	VCCIO1	1	-	-
G13	VCCIO1	1	-	-	VCCIO1	1	-	-	VCCIO1	1	-	-
G14	VCCIO1	1	-	-	VCCIO1	1	-	-	VCCIO1	1	-	-
G15	VCCIO1	1	-	-	VCCIO1	1	-	-	VCCIO1	1	-	-
H15	VCCIO1	1	-	-	VCCIO1	1	-	-	VCCIO1	1	-	-
H16	VCCIO2	2	-	-	VCCIO2	2	-	-	VCCIO2	2	-	-
J16	VCCIO2	2	-	-	VCCIO2	2	-	-	VCCIO2	2	-	-
K16	VCCIO2	2	-	-	VCCIO2	2	-	-	VCCIO2	2	-	-
L16	VCCIO2	2	-	-	VCCIO2	2	-	-	VCCIO2	2	-	-
M16	VCCIO3	3	-	-	VCCIO3	3	-	-	VCCIO3	3	-	-
N16	VCCIO3	3	-	-	VCCIO3	3	-	-	VCCIO3	3	-	-
P16	VCCIO3	3	-	-	VCCIO3	3	-	-	VCCIO3	3	-	-
R16	VCCIO3	3	-	-	VCCIO3	3	-	-	VCCIO3	3	-	-
R15	VCCIO4	4	-	-	VCCIO4	4	-	-	VCCIO4	4	-	-
T12	VCCIO4	4	-	-	VCCIO4	4	-	-	VCCIO4	4	-	-
T13	VCCIO4	4	-	-	VCCIO4	4	-	-	VCCIO4	4	-	-
T14	VCCIO4	4	-	-	VCCIO4	4	-	-	VCCIO4	4	-	-
T15	VCCIO4	4	-	-	VCCIO4	4	-	-	VCCIO4	4	-	-
R8	VCCIO5	5	-	-	VCCIO5	5	-	-	VCCIO5	5	-	-
T10	VCCIO5	5	-	-	VCCIO5	5	-	-	VCCIO5	5	-	-
T11	VCCIO5	5	-	-	VCCIO5	5	-	-	VCCIO5	5	-	-
T8	VCCIO5	5	-	-	VCCIO5	5	-	-	VCCIO5	5	-	-
T9	VCCIO5	5	-	-	VCCIO5	5	-	-	VCCIO5	5	-	-
M7	VCCIO6	6	-	-	VCCIO6	6	-	-	VCCIO6	6	-	-
N7	VCCIO6	6	-	-	VCCIO6	6	-	-	VCCIO6	6	-	-
P7	VCCIO6	6	-	-	VCCIO6	6	-	-	VCCIO6	6	-	-
R7	VCCIO6	6	-	-	VCCIO6	6	-	-	VCCIO6	6	-	-
H7	VCCIO7	7	-	-	VCCIO7	7	-	-	VCCIO7	7	-	-
J7	VCCIO7	7	-	-	VCCIO7	7	-	-	VCCIO7	7	-	-
K7	VCCIO7	7	-	-	VCCIO7	7	-	-	VCCIO7	7	-	-
L7	VCCIO7	7	-	-	VCCIO7	7	-	-	VCCIO7	7	-	-

1. Applies to LFXP "C" only.

2. Applies to LFXP "E" only.

3. Supports dedicated LVDS outputs.

**LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)**

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
R18	PR38B	3	C	RLM0_PLLC_FB_A	PR42B	3	C	RLM0_PLLC_FB_A
R17	PR38A	3	T	RLM0_PLLT_FB_A	PR42A	3	T	RLM0_PLLT_FB_A
Y22	PR37B	3	C <sup>3</sup>	-	PR41B	3	C <sup>3</sup>	-
Y21	PR37A	3	T <sup>3</sup>	DQS	PR41A	3	T <sup>3</sup>	DQS
W22	PR36B	3	-	-	PR40B	3	-	-
W21	PR35A	3	-	VREF1_3	PR39A	3	-	VREF1_3
P17	PR34B	3	C <sup>3</sup>	-	PR38B	3	C <sup>3</sup>	-
P18	PR34A	3	T <sup>3</sup>	-	PR38A	3	T <sup>3</sup>	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
R19	PR33B	3	C	-	PR37B	3	C	-
R20	PR33A	3	T	-	PR37A	3	T	-
V22	PR32B	3	C <sup>3</sup>	-	PR36B	3	C <sup>3</sup>	-
V21	PR32A	3	T <sup>3</sup>	-	PR36A	3	T <sup>3</sup>	-
U22	PR30B	3	C <sup>3</sup>	-	PR34B	3	C <sup>3</sup>	-
U21	PR30A	3	T <sup>3</sup>	-	PR34A	3	T <sup>3</sup>	-
P19	PR29B	3	C	RLM0_PLLC_IN_A	PR33B	3	C	RLM0_PLLC_IN_A
P20	PR29A	3	T	RLM0_PLLT_IN_A	PR33A	3	T	RLM0_PLLT_IN_A
-	GNDIO3	3	-	-	GNDIO3	3	-	-
T22	PR28B	3	C <sup>3</sup>	-	PR32B	3	C <sup>3</sup>	-
T21	PR28A	3	T <sup>3</sup>	DQS	PR32A	3	T <sup>3</sup>	DQS
R22	PR27B	3	-	-	PR31B	3	-	-
R21	PR26A	3	-	VREF2_3	PR30A	3	-	VREF2_3
N19	PR25B	3	C <sup>3</sup>	-	PR29B	3	C <sup>3</sup>	-
N20	PR25A	3	T <sup>3</sup>	-	PR29A	3	T <sup>3</sup>	-
N18	PR24B	3	C	-	PR28B	3	C	-
M18	PR24A	3	T	-	PR28A	3	T	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
P22	PR23B	3	C <sup>3</sup>	-	PR27B	3	C <sup>3</sup>	-
P21	PR23A	3	T <sup>3</sup>	-	PR27A	3	T <sup>3</sup>	-
N22	-	-	-	-	PR26B	3	C <sup>3</sup>	-
N21	-	-	-	-	PR26A	3	T <sup>3</sup>	-
M19	-	-	-	-	PR25B	3	-	-
M20	GNDP1	-	-	-	GNDP1	-	-	-
L18	VCCP1	-	-	-	VCCP1	-	-	-
M21	-	-	-	-	PR24A	2	-	-
M22	PR22B	2	C <sup>3</sup>	-	PR23B	2	C <sup>3</sup>	-
L22	PR22A	2	T <sup>3</sup>	-	PR23A	2	T <sup>3</sup>	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
L19	-	-	-	-	PR22B	2	C <sup>3</sup>	-
L20	-	-	-	-	PR22A	2	T <sup>3</sup>	-
L21	PR21B	2	C	PCLKC2_0	PR21B	2	C	PCLKC2_0
K22	PR21A	2	T	PCLKT2_0	PR21A	2	T	PCLKT2_0

**LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)**

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
J21	PR20B	2	C <sup>3</sup>	-	PR20B	2	C <sup>3</sup>	-
J22	PR20A	2	T <sup>3</sup>	DQS	PR20A	2	T <sup>3</sup>	DQS
K18	PR19B	2	-	-	PR19B	2	-	-
K19	PR18A	2	-	VREF1_2	PR18A	2	-	VREF1_2
-	GNDIO2	2	-	-	GNDIO2	2	-	-
K21	PR17B	2	C <sup>3</sup>	-	PR17B	2	C <sup>3</sup>	-
K20	PR17A	2	T <sup>3</sup>	-	PR17A	2	T <sup>3</sup>	-
H21	PR16B	2	C	RUM0_PLLC_IN_A	PR16B	2	C	RUM0_PLLC_IN_A
H22	PR16A	2	T	RUM0_PLLT_IN_A	PR16A	2	T	RUM0_PLLT_IN_A
J20	PR15B	2	C <sup>3</sup>	-	PR15B	2	C <sup>3</sup>	-
J19	PR15A	2	T <sup>3</sup>	-	PR15A	2	T <sup>3</sup>	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
J17	PR13B	2	C <sup>3</sup>	-	PR13B	2	C <sup>3</sup>	-
J18	PR13A	2	T <sup>3</sup>	-	PR13A	2	T <sup>3</sup>	-
G21	PR12B	2	C	-	PR12B	2	C	-
G22	PR12A	2	T	-	PR12A	2	T	-
F21	PR11B	2	C <sup>3</sup>	-	PR11B	2	C <sup>3</sup>	-
F22	PR11A	2	T <sup>3</sup>	DQS	PR11A	2	T <sup>3</sup>	DQS
-	GNDIO2	2	-	-	GNDIO2	2	-	-
H20	PR10B	2	-	-	PR10B	2	-	-
H19	PR9A	2	-	VREF2_2	PR9A	2	-	VREF2_2
H17	PR8B	2	C <sup>3</sup>	-	PR8B	2	C <sup>3</sup>	-
H18	PR8A	2	T <sup>3</sup>	-	PR8A	2	T <sup>3</sup>	-
E21	PR7B	2	C	RUM0_PLLC_FB_A	PR7B	2	C	RUM0_PLLC_FB_A
E22	PR7A	2	T	RUM0_PLLT_FB_A	PR7A	2	T	RUM0_PLLT_FB_A
D21	PR6B	2	C <sup>3</sup>	-	PR6B	2	C <sup>3</sup>	-
D22	PR6A	2	T <sup>3</sup>	-	PR6A	2	T <sup>3</sup>	-
G20	PR5B	2	C <sup>3</sup>	-	PR5B	2	C <sup>3</sup>	-
G19	PR5A	2	T <sup>3</sup>	-	PR5A	2	T <sup>3</sup>	-
G17	PR4B	2	C	-	PR4B	2	C	-
G18	PR4A	2	T	-	PR4A	2	T	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
F18	PR3B	2	C <sup>3</sup>	-	PR3B	2	C <sup>3</sup>	-
F19	PR3A	2	T <sup>3</sup>	-	PR3A	2	T <sup>3</sup>	-
C22	PR2B	2	-	-	PR2B	2	-	-
F20	TDO	-	-	-	TDO	-	-	-
E20	VCCJ	-	-	-	VCCJ	-	-	-
D19	TDI	-	-	-	TDI	-	-	-
E19	TMS	-	-	-	TMS	-	-	-
D20	TCK	-	-	-	TCK	-	-	-
C20	-	-	-	-	PT56A	1	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-

**LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)**

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
D18	-	-	-	-	PT55B	1	C	-
E18	-	-	-	-	PT55A	1	T	-
C19	-	-	-	-	PT54B	1	C	-
C18	-	-	-	-	PT54A	1	T	-
C21	-	-	-	-	PT53B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B21	-	-	-	-	PT53A	1	T	-
E17	PT48B	1	C	-	PT52B	1	C	-
E16	PT48A	1	T	-	PT52A	1	T	-
C17	PT47B	1	C	-	PT51B	1	C	-
D17	PT47A	1	T	DQS	PT51A	1	T	DQS
F17	PT46B	1	-	-	PT50B	1	-	-
F16	PT45A	1	-	-	PT49A	1	-	-
C16	PT44B	1	C	-	PT48B	1	C	-
D16	PT44A	1	T	-	PT48A	1	T	-
A20	PT43B	1	C	-	PT47B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B20	PT43A	1	T	-	PT47A	1	T	-
A19	PT42B	1	C	-	PT46B	1	C	-
B19	PT42A	1	T	-	PT46A	1	T	-
C15	PT41B	1	C	-	PT45B	1	C	-
D15	PT41A	1	T	-	PT45A	1	T	-
A18	PT40B	1	C	-	PT44B	1	C	-
B18	PT40A	1	T	-	PT44A	1	T	-
F15	PT39B	1	C	VREF1_1	PT43B	1	C	VREF1_1
-	GNDIO1	1	-	-	GNDIO1	1	-	-
E15	PT39A	1	T	DQS	PT43A	1	T	DQS
A17	PT38B	1	-	-	PT42B	1	-	-
B17	PT37A	1	-	-	PT41A	1	-	-
E14	PT36B	1	C	-	PT40B	1	C	-
F14	PT36A	1	T	-	PT40A	1	T	-
D14	PT35B	1	C	-	PT39B	1	C	-
C14	PT35A	1	T	D0	PT39A	1	T	D0
A16	PT34B	1	C	D1	PT38B	1	C	D1
B16	PT34A	1	T	VREF2_1	PT38A	1	T	VREF2_1
A15	PT33B	1	C	-	PT37B	1	C	-
B15	PT33A	1	T	D2	PT37A	1	T	D2
-	GNDIO1	1	-	-	GNDIO1	1	-	-
E13	PT32B	1	C	D3	PT36B	1	C	D3
D13	PT32A	1	T	-	PT36A	1	T	-
C13	PT31B	1	C	-	PT35B	1	C	-
B13	PT31A	1	T	DQS	PT35A	1	T	DQS

**Commercial (Cont.)**

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP15E-3FN484C	300	1.2V	-3	fpBGA	484	COM	15.5K
LFXP15E-4FN484C	300	1.2V	-4	fpBGA	484	COM	15.5K
LFXP15E-5FN484C	300	1.2V	-5	fpBGA	484	COM	15.5K
LFXP15E-3FN388C	268	1.2V	-3	fpBGA	388	COM	15.5K
LFXP15E-4FN388C	268	1.2V	-4	fpBGA	388	COM	15.5K
LFXP15E-5FN388C	268	1.2V	-5	fpBGA	388	COM	15.5K
LFXP15E-3FN256C	188	1.2V	-3	fpBGA	256	COM	15.5K
LFXP15E-4FN256C	188	1.2V	-4	fpBGA	256	COM	15.5K
LFXP15E-5FN256C	188	1.2V	-5	fpBGA	256	COM	15.5K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP20E-3FN484C	340	1.2V	-3	fpBGA	484	COM	19.7K
LFXP20E-4FN484C	340	1.2V	-4	fpBGA	484	COM	19.7K
LFXP20E-5FN484C	340	1.2V	-5	fpBGA	484	COM	19.7K
LFXP20E-3FN388C	268	1.2V	-3	fpBGA	388	COM	19.7K
LFXP20E-4FN388C	268	1.2V	-4	fpBGA	388	COM	19.7K
LFXP20E-5FN388C	268	1.2V	-5	fpBGA	388	COM	19.7K
LFXP20E-3FN256C	188	1.2V	-3	fpBGA	256	COM	19.7K
LFXP20E-4FN256C	188	1.2V	-4	fpBGA	256	COM	19.7K
LFXP20E-5FN256C	188	1.2V	-5	fpBGA	256	COM	19.7K

**Industrial**

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP3C-3QN208I	136	1.8/2.5/3.3V	-3	PQFP	208	IND	3.1K
LFXP3C-4QN208I	136	1.8/2.5/3.3V	-4	PQFP	208	IND	3.1K
LFXP3C-3TN144I	100	1.8/2.5/3.3V	-3	TQFP	144	IND	3.1K
LFXP3C-4TN144I	100	1.8/2.5/3.3V	-4	TQFP	144	IND	3.1K
LFXP3C-3TN100I	62	1.8/2.5/3.3V	-3	TQFP	100	IND	3.1K
LFXP3C-4TN100I	62	1.8/2.5/3.3V	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs
LFXP6C-3FN256I	188	1.8/2.5/3.3V	-3	fpBGA	256	IND	5.8K
LFXP6C-4FN256I	188	1.8/2.5/3.3V	-4	fpBGA	256	IND	5.8K
LFXP6C-3QN208I	142	1.8/2.5/3.3V	-3	PQFP	208	IND	5.8K
LFXP6C-4QN208I	142	1.8/2.5/3.3V	-4	PQFP	208	IND	5.8K
LFXP6C-3TN144I	100	1.8/2.5/3.3V	-3	TQFP	144	IND	5.8K
LFXP6C-4TN144I	100	1.8/2.5/3.3V	-4	TQFP	144	IND	5.8K