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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6000
Total RAM Bits	73728
Number of I/O	100
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp6e-4t144i

Introduction

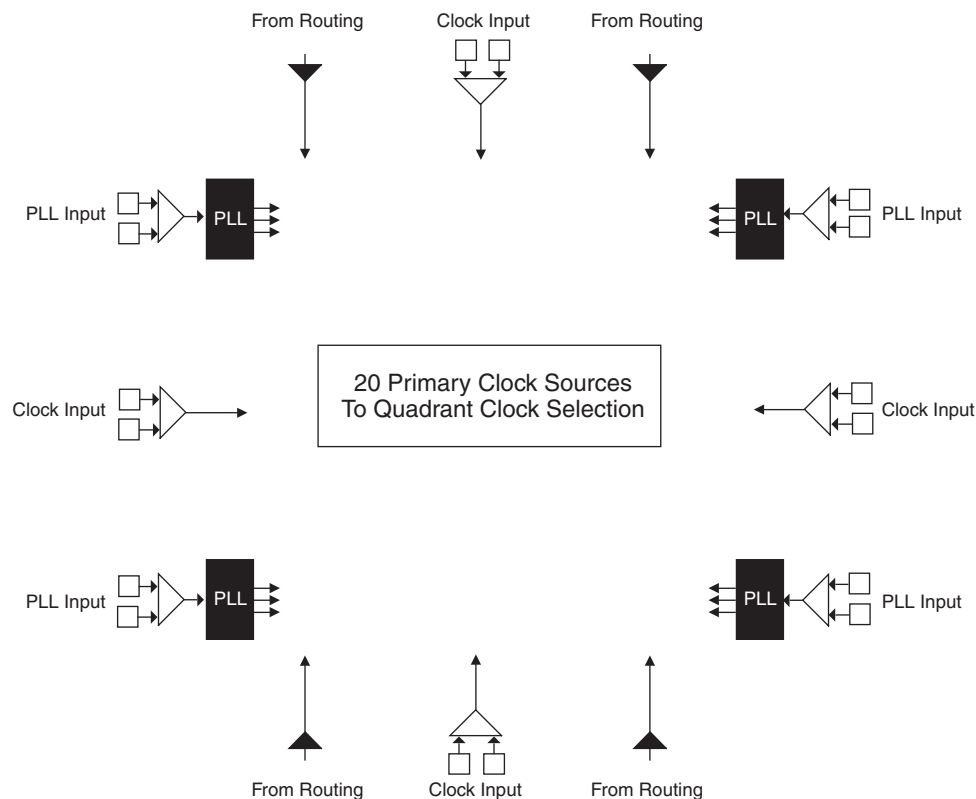
The LatticeXP family of FPGA devices combine logic gates, embedded memory and high performance I/Os in a single architecture that is both non-volatile and infinitely reconfigurable to support cost-effective system designs.

The re-programmable non-volatile technology used in the LatticeXP family is the next generation ispXP™ technology. With this technology, expensive external configuration memories are not required and designs are secured from unauthorized read-back. In addition, instant-on capability allows for easy interfacing in many applications.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeXP family of FPGA devices. Synthesis library support for LatticeXP is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeXP device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeXP family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Figure 2-5. Primary Clock Sources



Note: Smaller devices have two PLLs.

Secondary Clock Sources

LatticeXP devices have four secondary clock resources per quadrant. The secondary clock branches are tapped at every PFU. These secondary clock networks can also be used for controls and high fanout data. These secondary clocks are derived from four clock input pads and 16 routing signals as shown in Figure 2-6.

Table 2-6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

Figure 2-14 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{IL}, I_{IH}^{1,2,4}$	Input or I/O Leakage	$0 \leq V_{IN} \leq (V_{CCIO} - 0.2V)$	—	—	10	μA
		$(V_{CCIO} - 0.2V) < V_{IN} \leq 3.6V$	—	—	40	μA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7 V_{CCIO}$	-30	—	-150	μA
I_{PD}	I/O Active Pull-down Current	$V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MAX)$	30	—	150	μA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL} (MAX)$	30	—	—	μA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	-30	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	150	μA
I_{BHHO}	Bus Hold High Overdrive current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	-150	μA
V_{BHT}	Bus Hold trip Points	$0 \leq V_{IN} \leq V_{IH} (MAX)$	$V_{IL} (MAX)$	—	$V_{IH} (MIN)$	V
C1	I/O Capacitance ³	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,$ $V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—	8	—	pf
C2	Dedicated Input Capacitance ³	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,$ $V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—	8	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. Not applicable to SLEEPN/TOE pin.

3. $T_A = 25^\circ C$, $f = 1.0MHz$

4. When V_{IH} is higher than V_{CCIO} , a transient current typically of 30ns in duration or less with a peak current of 6mA can be expected on the high-to-low transition.

Supply Current (Sleep Mode)^{1, 2, 3}

Symbol	Parameter	Device	Typ. ⁴	Max	Units
I_{CC}	Core Power Supply	LFXP3C	12	65	μA
		LFXP6C	14	75	μA
		LFXP10C	16	85	μA
		LFXP15C	18	95	μA
		LFXP20C	20	105	μA
I_{CCP}	PLL Power Supply (per PLL)	All LFXP 'C' Devices	1	5	μA
I_{CCAUX}	Auxiliary Power Supply	LFXP3C	2	90	μA
		LFXP6C	2	100	μA
		LFXP10C	2	110	μA
		LFXP15C	3	120	μA
		LFXP20C	4	130	μA
I_{CCIO}	Bank Power Supply ⁵	LFXP3C	2	20	μA
		LFXP6C	2	22	μA
		LFXP10C	2	24	μA
		LFXP15C	3	27	μA
		LFXP20C	4	30	μA
I_{CCJ}	VCCJ Power Supply	All LFXP 'C' Devices	1	5	μA

1. Assumes all inputs are configured as LVCMOS and held at the VCCIO or GND.

2. Frequency 0MHz.

3. User pattern: blank.

4. $T_A = 25^\circ C$, power supplies at nominal voltage.

5. Per bank.

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

LVDS25E

The top and bottom side of LatticeXP devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

Figure 3-1. LVDS25E Output Termination Example

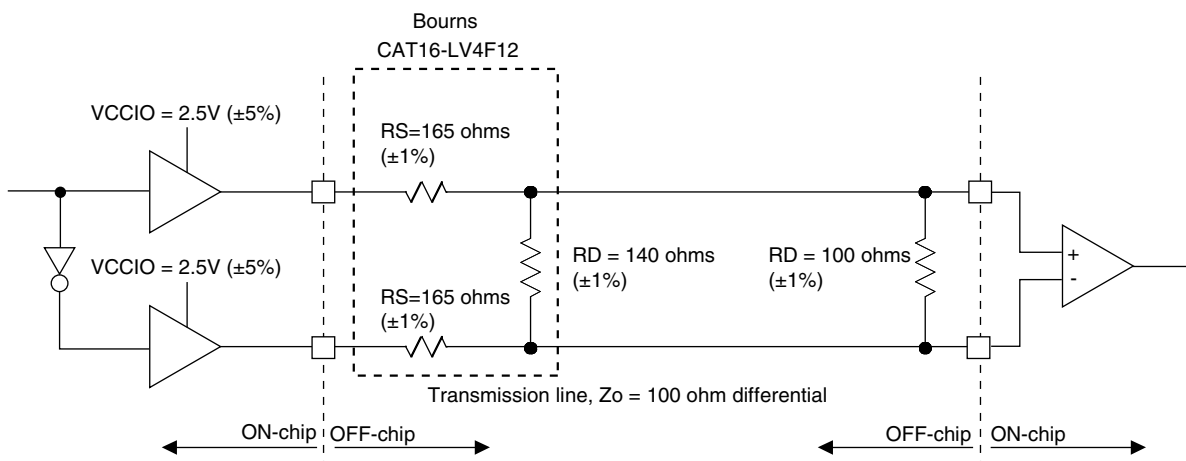


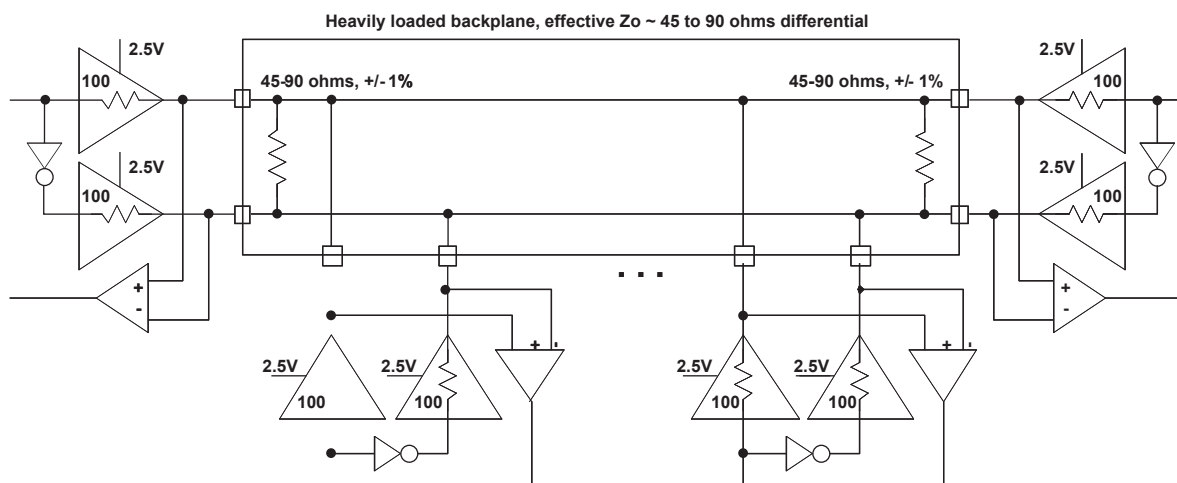
Table 3-1. LVDS25E DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100	ohms
I_{DC}	DC output current	3.66	mA

BLVDS

The LatticeXP devices support BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example**Table 3-2. BLVDS DC Conditions¹****Over Recommended Operating Conditions**

Symbol	Description	Typical		Units
		Zo = 45	Zo = 90	
Z _{OUT}	Output impedance	100	100	ohms
R _{TLEFT}	Left end termination	45	90	ohms
R _{TRIGHT}	Right end termination	45	90	ohms
V _{OH}	Output high voltage	1.375	1.48	V
V _{OL}	Output low voltage	1.125	1.02	V
V _{OD}	Output differential voltage	0.25	0.46	V
V _{CM}	Output common mode voltage	1.25	1.25	V
I _{DC}	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

[illegible]

Parameter	Description	Typical	Units
Z _{OUT}	Output impedance	20	ohms
R _S	Driver series resistor	300	ohms
R _P	Driver parallel resistor	121	ohms
R _T	Receiver termination	100	ohms
V _{OH}	Output high voltage	1.35	V
V _{OL}	Output low voltage	1.15	V
V _{OD}	Output differential voltage	0.20	V
V _{CM}	Output common mode voltage	1.25	V
Z _{BACK}	Back impedance	101.5	ohms
I _{DC}	DC output current	3.66	mA

PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO within PIC	Polarity	DDR Strobe (DQS) and Data (DQ) Pins
P[Edge] [n-4]	A	True	DQ
	B	Complement	DQ
P[Edge] [n-3]	A	True	DQ
	B	Complement	DQ
P[Edge] [n-2]	A	True	DQ
	B	Complement	DQ
P[Edge] [n-1]	A	True	DQ
P[Edge] [n]			
	B	Complement	DQ
P[Edge] [n+1]	A	True	[Edge]DQSn
	B	Complement	DQ
P[Edge] [n+2]	A	True	DQ
	B	Complement	DQ
P[Edge] [n+3]	A	True	DQ
	B	Complement	DQ

Notes:

1. "n" is a row/column PIC number.
2. The DDR interface is designed for memories that support one DQS strobe per eight bits of data. In some packages, all the potential DDR data (DQ) pins may not be available.
3. The definition of the PIC numbering is provided in the Signal Names column of the Signal Descriptions table in this data sheet.

LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
47	PB11A	5	T	DQS	PB14A	5	T	DQS
48	PB11B	5	C	-	PB14B	5	C	-
49	VCCIO5	5	-	-	VCCIO5	5	-	-
50	PB12A	5	T	-	PB15A	5	T	-
51	PB12B	5	C	-	PB15B	5	C	-
52	PB13A	5	T	-	PB16A	5	T	-
53	PB13B	5	C	-	PB16B	5	C	-
54	GND	-	-	-	GND	-	-	-
55	PB14A	4	T	-	PB17A	4	T	-
56	GNDIO4	4	-	-	GNDIO4	4	-	-
57	PB14B	4	C	-	PB17B	4	C	-
58	PB15A	4	T	PCLKT4_0	PB18A	4	T	PCLKT4_0
59	PB15B	4	C	PCLKC4_0	PB18B	4	C	PCLKC4_0
60	PB16A	4	T	-	PB19A	4	T	-
61	VCCIO4	4	-	-	VCCIO4	4	-	-
62	PB16B	4	C	-	PB19B	4	C	-
63	PB19A	4	T	DQS	PB22A	4	T	DQS
64	GNDIO4	4	-	-	GNDIO4	4	-	-
65	PB19B	4	C	VREF1_4	PB22B	4	C	VREF1_4
66	PB20A	4	T	-	PB23A	4	T	-
67	PB20B	4	C	-	PB23B	4	C	-
68	VCCIO4	4	-	-	VCCIO4	4	-	-
69	PB22A	4	-	-	PB25A	4	-	-
70	PB24A	4	T	VREF2_4	PB27A	4	T	VREF2_4
71	PB24B	4	C	-	PB27B	4	C	-
72	PB25A	4	-	-	PB28A	4	-	-
73	VCC	-	-	-	VCC	-	-	-
74	PR18B	3	C ³	-	PR26B	3	C ³	-
75	GNDIO3	3	-	-	GNDIO3	3	-	-
76	PR18A	3	T ³	-	PR26A	3	T ³	-
77	PR17B	3	C	-	PR25B	3	C	-
78	PR17A	3	T	-	PR25A	3	T	-
79	PR16B	3	C ³	-	PR24B	3	C ³	-
80	PR16A	3	T ³	DQS	PR24A	3	T ³	DQS
81	PR15B	3	-	VREF1_3	PR23B	3	-	VREF1_3
82	PR14A	3	-	VREF2_3	PR22A	3	-	VREF2_3
83	PR13B	3	C	-	PR21B	3	C ³	-
84	PR13A	3	T	-	PR21A	3	T ³	-
85	GND	-	-	-	GND	-	-	-
86	PR12A	3	-	-	PR20A	3	-	-
87	PR11B	3	C	-	PR19B	3	C ³	-
88	VCCIO3	3	-	-	VCCIO3	3	-	-
89	PR11A	3	T	-	PR19A	3	T ³	-
90	GNDP1	-	-	-	GNDP1	-	-	-
91	VCCP1	-	-	-	VCCP1	-	-	-
92	PR9B	2	C	PCLKC2_0	PR12B	2	C	PCLKC2_0

LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
93	PR9A	2	T	PCLKT2_0	PR12A	2	T	PCLKT2_0
94	PR8B	2	C	RUM0_PLLC_IN_A	PR8B	2	C	RUM0_PLLC_IN_A
95	PR8A	2	T	RUM0_PLLT_IN_A	PR8A	2	T	RUM0_PLLT_IN_A
96	PR7B	2	C ³	-	PR7B	2	C ³	-
97	PR7A	2	T ³	DQS	PR7A	2	T ³	DQS
98	VCCIO2	2	-	-	VCCIO2	2	-	-
99	PR6B	2	-	VREF1_2	PR6B	2	-	VREF1_2
100	PR5A	2	-	VREF2_2	PR5A	2	-	VREF2_2
101	GNDIO2	2	-	-	GNDIO2	2	-	-
102	PR3B	2	C	RUM0_PLLC_FB_A	PR3B	2	C	RUM0_PLLC_FB_A
103	PR3A	2	T	RUM0_PLLT_FB_A	PR3A	2	T	RUM0_PLLT_FB_A
104	PR2B	2	C ³	-	PR2B	2	C ³	-
105	PR2A	2	T ³	-	PR2A	2	T ³	-
106	VCCAUX	-	-	-	VCCAUX	-	-	-
107	TDO	-	-	-	TDO	-	-	-
108	VCCJ	-	-	-	VCCJ	-	-	-
109	TDI	-	-	-	TDI	-	-	-
110	TMS	-	-	-	TMS	-	-	-
111	TCK	-	-	-	TCK	-	-	-
112	VCC	-	-	-	VCC	-	-	-
113	PT25A	1	-	VREF1_1	PT28A	1	-	VREF1_1
114	PT24A	1	-	-	PT27A	1	-	-
115	PT23A	1	-	D0	PT26A	1	-	D0
116	PT22B	1	C	D1	PT25B	1	C	D1
117	PT22A	1	T	VREF2_1	PT25A	1	T	VREF2_1
118	PT21A	1	-	D2	PT24A	1	-	D2
119	VCCIO1	1	-	-	VCCIO1	1	-	-
120	PT20B	1	-	D3	PT23B	1	-	D3
121	GNDIO1	1	-	-	GNDIO1	1	-	-
122	PT17A	1	-	D4	PT20A	1	-	D4
123	PT16A	1	-	D5	PT19A	1	-	D5
124	PT15B	1	C	D6	PT18B	1	C	D6
125	PT15A	1	T	-	PT18A	1	T	-
126	PT14B	1	-	D7	PT17B	1	-	D7
127	GND	-	-	-	GND	-	-	-
128	PT13B	0	C	BUSY	PT16B	0	C	BUSY
129	PT13A	0	T	CS1N	PT16A	0	T	CS1N
130	PT12B	0	C	PCLKC0_0	PT15B	0	C	PCLKC0_0
131	PT12A	0	T	PCLKT0_0	PT15A	0	T	PCLKT0_0
132	PT11B	0	C	-	PT14B	0	C	-
133	VCCIO0	0	-	-	VCCIO0	0	-	-
134	PT11A	0	T	DQS	PT14A	0	T	DQS
135	PT9A	0	-	DOUT	PT12A	0	-	DOUT
136	GNDIO0	0	-	-	GNDIO0	0	-	-
137	PT8A	0	-	WRITEN	PT11A	0	-	WRITEN
138	PT7A	0	-	VREF1_0	PT10A	0	-	VREF1_0

LFXP3 & LFXP6 Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
139	PT6A	0	-	DI	PT9A	0	-	DI
140	PT5A	0	-	CSN	PT8A	0	-	CSN
141	PT3B	0	-	VREF2_0	PT6B	0	-	VREF2_0
142	CFG0	0	-	-	CFG0	0	-	-
143	CFG1	0	-	-	CFG1	0	-	-
144	DONE	0	-	-	DONE	0	-	-

1. Applies to LFXP "C" only.
2. Applies to LFXP "E" only.
3. Supports dedicated LVDS outputs.

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
139	PR7A	2	T ³	DQS	PR7A	2	T ³	DQS
140	VCCIO2	2	-	-	VCCIO2	2	-	-
141	PR6B	2	-	VREF1_2	PR6B	2	-	VREF1_2
142	PR5A	2	-	VREF2_2	PR5A	2	-	VREF2_2
143	GNDIO2	2	-	-	GNDIO2	2	-	-
144	PR4B	2	C ³	-	PR4B	2	C ³	-
145	PR4A	2	T ³	-	PR4A	2	T ³	-
146	PR3B	2	C	RUM0_PLLC_FB_A	PR3B	2	C	RUM0_PLLC_FB_A
147	PR3A	2	T	RUM0_PLLT_FB_A	PR3A	2	T	RUM0_PLLT_FB_A
148	PR2B	2	C ³	-	PR2B	2	C ³	-
149	VCCIO2	2	-	-	VCCIO2	2	-	-
150	PR2A	2	T ³	-	PR2A	2	T ³	-
151	VCC	-	-	-	VCC	-	-	-
152	VCCAUX	-	-	-	VCCAUX	-	-	-
153	TDO	-	-	-	TDO	-	-	-
154	VCCJ	-	-	-	VCCJ	-	-	-
155	TDI	-	-	-	TDI	-	-	-
156	TMS	-	-	-	TMS	-	-	-
157	TCK	-	-	-	TCK	-	-	-
158	VCC	-	-	-	VCC	-	-	-
159	PT25A	1	-	VREF1_1	PT28A	1	-	VREF1_1
160	PT24B	1	C	-	PT27B	1	C	-
161	PT24A	1	T	-	PT27A	1	T	-
162	PT23A	1	-	D0	PT26A	1	-	D0
163	GNDIO1	1	-	-	GNDIO1	1	-	-
164	PT22B	1	C	D1	PT25B	1	C	D1
165	PT22A	1	T	VREF2_1	PT25A	1	T	VREF2_1
166	PT21A	1	-	D2	PT24A	1	-	D2
167	VCCIO1	1	-	-	VCCIO1	1	-	-
168	PT20B	1	C	D3	PT23B	1	C	D3
169	PT20A	1	T	-	PT23A	1	T	-
170	PT19B	1	C	-	PT22B	1	C	-
171	PT19A	1	T	DQS	PT22A	1	T	DQS
172	GNDIO1	1	-	-	GNDIO1	1	-	-
173	PT18B	1	-	-	PT21B	1	-	-
174	PT17A	1	-	D4	PT20A	1	-	D4
175	PT16B	1	C	-	PT19B	1	C	-
176	PT16A	1	T	D5	PT19A	1	T	D5
177	VCCIO1	1	-	-	VCCIO1	1	-	-
178	PT15B	1	C	D6	PT18B	1	C	D6
179	PT15A	1	T	-	PT18A	1	T	-
180	PT14B	1	-	D7	PT17B	1	-	D7
181	GND	-	-	-	GND	-	-	-
182	VCC	-	-	-	VCC	-	-	-
183	PT13B	0	C	BUSY	PT16B	0	C	BUSY
184	GNDIO0	0	-	-	GNDIO0	0	-	-

LFXP3 & LFXP6 Logic Signal Connections: 208 PQFP (Cont.)

Pin Number	LFXP3				LFXP6			
	Pin Function	Bank	Differential	Dual Function	Pin Function	Bank	Differential	Dual Function
185	PT13A	0	T	CS1N	PT16A	0	T	CS1N
186	PT12B	0	C	PCLKC0_0	PT15B	0	C	PCLKC0_0
187	PT12A	0	T	PCLKT0_0	PT15A	0	T	PCLKT0_0
188	PT11B	0	C	-	PT14B	0	C	-
189	VCCIO0	0	-	-	VCCIO0	0	-	-
190	PT11A	0	T	DQS	PT14A	0	T	DQS
191	PT10B	0	-	-	PT13B	0	-	-
192	PT9A	0	-	DOUT	PT12A	0	-	DOUT
193	PT8B	0	C	-	PT11B	0	C	-
194	GNDIO0	0	-	-	GNDIO0	0	-	-
195	PT8A	0	T	WRITEN	PT11A	0	T	WRITEN
196	PT7B	0	C	-	PT10B	0	C	-
197	PT7A	0	T	VREF1_0	PT10A	0	T	VREF1_0
198	PT6B	0	C	-	PT9B	0	C	-
199	VCCIO0	0	-	-	VCCIO0	0	-	-
200	PT6A	0	T	DI	PT9A	0	T	DI
201	PT5B	0	C	-	PT8B	0	C	-
202	PT5A	0	T	CSN	PT8A	0	T	CSN
203	PT4B	0	C	-	PT7B	0	C	-
204	PT4A	0	T	-	PT7A	0	T	-
205	PT3B	0	-	VREF2_0	PT6B	0	-	VREF2_0
206	PT2B	0	-	-	PT5B	0	-	-
207	GND	-	-	-	GND	-	-	-
208	CFG0	0	-	-	CFG0	0	-	-

1. Applies to LFXP "C" only.
2. Applies to LFXP "E" only.
3. Supports dedicated LVDS outputs.

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
F4	PROGRAMN	7	-	-	PROGRAMN	7	-	-	PROGRAMN	7	-	-
G4	CCLK	7	-	-	CCLK	7	-	-	CCLK	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
D2	PL2A	7	T ³	-	PL6A	7	T ³	-	PL6A	7	T ³	-
D1	PL2B	7	C ³	-	PL6B	7	C ³	-	PL6B	7	C ³	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
E2	PL3A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A
E3	PL3B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A
F3	PL4A	7	T ³	-	PL8A	7	T ³	-	PL8A	7	T ³	-
F2	PL4B	7	C ³	-	PL8B	7	C ³	-	PL8B	7	C ³	-
H4	PL5A	7	-	-	PL9A	7	-	-	PL9A	7	-	-
H3	PL6B	7	-	VREF1_7	PL10B	7	-	VREF1_7	PL10B	7	-	VREF1_7
G3	PL7A	7	T ³	DQS	PL11A	7	T ³	DQS	PL11A	7	T ³	DQS
G2	PL7B	7	C ³	-	PL11B	7	C ³	-	PL11B	7	C ³	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
F1	PL8A	7	T	-	PL12A	7	T	-	PL12A	7	T	-
E1	PL8B	7	C	-	PL12B	7	C	-	PL12B	7	C	-
J4	PL9A	7	T ³	-	PL13A	7	T ³	-	PL13A	7	T ³	-
K4	PL9B	7	C ³	-	PL13B	7	C ³	-	PL13B	7	C ³	-
G1	PL11A	7	T ³	-	PL15A	7	T ³	-	PL15A	7	T ³	-
H2	PL11B	7	C ³	-	PL15B	7	C ³	-	PL15B	7	C ³	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
J2	PL12A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A
H1	PL12B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A
J1	PL13A	7	T ³	-	PL17A	7	T ³	-	PL17A	7	T ³	-
K2	PL13B	7	C ³	-	PL17B	7	C ³	-	PL17B	7	C ³	-
K3	PL14A	7	-	VREF2_7	PL18A	7	-	VREF2_7	PL18A	7	-	VREF2_7
J3	PL15B	7	-	-	PL19B	7	-	-	PL19B	7	-	-
K1	PL16A	7	T ³	DQS	PL20A	7	T ³	DQS	PL20A	7	T ³	DQS
-	GNDIO7	7	-	-	GNDIO7	7	-	-	GNDIO7	7	-	-
L2	PL16B	7	C ³	-	PL20B	7	C ³	-	PL20B	7	C ³	-
L3	PL17A	7	T	-	PL21A	7	T	-	PL21A	7	T	-
L4	PL17B	7	C	-	PL21B	7	C	-	PL21B	7	C	-
L1	PL18A	7	T ³	-	PL22A	7	T ³	-	PL22A	7	T ³	-
M1	PL18B	7	C ³	-	PL22B	7	C ³	-	PL22B	7	C ³	-
M2	VCCP0	-	-	-	VCCP0	-	-	-	VCCP0	-	-	-
N1	GNDP0	-	-	-	GNDP0	-	-	-	GNDP0	-	-	-
M3	PL19A	6	T ³	-	PL23A	6	T ³	-	PL27A	6	T ³	-
M4	PL19B	6	C ³	-	PL23B	6	C ³	-	PL27B	6	C ³	-
P1	PL20A	6	T	PCLKT6_0	PL24A	6	T	PCLKT6_0	PL28A	6	T	PCLKT6_0
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
N2	PL20B	6	C	PCLKC6_0	PL24B	6	C	PCLKC6_0	PL28B	6	C	PCLKC6_0
R1	PL21A	6	T ³	-	PL25A	6	T ³	-	PL29A	6	T ³	-
P2	PL21B	6	C ³	-	PL25B	6	C ³	-	PL29B	6	C ³	-
N3	PL22A	6	-	-	PL26A	6	-	-	PL30A	6	-	-
N4	PL23B	6	-	VREF1_6	PL27B	6	-	VREF1_6	PL31B	6	-	VREF1_6
T1	PL24A	6	T ³	DQS	PL28A	6	T ³	DQS	PL32A	6	T ³	DQS
R2	PL24B	6	C ³	-	PL28B	6	C ³	-	PL32B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-

LFXP10, LFXP15 & LFXP20 Logic Signal Connections: 388 fpBGA (Cont.)

Ball Number	LFXP10				LFXP15				LFXP20			
	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function	Ball Function	Bank	Diff.	Dual Function
U1	PL25A	6	T	LLM0_PLLT_IN_A	PL29A	6	T	LLM0_PLLT_IN_A	PL33A	6	T	LLM0_PLLT_IN_A
T2	PL25B	6	C	LLM0_PLLC_IN_A	PL29B	6	C	LLM0_PLLC_IN_A	PL33B	6	C	LLM0_PLLC_IN_A
V1	PL26A	6	T ³	-	PL30A	6	T ³	-	PL34A	6	T ³	-
U2	PL26B	6	C ³	-	PL30B	6	C ³	-	PL34B	6	C ³	-
W1	PL28A	6	T ³	-	PL32A	6	T ³	-	PL36A	6	T ³	-
V2	PL28B	6	C ³	-	PL32B	6	C ³	-	PL36B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	-	-	-	GNDIO6	6	-	-
P3	PL29A	6	T	-	PL33A	6	T	-	PL37A	6	T	-
P4	PL29B	6	C	-	PL33B	6	C	-	PL37B	6	C	-
Y1	PL30A	6	T ³	-	PL34A	6	T ³	-	PL38A	6	T ³	-
W2	PL30B	6	C ³	-	PL34B	6	C ³	-	PL38B	6	C ³	-
R3	PL31A	6	-	VREF2_6	PL35A	6	-	VREF2_6	PL39A	6	-	VREF2_6
R4	PL32B	6	-	-	PL36B	6	-	-	PL40B	6	-	-
T3	PL33A	6	T ³	DQS	PL37A	6	T ³	DQS	PL41A	6	T ³	DQS
T4	PL33B	6	C ³	-	PL37B	6	C ³	-	PL41B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
V4	PL34A	6	T	LLM0_PLLT_FB_A	PL38A	6	T	LLM0_PLLT_FB_A	PL42A	6	T	LLM0_PLLT_FB_A
V3	PL34B	6	C	LLM0_PLLC_FB_A	PL38B	6	C	LLM0_PLLC_FB_A	PL42B	6	C	LLM0_PLLC_FB_A
U4	PL35A	6	T ³	-	PL39A	6	T ³	-	PL43A	6	T ³	-
U3	PL35B	6	C ³	-	PL39B	6	C ³	-	PL43B	6	C ³	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-	GNDIO6	6	-	-
W5	SLEEPN ¹ / TOE ²	-	-	-	SLEEPN ¹ / TOE ²	-	-	-	SLEEPN ¹ / TOE ²	-	-	-
Y2	INITN	5	-	-	INITN	5	-	-	INITN	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y3	-	-	-	-	PB3B	5	-	-	PB7B	5	-	-
W3	-	-	-	-	PB4A	5	T	-	PB8A	5	T	-
W4	-	-	-	-	PB4B	5	C	-	PB8B	5	C	-
AA2	-	-	-	-	PB5A	5	-	-	PB9A	5	-	-
AA1	-	-	-	-	PB6B	5	-	-	PB10B	5	-	-
W6	PB2A	5	-	-	PB7A	5	T	DQS	PB11A	5	T	DQS
W7	-	-	-	-	PB7B	5	C	-	PB11B	5	C	-
Y4	PB3A	5	T	-	PB8A	5	T	-	PB12A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
Y5	PB3B	5	C	-	PB8B	5	C	-	PB12B	5	C	-
AB2	PB4A	5	T	-	PB9A	5	T	-	PB13A	5	T	-
AA3	PB4B	5	C	-	PB9B	5	C	-	PB13B	5	C	-
AB3	PB5A	5	T	-	PB10A	5	T	-	PB14A	5	T	-
AA4	PB5B	5	C	-	PB10B	5	C	-	PB14B	5	C	-
W8	PB6A	5	T	-	PB11A	5	T	-	PB15A	5	T	-
W9	PB6B	5	C	-	PB11B	5	C	-	PB15B	5	C	-
AB4	PB7A	5	T	VREF1_5	PB12A	5	T	VREF1_5	PB16A	5	T	VREF1_5
-	GNDIO5	5	-	-	GNDIO5	5	-	-	GNDIO5	5	-	-
AA5	PB7B	5	C	-	PB12B	5	C	-	PB16B	5	C	-
AB5	PB8A	5	-	-	PB13A	5	-	-	PB17A	5	-	-
Y6	PB9B	5	-	-	PB14B	5	-	-	PB18B	5	-	-
AA6	PB10A	5	T	DQS	PB15A	5	T	DQS	PB19A	5	T	DQS
AB6	PB10B	5	C	-	PB15B	5	C	-	PB19B	5	C	-
Y9	PB11A	5	T	-	PB16A	5	T	-	PB20A	5	T	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
T6	PL41A	6	T	-	PL45A	6	T	-
T5	PL41B	6	C	-	PL45B	6	C	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
U3	PL42A	6	T ³	-	PL46A	6	T ³	-
U4	PL42B	6	C ³	-	PL46B	6	C ³	-
V4	PL43A	6	-	-	PL47A	6	-	-
W4	SLEEPN ¹ / TOE ²	-	-	-	SLEEPN ¹ / TOE ²	-	-	-
W5	INITN	5	-	-	INITN	5	-	-
Y3	-	-	-	-	PB3B	5	-	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
U5	-	-	-	-	PB4A	5	T	-
V5	-	-	-	-	PB4B	5	C	-
Y4	-	-	-	-	PB5A	5	T	-
Y5	-	-	-	-	PB5B	5	C	-
V6	-	-	-	-	PB6A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
U6	-	-	-	-	PB6B	5	C	-
W6	PB3A	5	T	-	PB7A	5	T	-
Y6	PB3B	5	C	-	PB7B	5	C	-
AA2	PB4A	5	T	-	PB8A	5	T	-
AA3	PB4B	5	C	-	PB8B	5	C	-
V7	PB5A	5	-	-	PB9A	5	-	-
U7	PB6B	5	-	-	PB10B	5	-	-
Y7	PB7A	5	T	DQS	PB11A	5	T	DQS
W7	PB7B	5	C	-	PB11B	5	C	-
AA4	PB8A	5	T	-	PB12A	5	T	-
-	GNDIO5	5	-	-	GNDIO5	5	-	-
AA5	PB8B	5	C	-	PB12B	5	C	-
AB3	PB9A	5	T	-	PB13A	5	T	-
AB4	PB9B	5	C	-	PB13B	5	C	-
AA6	PB10A	5	T	-	PB14A	5	T	-
AA7	PB10B	5	C	-	PB14B	5	C	-
U8	PB11A	5	T	-	PB15A	5	T	-
V8	PB11B	5	C	-	PB15B	5	C	-
Y8	PB12A	5	T	VREF1_5	PB16A	5	T	VREF1_5
-	GNDIO5	5	-	-	GNDIO5	5	-	-
W8	PB12B	5	C	-	PB16B	5	C	-
V9	PB13A	5	-	-	PB17A	5	-	-
U9	PB14B	5	-	-	PB18B	5	-	-
Y9	PB15A	5	T	DQS	PB19A	5	T	DQS
W9	PB15B	5	C	-	PB19B	5	C	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
R18	PR38B	3	C	RLM0_PLLC_FB_A	PR42B	3	C	RLM0_PLLC_FB_A
R17	PR38A	3	T	RLM0_PLLT_FB_A	PR42A	3	T	RLM0_PLLT_FB_A
Y22	PR37B	3	C ³	-	PR41B	3	C ³	-
Y21	PR37A	3	T ³	DQS	PR41A	3	T ³	DQS
W22	PR36B	3	-	-	PR40B	3	-	-
W21	PR35A	3	-	VREF1_3	PR39A	3	-	VREF1_3
P17	PR34B	3	C ³	-	PR38B	3	C ³	-
P18	PR34A	3	T ³	-	PR38A	3	T ³	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
R19	PR33B	3	C	-	PR37B	3	C	-
R20	PR33A	3	T	-	PR37A	3	T	-
V22	PR32B	3	C ³	-	PR36B	3	C ³	-
V21	PR32A	3	T ³	-	PR36A	3	T ³	-
U22	PR30B	3	C ³	-	PR34B	3	C ³	-
U21	PR30A	3	T ³	-	PR34A	3	T ³	-
P19	PR29B	3	C	RLM0_PLLC_IN_A	PR33B	3	C	RLM0_PLLC_IN_A
P20	PR29A	3	T	RLM0_PLLT_IN_A	PR33A	3	T	RLM0_PLLT_IN_A
-	GNDIO3	3	-	-	GNDIO3	3	-	-
T22	PR28B	3	C ³	-	PR32B	3	C ³	-
T21	PR28A	3	T ³	DQS	PR32A	3	T ³	DQS
R22	PR27B	3	-	-	PR31B	3	-	-
R21	PR26A	3	-	VREF2_3	PR30A	3	-	VREF2_3
N19	PR25B	3	C ³	-	PR29B	3	C ³	-
N20	PR25A	3	T ³	-	PR29A	3	T ³	-
N18	PR24B	3	C	-	PR28B	3	C	-
M18	PR24A	3	T	-	PR28A	3	T	-
-	GNDIO3	3	-	-	GNDIO3	3	-	-
P22	PR23B	3	C ³	-	PR27B	3	C ³	-
P21	PR23A	3	T ³	-	PR27A	3	T ³	-
N22	-	-	-	-	PR26B	3	C ³	-
N21	-	-	-	-	PR26A	3	T ³	-
M19	-	-	-	-	PR25B	3	-	-
M20	GNDP1	-	-	-	GNDP1	-	-	-
L18	VCCP1	-	-	-	VCCP1	-	-	-
M21	-	-	-	-	PR24A	2	-	-
M22	PR22B	2	C ³	-	PR23B	2	C ³	-
L22	PR22A	2	T ³	-	PR23A	2	T ³	-
-	GNDIO2	2	-	-	GNDIO2	2	-	-
L19	-	-	-	-	PR22B	2	C ³	-
L20	-	-	-	-	PR22A	2	T ³	-
L21	PR21B	2	C	PCLKC2_0	PR21B	2	C	PCLKC2_0
K22	PR21A	2	T	PCLKT2_0	PR21A	2	T	PCLKT2_0

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
B3	PT8B	0	C	-	PT12B	0	C	-
A3	PT8A	0	T	-	PT12A	0	T	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
D7	PT7B	0	C	-	PT11B	0	C	-
C7	PT7A	0	T	DQS	PT11A	0	T	DQS
B2	PT6B	0	-	-	PT10B	0	-	-
C2	PT5A	0	-	-	PT9A	0	-	-
C3	PT4B	0	C	-	PT8B	0	C	-
D3	PT4A	0	T	-	PT8A	0	T	-
F7	PT3B	0	C	-	PT7B	0	C	-
E7	PT3A	0	T	-	PT7A	0	T	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
C6	-	-	-	-	PT6B	0	C	-
D6	-	-	-	-	PT6A	0	T	-
C5	-	-	-	-	PT5B	0	C	-
C4	-	-	-	-	PT5A	0	T	-
F6	-	-	-	-	PT4B	0	C	-
E6	-	-	-	-	PT4A	0	T	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
E4	-	-	-	-	PT3B	0	-	-
E5	CFG0	0	-	-	CFG0	0	-	-
D4	CFG1	0	-	-	CFG1	0	-	-
D5	DONE	0	-	-	DONE	0	-	-
A1	GND	-	-	-	GND	-	-	-
A2	GND	-	-	-	GND	-	-	-
A21	GND	-	-	-	GND	-	-	-
A22	GND	-	-	-	GND	-	-	-
AA1	GND	-	-	-	GND	-	-	-
AA22	GND	-	-	-	GND	-	-	-
AB1	GND	-	-	-	GND	-	-	-
AB2	GND	-	-	-	GND	-	-	-
AB21	GND	-	-	-	GND	-	-	-
AB22	GND	-	-	-	GND	-	-	-
B1	GND	-	-	-	GND	-	-	-
B22	GND	-	-	-	GND	-	-	-
H14	GND	-	-	-	GND	-	-	-
H9	GND	-	-	-	GND	-	-	-
J10	GND	-	-	-	GND	-	-	-
J11	GND	-	-	-	GND	-	-	-
J12	GND	-	-	-	GND	-	-	-
J13	GND	-	-	-	GND	-	-	-
J14	GND	-	-	-	GND	-	-	-

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
G9	VCC	-	-	-	VCC	-	-	-
H15	VCC	-	-	-	VCC	-	-	-
H8	VCC	-	-	-	VCC	-	-	-
J16	VCC	-	-	-	VCC	-	-	-
J7	VCC	-	-	-	VCC	-	-	-
K16	VCC	-	-	-	VCC	-	-	-
K17	VCC	-	-	-	VCC	-	-	-
K6	VCC	-	-	-	VCC	-	-	-
K7	VCC	-	-	-	VCC	-	-	-
N16	VCC	-	-	-	VCC	-	-	-
N17	VCC	-	-	-	VCC	-	-	-
N6	VCC	-	-	-	VCC	-	-	-
N7	VCC	-	-	-	VCC	-	-	-
P16	VCC	-	-	-	VCC	-	-	-
P7	VCC	-	-	-	VCC	-	-	-
R15	VCC	-	-	-	VCC	-	-	-
R8	VCC	-	-	-	VCC	-	-	-
T10	VCC	-	-	-	VCC	-	-	-
T13	VCC	-	-	-	VCC	-	-	-
T14	VCC	-	-	-	VCC	-	-	-
T9	VCC	-	-	-	VCC	-	-	-
U10	VCC	-	-	-	VCC	-	-	-
U13	VCC	-	-	-	VCC	-	-	-
G15	VCCAUX	-	-	-	VCCAUX	-	-	-
G16	VCCAUX	-	-	-	VCCAUX	-	-	-
G7	VCCAUX	-	-	-	VCCAUX	-	-	-
G8	VCCAUX	-	-	-	VCCAUX	-	-	-
H16	VCCAUX	-	-	-	VCCAUX	-	-	-
H7	VCCAUX	-	-	-	VCCAUX	-	-	-
R16	VCCAUX	-	-	-	VCCAUX	-	-	-
R7	VCCAUX	-	-	-	VCCAUX	-	-	-
T15	VCCAUX	-	-	-	VCCAUX	-	-	-
T16	VCCAUX	-	-	-	VCCAUX	-	-	-
T7	VCCAUX	-	-	-	VCCAUX	-	-	-
T8	VCCAUX	-	-	-	VCCAUX	-	-	-
F11	VCCIO0	0	-	-	VCCIO0	0	-	-
G11	VCCIO0	0	-	-	VCCIO0	0	-	-
H10	VCCIO0	0	-	-	VCCIO0	0	-	-
H11	VCCIO0	0	-	-	VCCIO0	0	-	-
F12	VCCIO1	1	-	-	VCCIO1	1	-	-
G12	VCCIO1	1	-	-	VCCIO1	1	-	-
H12	VCCIO1	1	-	-	VCCIO1	1	-	-

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following located on the Lattice website at www.latticesemi.com.

- Thermal Management document
- Technical Note TN1052 - Power Estimation and Management for LatticeECP/EC and LatticeXP Devices
- Power Calculator tool included with Lattice's ispLEVER design tool, or as a standalone download from www.latticesemi.com/software