Lattice Semiconductor Corporation - LFXP6E-4TN144C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6000
Total RAM Bits	73728
Number of I/O	100
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp6e-4tn144c

LatticeXP Family Data Sheet Introduction

July 2007 Data Sheet DS1001

Features

- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on – powers up in microseconds
  - No external configuration memory
  - Excellent design security, no bit stream to intercept
  - Reconfigure SRAM based logic in milliseconds
  - SRAM and non-volatile memory programmable through system configuration and JTAG ports
- **Sleep Mode**
  - Allows up to 1000x static current reduction
- **TransFR™ Reconfiguration (TFR)**
  - In-field logic update while system operates
- **Extensive Density and Package Options**
  - 3.1K to 19.7K LUT4s
  - 62 to 340 I/Os
  - Density migration supported
- **Embedded and Distributed Memory**
  - 54 Kbits to 396 Kbits sysMEM™ Embedded Block RAM
  - Up to 79 Kbits distributed RAM
  - Flexible memory resources:
    - Distributed and block memory
- **Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - SSTL 18 Class I
    - SSTL 3/2 Class I, II
    - HSTL15 Class I, III
    - HSTL 18 Class I, II, III
    - PCI
    - LVDS, Bus-LVDS, LVPECL, RSDS
- **Dedicated DDR Memory Support**
  - Implements interface up to DDR333 (166MHz)
- **sysCLOCK™ PLLs**
  - Up to 4 analog PLLs per device
  - Clock multiply, divide and phase shifting
- **System Level Support**
  - IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
  - Onboard oscillator for configuration
  - Devices operate with 3.3V, 2.5V, 1.8V or 1.2V power supply

Table 1-1. LatticeXP Family Selection Guide

Device	LFXP3	LFXP6	LFXP10	LFXP15	LFXP20
PFU/PFF Rows	16	24	32	40	44
PFU/PFF Columns	24	30	38	48	56
PFU/PFF (Total)	384	720	1216	1932	2464
LUTs (K)	3	6	10	15	20
Distributed RAM (KBits)	12	23	39	61	79
EBR SRAM (KBits)	54	72	216	324	396
EBR SRAM Blocks	6	8	24	36	44
V_{CC} Voltage	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V
PLLs	2	2	4	4	4
Max. I/O	136	188	244	300	340
Packages and I/O Combinations:					
100-pin TQFP (14 x 14 mm)	62				
144-pin TQFP (20 x 20 mm)	100	100			
208-pin PQFP (28 x 28 mm)	136	142			
256-ball fpBGA (17 x 17 mm)		188	188	188	188
388-ball fpBGA (23 x 23 mm)			244	268	268
484-ball fpBGA (23 x 23 mm)				300	340

Figure 2-8. Per Quadrant Secondary Clock Selection

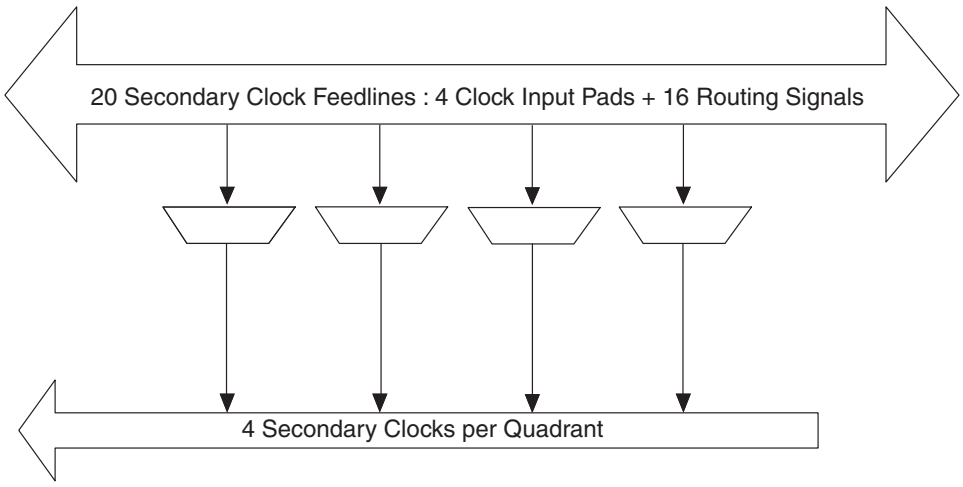
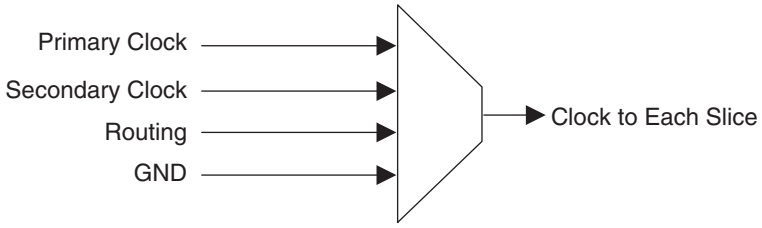


Figure 2-9. Slice Clock Selection



sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signals to the feedback divider: from CLKOP (PLL internal), from clock net (CLKOP or CLKOS) or from a user clock (PIN or logic). There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the t_{LOCK} parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved irrespective of where the select signal is toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-12 illustrates the DCS Block Macro.

Figure 2-12. DCS Block Primitive

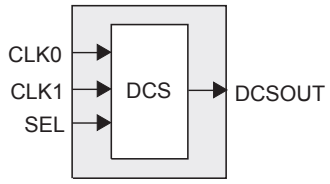
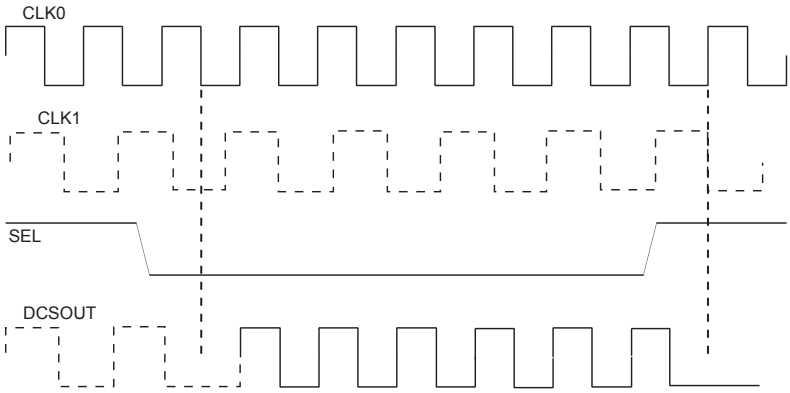


Figure 2-13 shows timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information on the DCS, please see details of additional technical documentation at the end of this data sheet.

Figure 2-13. DCS Waveforms



sysMEM Memory

The LatticeXP family of devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-6.

Figure 2-21. Input Register DDR Waveforms

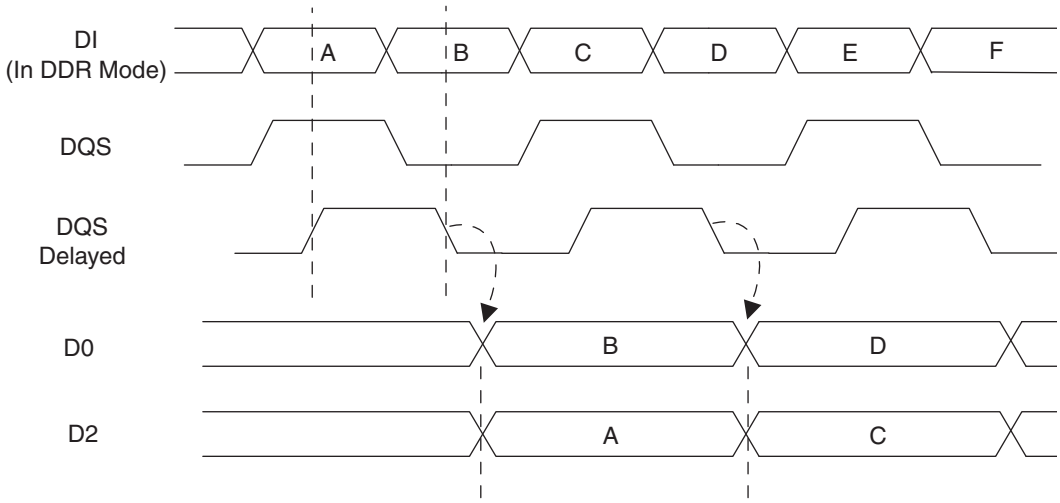
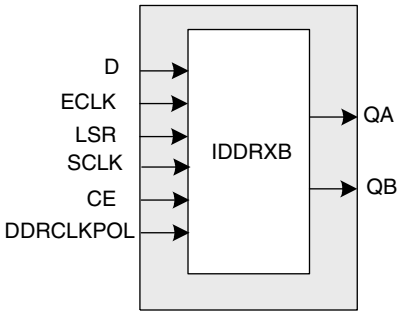


Figure 2-22. INDDRXB Primitive



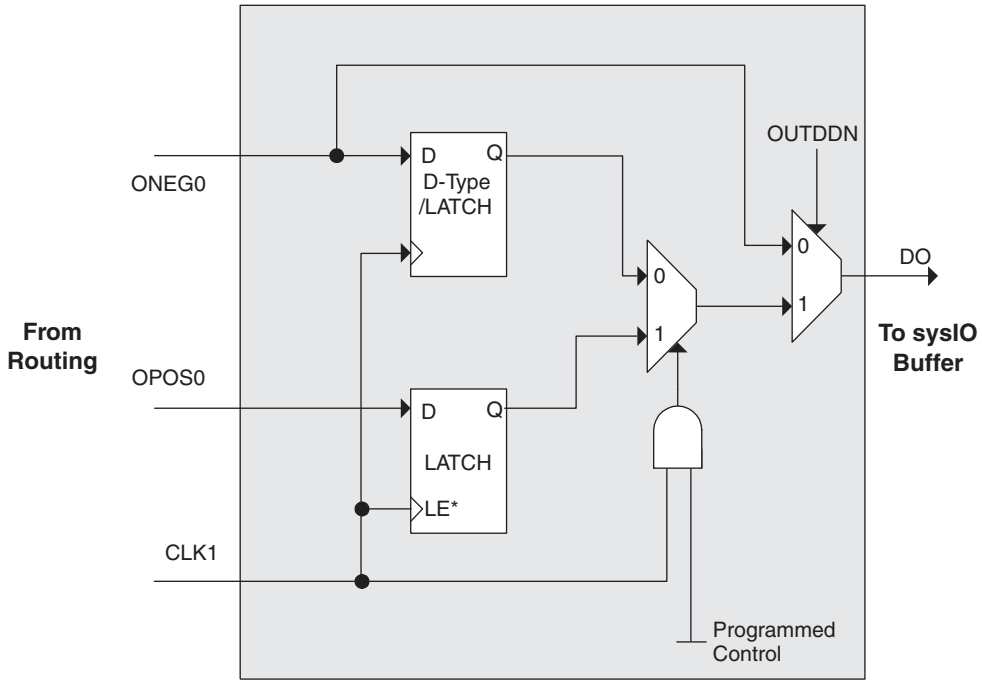
Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-23 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or as a latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

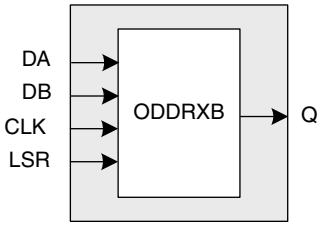
Figure 2-24 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

Figure 2-23. Output Register Block



*Latch is transparent when input is low.

Figure 2-24. ODDRXB Primitive



Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-25 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Table 2-8. Supported Output Standards

Output Standard	Drive	V_{CCIO} (Nom.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVCMOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVCMOS25	4mA, 8mA, 12mA 16mA, 20mA	2.5
LVCMOS18	4mA, 8mA, 12mA 16mA	1.8
LVCMOS15	4mA, 8mA	1.5
LVCMOS12	2mA, 6mA	1.2
LVCMOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVCMOS15, Open Drain	4mA, 8mA	—
LVCMOS12, Open Drain	2mA. 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II, III	N/A	1.8
HSTL15 Class I, III	N/A	1.5
SSTL3 Class I, II	N/A	3.3
SSTL2 Class I, II	N/A	2.5
SSTL18 Class I	N/A	1.8
Differential Interfaces		
Differential SSTL3, Class I, II	N/A	3.3
Differential SSTL2, Class I, II	N/A	2.5
Differential SSTL18, Class I	N/A	1.8
Differential HSTL18, Class I, II, III	N/A	1.8
Differential HSTL15, Class I, III	N/A	1.5
LVDS	N/A	2.5
BLVDS[1]	N/A	2.5
LVPECL[1]	N/A	3.3

1. Emulated with external resistors.

Hot Socketing

The LatticeXP devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits, which allows easy integration with the rest of the system. These capabilities make the LatticeXP ideal for many multiple power supply and hot-swap applications.

Sleep Mode

The LatticeXP "C" devices (V_{CC} = 1.8/2.5/3.3V) have a sleep mode that allows standby current to be reduced by up to three orders of magnitude during periods of system inactivity. Entry and exit to Sleep Mode is controlled by the SLEEPN pin.

During Sleep Mode, the FPGA logic is non-operational, registers and EBR contents are not maintained and I/Os are tri-stated. Do not enter Sleep Mode during device programming or configuration operation. In Sleep Mode, power supplies can be maintained in their normal operating range, eliminating the need for external switching of power supplies. Table 2-9 compares the characteristics of Normal, Off and Sleep Modes.

Hot Socketing Specifications[1, 2, 3, 4, 5, 6]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX.)	—	—	+/-1000	µA

1. Insensitive to sequence of V_{CC}, V_{CCAUX} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC}, V_{CCAUX} and V_{CCIO}.
2. $0 \le V_{CC} \le V_{CC}$ (MAX) or $0 \le V_{CCAUX} \le V_{CCAUX}$ (MAX).
3. $0 \le V_{CCIO} \le V_{CCIO}$ (MAX) for top and bottom I/O banks.
4. $0.2 \le V_{CCIO} \le V_{CCIO}$ (MAX) for left and right I/O banks.
5. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.
6. LVCMOS and LVTTL only.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 2, 4]	Input or I/O Leakage	$0 \le V_{IN} \le (V_{CCIO} - 0.2V)$	—	—	10	µA
		$(V_{CCIO} - 0.2V) < V_{IN} \le 3.6V$	—	—	40	µA
I_{PU}	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7\ V_{CCIO}$	-30	—	-150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	-150	µA
V_{BHT}	Bus Hold trip Points	$0 \le V_{IN} \le V_{IH}$ (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[3]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Dedicated Input Capacitance[3]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. Not applicable to SLEEPN/TOE pin.
3. T_A 25°C, f = 1.0MHz
4. When V_{IH} is higher than V_{CCIO}, a transient current typically of 30ns in duration or less with a peak current of 6mA can be expected on the high-to-low transition.

Supply Current (Sleep Mode)[1, 2, 3]

Symbol	Parameter	Device	Typ.[4]	Max	Units
I_{CC}	Core Power Supply	LFXP3C	12	65	µA
		LFXP6C	14	75	µA
		LFXP10C	16	85	µA
		LFXP15C	18	95	µA
		LFXP20C	20	105	µA
I_{CCP}	PLL Power Supply (per PLL)	All LFXP 'C' Devices	1	5	µA
I_{CCAUX}	Auxiliary Power Supply	LFXP3C	2	90	µA
		LFXP6C	2	100	µA
		LFXP10C	2	110	µA
		LFXP15C	3	120	µA
		LFXP20C	4	130	µA
I_{CCIO}	Bank Power Supply[5]	LFXP3C	2	20	µA
		LFXP6C	2	22	µA
		LFXP10C	2	24	µA
		LFXP15C	3	27	µA
		LFXP20C	4	30	µA
I_{CCJ}	VCCJ Power Supply	All LFXP 'C' Devices	1	5	µA

1. Assumes all inputs are configured as LVCMOS and held at the VCCIO or GND.
2. Frequency 0MHz.
3. User pattern: blank.
4. T_A=25°C, power supplies at nominal voltage.
5. Per bank.

sysIO Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.465	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
SSTL18 Class I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL2 Class I, II	2.375	2.5	2.625	1.15	1.25	1.35
SSTL3 Class I, II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15 Class I	1.425	1.5	1.575	0.68	0.75	0.9
HSTL15 Class III	1.425	1.5	1.575	—	0.9	—
HSTL 18 Class I, II	1.71	1.8	1.89	—	0.9	—
HSTL 18 Class III	1.71	1.8	1.89	—	1.08	—
LVDS	2.375	2.5	2.625	—	—	—
LVPECL[1]	3.135	3.3	3.465	—	—	—
BLVDS[1]	2.375	2.5	2.625	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.

Figure 3-2. BLVDS Multi-point Output Example

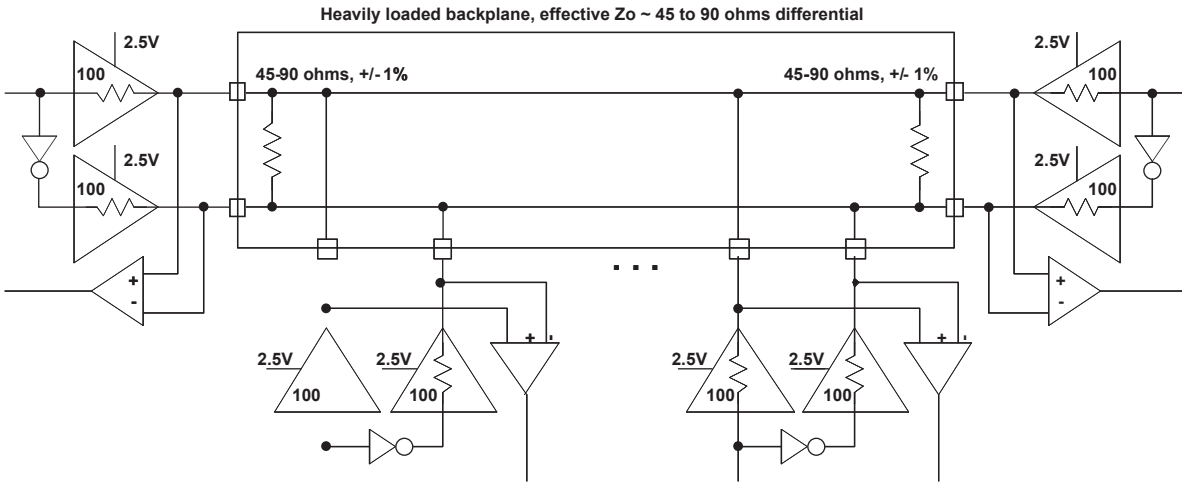


Table 3-2. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Typical		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	100	100	ohms
R_{TLEFT}	Left end termination	45	90	ohms
R_{TRIGHT}	Right end termination	45	90	ohms
V_{OH}	Output high voltage	1.375	1.48	V
V_{OL}	Output low voltage	1.125	1.02	V
V_{OD}	Output differential voltage	0.25	0.46	V
V_{CM}	Output common mode voltage	1.25	1.25	V
I_{DC}	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

LatticeXP External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Device	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (Using Primary Clock without PLL)[1]									
t_{CO}	Clock to Output - PIO Output Register	LFXP3	—	5.12	—	6.12	—	7.43	ns
		LFXP6	—	5.30	—	6.34	—	7.69	ns
		LFXP10	—	5.52	—	6.60	—	8.00	ns
		LFXP15	—	5.72	—	6.84	—	8.29	ns
		LFXP20	—	5.97	—	7.14	—	8.65	ns
t_{SU}	Clock to Data Setup - PIO Input Register	LFXP3	-0.40	—	-0.28	—	-0.16	—	ns
		LFXP6	-0.33	—	-0.32	—	-0.30	—	ns
		LFXP10	-0.61	—	-0.71	—	-0.81	—	ns
		LFXP15	-0.71	—	-0.77	—	-0.87	—	ns
		LFXP20	-0.95	—	-1.14	—	-1.35	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	LFXP3	2.10	—	2.50	—	2.98	—	ns
		LFXP6	2.28	—	2.72	—	3.24	—	ns
		LFXP10	3.02	—	3.51	—	3.71	—	ns
		LFXP15	2.70	—	3.22	—	3.85	—	ns
		LFXP20	2.95	—	3.52	—	4.21	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Input Data Delay	LFXP3	2.38	—	2.49	—	2.66	—	ns
		LFXP6	2.92	—	3.18	—	3.42	—	ns
		LFXP10	2.72	—	2.75	—	2.84	—	ns
		LFXP15	2.99	—	3.13	—	3.18	—	ns
		LFXP20	4.47	—	4.56	—	4.80	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFXP3	-0.70	—	-0.80	—	-0.92	—	ns
		LFXP6	-0.47	—	-0.38	—	-0.31	—	ns
		LFXP10	-0.60	—	-0.47	—	-0.32	—	ns
		LFXP15	-1.05	—	-0.98	—	-1.01	—	ns
		LFXP20	-0.80	—	-0.58	—	-0.31	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All	—	400	—	360	—	320	MHz
DDR I/O Pin Parameters[2]									
t_{DVADQ}	Data Valid After DQS (DDR Read)	All	—	0.19	—	0.19	—	0.19	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	All	0.67	—	0.67	—	0.67	—	UI
t_{DQVBS}	Data Valid Before DQS	All	0.20	—	0.20	—	0.20	—	UI
t_{DQVAS}	Data Valid After DQS	All	0.20	—	0.20	—	0.20	—	UI
f_{MAX_DDR}	DDR Clock Frequency	All	95	166	95	133	95	100	MHz
Primary and Secondary Clocks									
f_{MAX_PRI}	Frequency for Primary Clock Tree	All	—	450	—	412	—	375	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All	1.19	—	1.19	—	1.19	—	ns
t_{SKEW_PRI}	Primary Clock Skew within an I/O Bank	LFXP3/6/10/15	—	250	—	300	—	350	ps
		LFXP20	—	300	—	350	—	400	ps

1. General timing numbers based on LVCMOS 2.5, 12mA.
2. DDR timing numbers based on SSTL I/O.

Timing v.F0.11

LatticeXP Family Timing Adders[1] (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	-5	-4	-3	Units
HSTL15_I	HSTL_15 class I	0.2	0.2	0.2	ns
HSTL15_III	HSTL_15 class III	0.2	0.2	0.2	ns
HSTL15D_I	Differential HSTL 15 class I	0.2	0.2	0.2	ns
HSTL15D_III	Differential HSTL 15 class III	0.2	0.2	0.2	ns
SSTL33_I	SSTL_3 class I	0.1	0.1	0.1	ns
SSTL33_II	SSTL_3 class II	0.3	0.3	0.3	ns
SSTL33D_I	Differential SSTL_3 class I	0.1	0.1	0.1	ns
SSTL33D_II	Differential SSTL_3 class II	0.3	0.3	0.3	ns
SSTL25_I	SSTL_2 class I	-0.1	-0.1	-0.1	ns
SSTL25_II	SSTL_2 class II	0.3	0.3	0.3	ns
SSTL25D_I	Differential SSTL_2 class I	-0.1	-0.1	-0.1	ns
SSTL25D_II	Differential SSTL_2 class II	0.3	0.3	0.3	ns
SSTL18_I	SSTL_1.8 class I	0.1	0.1	0.1	ns
SSTL18D_I	Differential SSTL_1.8 class I	0.1	0.1	0.1	ns
LVTTL33_4mA	LVTTL 4mA drive	0.8	0.8	0.8	ns
LVTTL33_8mA	LVTTL 8mA drive	0.5	0.5	0.5	ns
LVTTL33_12mA	LVTTL 12mA drive	0.3	0.3	0.3	ns
LVTTL33_16mA	LVTTL 16mA drive	0.4	0.4	0.4	ns
LVTTL33_20mA	LVTTL 20mA drive	0.3	0.3	0.3	ns
LVCMOS33_2mA	LVCMOS 3.3 2mA drive	0.8	0.8	0.8	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive	0.8	0.8	0.8	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive	0.5	0.5	0.5	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive	0.3	0.3	0.3	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive	0.4	0.4	0.4	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive	0.3	0.3	0.3	ns
LVCMOS25_2mA	LVCMOS 2.5 2mA drive	0.7	0.7	0.7	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive	0.7	0.7	0.7	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive	0.4	0.4	0.4	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive	0.0	0.0	0.0	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive	0.2	0.2	0.2	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive	0.4	0.4	0.4	ns
LVCMOS18_2mA	LVCMOS 1.8 2mA drive	0.6	0.6	0.6	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive	0.6	0.6	0.6	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive	0.4	0.4	0.4	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive	0.2	0.2	0.2	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive	0.2	0.2	0.2	ns
LVCMOS15_2mA	LVCMOS 1.5 2mA drive	0.6	0.6	0.6	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive	0.6	0.6	0.6	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive	0.2	0.2	0.2	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive	0.4	0.4	0.4	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive	0.4	0.4	0.4	ns
PCI33	PCI33	0.3	0.3	0.3	ns

1. General timing numbers based on LVCMOS 2.5, 12mA.

Timing v.F0.11

Pin Information Summary[1]

Pin Type		XP3			XP6		
		100 TQFP	144 TQFP	208 PQFP	144 TQFP	208 PQFP	256 fpBGA
Single Ended User I/O		62	100	136	100	142	188
Differential Pair User I/O[2]		19	35	56	35	58	80
Configuration	Dedicated	11	11	11	11	11	11
	Muxed	14	14	14	14	14	14
TAP		5	5	5	5	5	5
Dedicated (total without supplies)		6	6	6	6	6	6
V_{CC}		2	4	8	4	8	8
V_{CCAUX}		2	2	2	2	2	4
V_{CCPLL}		2	2	2	2	2	2
V_{CCIO}	Bank0	1	1	2	1	2	2
	Bank1	1	1	2	1	2	2
	Bank2	1	1	2	1	2	2
	Bank3	1	1	2	1	2	2
	Bank4	1	2	2	2	2	2
	Bank5	1	1	2	1	2	2
	Bank6	1	1	2	1	2	2
	Bank7	1	1	2	1	2	2
GND		10	13	24	13	24	24
GND_{PLL}		2	2	2	2	2	2
NC		0	0	6	0	0	0
Single Ended/Differential I/O per Bank[2]	Bank0	8/2	12/3	20/8	12/3	20/8	26/11
	Bank1	9/0	12/2	18/6	12/2	18/6	26/11
	Bank2	8/3	12/5	14/6	12/5	17/7	21/9
	Bank3	6/2	13/5	14/6	13/5	14/6	21/9
	Bank4	5/2	14/6	21/9	14/6	21/9	26/11
	Bank5	12/4	12/4	21/9	12/4	21/9	26/11
	Bank6	4/2	13/5	14/6	13/5	17/7	21/9
	Bank7	10/4	12/5	14/6	12/5	14/6	21/9
V_{CCJ}		1	1	1	1	1	1

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
2. The differential I/O per bank includes both dedicated LVDS and emulated LVDS pin pairs. Please see the Logic Signal Connections table for more information.

Pin Information Summary[1] (Cont.)

Pin Type		XP10		XP15			XP20		
		256 fpBGA	388 fpBGA	256 fpBGA	388 fpBGA	484 fpBGA	256 fpBGA	388 fpBGA	484 fpBGA
Single Ended User I/O		188	244	188	268	300	188	268	340
Differential Pair User I/O[2]		76	104	76	112	128	76	112	144
Configuration	Dedicated	11	11	11	11	11	11	11	11
	Muxed	14	14	14	14	14	14	14	14
TAP		5	5	5	5	5	5	5	5
Dedicated (total without supplies)		6	6	6	6	6	6	6	6
V_{CC}		8	14	8	14	28	8	14	28
V_{CCAUX}		4	4	4	4	12	4	4	12
V_{CCPLL}		2	2	2	2	2	2	2	2
V_{CCIO}	Bank0	2	5	2	5	4	2	5	4
	Bank1	2	5	2	5	4	2	5	4
	Bank2	2	4	2	4	4	2	4	4
	Bank3	2	4	2	4	4	2	4	4
	Bank4	2	5	2	5	4	2	5	4
	Bank5	2	5	2	5	4	2	5	4
	Bank6	2	4	2	4	4	2	4	4
	Bank7	2	4	2	4	4	2	4	4
GND		24	50	24	50	56	24	50	56
GND_{PLL}		2	2	2	2	2	2	2	2
NC		0	24	0	0	40	0	0	0
Single Ended/ Differential I/O per Bank[2]	Bank0	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank1	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank2	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank3	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank4	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank5	26/11	33/14	26/11	39/16	40/17	26/11	39/16	47/20
	Bank6	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
	Bank7	21/8	28/12	21/8	28/12	35/15	21/8	28/12	38/16
V_{CCJ}		1	1	1	1	1	1	1	1

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
2. The differential I/O per bank includes both dedicated LVDS and emulated LVDS pin pairs. Please see the Logic Signal Connections table for more information.

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
C2	PROGRAMN	7	-	-	PROGRAMN	7	-	-
C1	CCLK	7	-	-	CCLK	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
D2	PL7A	7	T	LUM0_PLLT_FB_A	PL7A	7	T	LUM0_PLLT_FB_A
D3	PL7B	7	C	LUM0_PLLC_FB_A	PL7B	7	C	LUM0_PLLC_FB_A
D1	PL9A	7	-	-	PL9A	7	-	-
E2	PL10B	7	-	VREF1_7	PL10B	7	-	VREF1_7
E1	PL11A	7	T[3]	DQS	PL11A	7	T[3]	DQS
F1	PL11B	7	C[3]	-	PL11B	7	C[3]	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
E3	PL12A	7	T	-	PL12A	7	T	-
F4	PL12B	7	C	-	PL12B	7	C	-
F3	PL13A	7	T[3]	-	PL13A	7	T[3]	-
F2	PL13B	7	C[3]	-	PL13B	7	C[3]	-
G1	PL15B	7	-	-	PL15B	7	-	-
-	GNDIO7	7	-	-	GNDIO7	7	-	-
G3	PL16A	7	T	LUM0_PLLT_IN_A	PL16A	7	T	LUM0_PLLT_IN_A
G2	PL16B	7	C	LUM0_PLLC_IN_A	PL16B	7	C	LUM0_PLLC_IN_A
H1	PL17A	7	T[3]	-	PL17A	7	T[3]	-
H2	PL17B	7	C[3]	-	PL17B	7	C[3]	-
G4	PL18A	7	-	VREF2_7	PL18A	7	-	VREF2_7
G5	PL19B	7	-	-	PL19B	7	-	-
J1	PL20A	7	T[3]	DQS	PL20A	7	T[3]	DQS
-	GNDIO7	7	-	-	GNDIO7	7	-	-
J2	PL20B	7	C[3]	-	PL20B	7	C[3]	-
H3	PL22A	7	T[3]	-	PL22A	7	T[3]	-
J3	PL22B	7	C[3]	-	PL22B	7	C[3]	-
H4	VCCP0	-	-	-	VCCP0	-	-	-
H5	GNDP0	-	-	-	GNDP0	-	-	-
K1	PL24A	6	T	PCLKT6_0	PL28A	6	T	PCLKT6_0
-	GNDIO6	6	-	-	GNDIO6	6	-	-
K2	PL24B	6	C	PCLKC6_0	PL28B	6	C	PCLKC6_0
J4	PL26A	6	-	-	PL30A	6	-	-
J5	PL27B	6	-	VREF1_6	PL31B	6	-	VREF1_6
L1	PL28A	6	T[3]	DQS	PL32A	6	T[3]	DQS
L2	PL28B	6	C[3]	-	PL32B	6	C[3]	-
-	GNDIO6	6	-	-	GNDIO6	6	-	-
M1	PL29A	6	T	LLM0_PLLT_IN_A	PL33A	6	T	LLM0_PLLT_IN_A
M2	PL29B	6	C	LLM0_PLLC_IN_A	PL33B	6	C	LLM0_PLLC_IN_A
K3	PL30A	6	T[3]	-	PL34A	6	T[3]	-
L3	PL30B	6	C[3]	-	PL34B	6	C[3]	-

LFXP15 & LFXP20 Logic Signal Connections: 256 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
-	GNDIO2	2	-	-	GNDIO2	2	-	-
F15	PR10B	2	-	-	PR10B	2	-	-
E15	PR9A	2	-	VREF2_2	PR9A	2	-	VREF2_2
F14	PR8B	2	C[3]	-	PR8B	2	C[3]	-
E14	PR8A	2	T[3]	-	PR8A	2	T[3]	-
D15	PR7B	2	C	RUM0_PLLC_FB_A	PR7B	2	C	RUM0_PLLC_FB_A
C15	PR7A	2	T	RUM0_PLLT_FB_A	PR7A	2	T	RUM0_PLLT_FB_A
-	GNDIO2	2	-	-	GNDIO2	2	-	-
E16	TDO	-	-	-	TDO	-	-	-
D16	VCCJ	-	-	-	VCCJ	-	-	-
D14	TDI	-	-	-	TDI	-	-	-
C14	TMS	-	-	-	TMS	-	-	-
B14	TCK	-	-	-	TCK	-	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
A15	PT40B	1	C	-	PT44B	1	C	-
B15	PT40A	1	T	-	PT44A	1	T	-
D12	PT39B	1	C	VREF1_1	PT43B	1	C	VREF1_1
-	GNDIO1	1	-	-	GNDIO1	1	-	-
C11	PT39A	1	T	DQS	PT43A	1	T	DQS
A14	PT38B	1	-	-	PT42B	1	-	-
B13	PT37A	1	-	-	PT41A	1	-	-
F12	PT36B	1	C	-	PT40B	1	C	-
E11	PT36A	1	T	-	PT40A	1	T	-
A13	PT35B	1	C	-	PT39B	1	C	-
C13	PT35A	1	T	D0	PT39A	1	T	D0
C10	PT34B	1	C	D1	PT38B	1	C	D1
E10	PT34A	1	T	VREF2_1	PT38A	1	T	VREF2_1
A12	PT33B	1	C	-	PT37B	1	C	-
B12	PT33A	1	T	D2	PT37A	1	T	D2
-	GNDIO1	1	-	-	GNDIO1	1	-	-
C12	PT32B	1	C	D3	PT36B	1	C	D3
A11	PT32A	1	T	-	PT36A	1	T	-
B11	PT31B	1	C	-	PT35B	1	C	-
D11	PT31A	1	T	DQS	PT35A	1	T	DQS
B9	PT30B	1	-	-	PT34B	1	-	-
D9	PT29A	1	-	D4	PT33A	1	-	D4
A10	PT28B	1	C	-	PT32B	1	C	-
B10	PT28A	1	T	D5	PT32A	1	T	D5
-	GNDIO1	1	-	-	GNDIO1	1	-	-
D10	PT27B	1	C	D6	PT31B	1	C	D6

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
D18	-	-	-	-	PT55B	1	C	-
E18	-	-	-	-	PT55A	1	T	-
C19	-	-	-	-	PT54B	1	C	-
C18	-	-	-	-	PT54A	1	T	-
C21	-	-	-	-	PT53B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B21	-	-	-	-	PT53A	1	T	-
E17	PT48B	1	C	-	PT52B	1	C	-
E16	PT48A	1	T	-	PT52A	1	T	-
C17	PT47B	1	C	-	PT51B	1	C	-
D17	PT47A	1	T	DQS	PT51A	1	T	DQS
F17	PT46B	1	-	-	PT50B	1	-	-
F16	PT45A	1	-	-	PT49A	1	-	-
C16	PT44B	1	C	-	PT48B	1	C	-
D16	PT44A	1	T	-	PT48A	1	T	-
A20	PT43B	1	C	-	PT47B	1	C	-
-	GNDIO1	1	-	-	GNDIO1	1	-	-
B20	PT43A	1	T	-	PT47A	1	T	-
A19	PT42B	1	C	-	PT46B	1	C	-
B19	PT42A	1	T	-	PT46A	1	T	-
C15	PT41B	1	C	-	PT45B	1	C	-
D15	PT41A	1	T	-	PT45A	1	T	-
A18	PT40B	1	C	-	PT44B	1	C	-
B18	PT40A	1	T	-	PT44A	1	T	-
F15	PT39B	1	C	VREF1_1	PT43B	1	C	VREF1_1
-	GNDIO1	1	-	-	GNDIO1	1	-	-
E15	PT39A	1	T	DQS	PT43A	1	T	DQS
A17	PT38B	1	-	-	PT42B	1	-	-
B17	PT37A	1	-	-	PT41A	1	-	-
E14	PT36B	1	C	-	PT40B	1	C	-
F14	PT36A	1	T	-	PT40A	1	T	-
D14	PT35B	1	C	-	PT39B	1	C	-
C14	PT35A	1	T	D0	PT39A	1	T	D0
A16	PT34B	1	C	D1	PT38B	1	C	D1
B16	PT34A	1	T	VREF2_1	PT38A	1	T	VREF2_1
A15	PT33B	1	C	-	PT37B	1	C	-
B15	PT33A	1	T	D2	PT37A	1	T	D2
-	GNDIO1	1	-	-	GNDIO1	1	-	-
E13	PT32B	1	C	D3	PT36B	1	C	D3
D13	PT32A	1	T	-	PT36A	1	T	-
C13	PT31B	1	C	-	PT35B	1	C	-
B13	PT31A	1	T	DQS	PT35A	1	T	DQS

LFXP15 & LFXP20 Logic Signal Connections: 484 fpBGA (Cont.)

Ball Number	LFXP15				LFXP20			
	Ball Function	Bank	Differential	Dual Function	Ball Function	Bank	Differential	Dual Function
B3	PT8B	0	C	-	PT12B	0	C	-
A3	PT8A	0	T	-	PT12A	0	T	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
D7	PT7B	0	C	-	PT11B	0	C	-
C7	PT7A	0	T	DQS	PT11A	0	T	DQS
B2	PT6B	0	-	-	PT10B	0	-	-
C2	PT5A	0	-	-	PT9A	0	-	-
C3	PT4B	0	C	-	PT8B	0	C	-
D3	PT4A	0	T	-	PT8A	0	T	-
F7	PT3B	0	C	-	PT7B	0	C	-
E7	PT3A	0	T	-	PT7A	0	T	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
C6	-	-	-	-	PT6B	0	C	-
D6	-	-	-	-	PT6A	0	T	-
C5	-	-	-	-	PT5B	0	C	-
C4	-	-	-	-	PT5A	0	T	-
F6	-	-	-	-	PT4B	0	C	-
E6	-	-	-	-	PT4A	0	T	-
-	GNDIO0	0	-	-	GNDIO0	0	-	-
E4	-	-	-	-	PT3B	0	-	-
E5	CFG0	0	-	-	CFG0	0	-	-
D4	CFG1	0	-	-	CFG1	0	-	-
D5	DONE	0	-	-	DONE	0	-	-
A1	GND	-	-	-	GND	-	-	-
A2	GND	-	-	-	GND	-	-	-
A21	GND	-	-	-	GND	-	-	-
A22	GND	-	-	-	GND	-	-	-
AA1	GND	-	-	-	GND	-	-	-
AA22	GND	-	-	-	GND	-	-	-
AB1	GND	-	-	-	GND	-	-	-
AB2	GND	-	-	-	GND	-	-	-
AB21	GND	-	-	-	GND	-	-	-
AB22	GND	-	-	-	GND	-	-	-
B1	GND	-	-	-	GND	-	-	-
B22	GND	-	-	-	GND	-	-	-
H14	GND	-	-	-	GND	-	-	-
H9	GND	-	-	-	GND	-	-	-
J10	GND	-	-	-	GND	-	-	-
J11	GND	-	-	-	GND	-	-	-
J12	GND	-	-	-	GND	-	-	-
J13	GND	-	-	-	GND	-	-	-
J14	GND	-	-	-	GND	-	-	-

LatticeXP Family Data Sheet Revision History

November 2007 **Data Sheet DS1001**

Revision History

Date	Version	Section	Change Summary
February 2005	01.0	—	Initial release.
April 2005	01.1	Architecture	EBR memory support section updated with clarification.
May 2005	01.2	Introduction	Added TransFR Reconfiguration to Features section.
		Architecture	Added TransFR section.
June 2005	01.3	Pinout Information	Added pinout information for LFXP3, LFXP6, LFXP15 and LFXP20.
July 2005	02.0	Introduction	Updated XP6, XP15 and XP20 EBR SRAM Bits and Block numbers.
		Architecture	Updated Per Quadrant Primary Clock Selection figure.
			Added Typical I/O Behavior During Power-up section.
			Updated Device Configuration section under Configuration and Testing.
		DC and Switching Characteristics	Clarified Hot Socketing Specification
			Updated Supply Current (Standby) Table
			Updated Initialization Supply Current Table
			Added Programming and Erase Flash Supply Current table
			Added LVDS Emulation section. Updated LVDS25E Output Termination Example figure and LVDS25E DC Conditions table.
			Updated Differential LVPECL diagram and LVPECL DC Conditions table.
			Deleted 5V Tolerant Input Buffer section. Updated RSDS figure and RSDS DC Conditions table.
			Updated sysCONFIG Port Timing Specifications
			Updated JTAG Port Timing Specifications. Added Flash Download Time table.
		Pinout Information	Updated Signal Descriptions table.
			Updated Logic Signal Connections Dual Function column.
		Ordering Information	Added lead-free ordering part numbers.
July 2005	02.1	DC and Switching Characteristics	Clarification of Flash Programming Junction Temperature
August 2005	02.2	Introduction	Added Sleep Mode feature.
		Architecture	Added Sleep Mode section.
		DC and Switching Characteristics	Added Sleep Mode Supply Current Table
			Added Sleep Mode Timing section
		Pinout Information	Added SLEEPN and TOE signal names, descriptions and footnotes.
			Added SLEEPN and TOE to pinout information and footnotes.
			Added footnote 3 to Logic Signal Connections tables for clarification on emulated LVDS output.
September 2005	03.0	Architecture	Added clarification of PCI clamp.
			Added clarification to SLEEPN Pin Characteristics section.
		DC and Switching Characteristics	DC Characteristics, added footnote 4 for clarification. Updated Supply Current (Sleep Mode), Supply Current (Standby), Initialization Supply Current, and Programming and Erase Flash Supply Current typical numbers.

Date	Version	Section	Change Summary
September 2005 (cont.)	03.0 (cont.)	DC and Switching Characteristics (cont.)	Updated Typical Building Block Function Performance timing numbers.
			Updated External Switching Characteristics timing numbers.
			Updated Internal Timing Parameters.
			Updated LatticeXP Family timing adders.
			Updated LatticeXP "C" Sleep Mode timing numbers.
			Updated JTAG Port Timing numbers.
		Pinout Information	Added clarification to SLEEPN and TOE description.
			Clarification of dedicated LVDS outputs.
		Supplemental Information	Updated list of technical notes.
September 2005	03.1	Pinout Information	Power Supply and NC Connections table corrected VCCP1 pin number for 208 PQFP.
December 2005	04.0	Introduction	Moved data sheet from Advance to Final.
		Architecture	Added clarification to Typical I/O Behavior During Power-up section.
		DC and Switching Characteristics	Added clarification to Recommended Operating Conditions.
			Updated timing numbers.
		Pinout Information	Updated Signal Descriptions table.
			Added clarification to Differential I/O Per Bank.
			Updated Differential dedicated LVDS output support.
		Ordering Information	Added 208 PQFP lead-free package and ordering part numbers.
February 2006	04.1	Pinout Information	Corrected description of Signal Names VREF1(x) and VREF2(x).
March 2006	04.2	DC and Switching Characteristics	Corrected condition for IIL and IIH.
March 2006	04.3	DC and Switching Characteristics	Added clarification to Recommended Operating Conditions for VCCAUX.
April 2006	04.4	Pinout Information	Removed Bank designator "5" from SLEEPN/TOE ball function.
May 2006	04.5	DC and Switching Characteristics	Added footnote 2 regarding threshold level for PROGRAMN to sysCONFIG Port Timing Specifications table.
June 2006	04.6	DC and Switching Characteristics	Corrected LVDS25E Output Termination Example.
August 2006	04.7	Architecture	Added clarification to Typical I/O Behavior During Power-Up section.
			Added clarification to Left and Right sysIO Buffer Pair section.
		DC and Switching Characteristics	Changes to LVDS25E Output Termination Example diagram.
December 2006	04.8	Architecture	EBR Asynchronous Reset section added.
February 2007	04.9	Architecture	Updated EBR Asynchronous Reset section.
July 2007	05.0	Introduction	Updated LatticeXP Family Selection Guide table.
		Architecture	Updated Typical I/O Behavior During Power-up text section.
		DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics table. Split out LVCMOS 1.2 by supply voltage.
November 2007	05.1	DC and Switching Characteristics	Added JTAG Port Timing Waveforms diagram.
		Pinout Information	Added Thermal Management text section.
		Supplemental Information	Updated title list.