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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8/300H
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, PWM, WDT
Number of I/O	70
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df3029f25wv

Section 5 Interrupt Controller

5.1 Overview

5.1.1 Features

The interrupt controller has the following features:

- Interrupt priority registers (IPRs) for setting interrupt priorities
  Interrupts other than NMI can be assigned to two priority levels on a module-by-module basis in interrupt priority registers A and B (IPRA and IPRB).
- Three-level masking by the I and UI bits in the CPU condition code register (CCR)
- Seven external interrupt pins
  NMI has the highest priority and is always accepted*; either the rising or falling edge can be selected. For each of IRQ_0 to IRQ_5, sensing of the falling edge or level sensing can be selected independently.

Note: * NMI input is sometimes disabled when flash memory is being programmed or erased. For details see section 18.4.5 Flash Vector Address Control Register (FVACR).

5.1.2 Block Diagram

Figure 5.1 shows a block diagram of the interrupt controller.

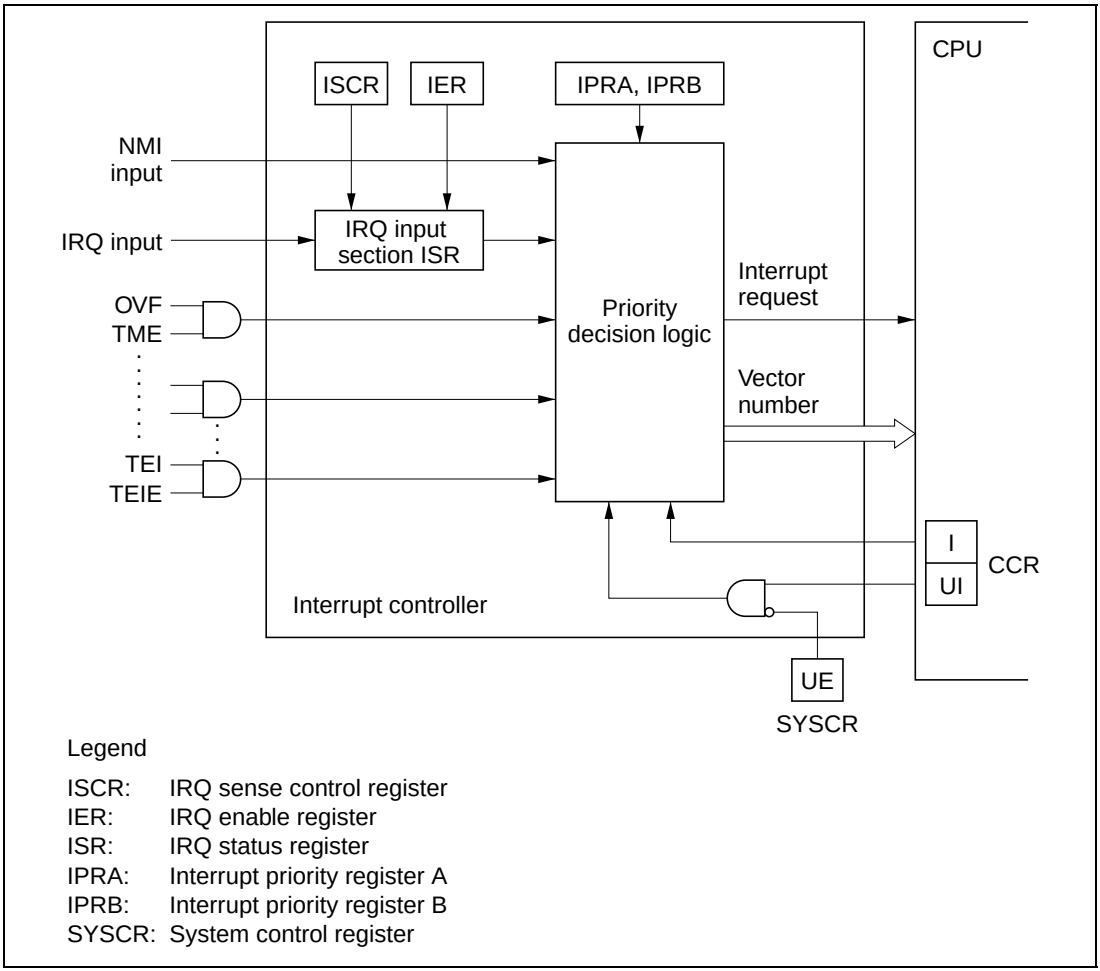


Figure 5.1 Interrupt Controller Block Diagram

5.2.3 IRQ Status Register (ISR)

ISR is an 8-bit readable/writable register that indicates the status of IRQ_0 to IRQ_5 interrupt requests.

Bit	7	6	5	4	3	2	1	0
	—	—	IRQ5F	IRQ4F	IRQ3F	IRQ2F	IRQ1F	IRQ0F
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Reserved bits

IRQ_5 to IRQ_0 flags
These bits indicate IRQ_5 to IRQ_0 interrupt request status

Note: * Only 0 can be written, to clear flags.

ISR is initialized to H'00 by a reset and in hardware standby mode.

Bits 7 and 6—Reserved: These bits can not be modified and are always read as 0.

Bits 5 to 0—IRQ_5 to IRQ_0 Flags (IRQ5F to IRQ0F): These bits indicate the status of IRQ_5 to IRQ_0 interrupt requests.

Bits 5 to 0 IRQ5F to IRQ0F	Description
0	[Clearing conditions] (Initial value) 0 is written in IRQnF after reading the IRQnF flag when IRQnF = 1. IRQnSC = 0, $\overline{\text{IRQn}}$ input is high, and interrupt exception handling is carried out. IRQnSC = 1 and IRQn interrupt exception handling is carried out.
1	[Setting conditions] IRQnSC = 0 and $\overline{\text{IRQn}}$ input is low. IRQnSC = 1 and $\overline{\text{IRQn}}$ input changes from high to low.

Note: n = 5 to 0

Bit 3—Reserved: This bit cannot be modified and is always read as 1.

Bit 2—TP Cycle Control (TPC): Selects whether a 1-state or two-state precharge cycle (T_p) is to be used for DRAM read/write cycles and CAS-before-RAS refresh cycles.

The setting of this bit does not affect the self-refresh function.

Bit 2 TPC	Description	
0	1-state precharge cycle inserted	(Initial value)
1	2-state precharge cycle inserted	

Bit 1—$\overline{\text{RAS}}$-$\overline{\text{CAS}}$ Wait (RCW): Controls wait state (Trw) insertion between T_r and T_{c1} in DRAM read/write cycles. The setting of this bit does not affect refresh cycles.

Bit 1 RCW	Description	
0	Wait state (Trw) insertion disabled	(Initial value)
1	One wait state (Trw) inserted	

Bit 0—Refresh Cycle Wait Control (RLW): Controls wait state (T_{RW}) insertion for CAS-before-RAS refresh cycles. The setting of this bit does not affect DRAM read/write cycles.

Bit 0 RLW	Description	
0	Wait state (T_{RW}) insertion disabled	(Initial value)
1	One wait state (T_{RW}) inserted	

6.2.9 Refresh Timer Control/Status Register (RTMCSR)

Bit	7	6	5	4	3	2	1	0
	CMF	CMIE	CKS2	CKS1	CKS0	—	—	—
Initial value	0	0	0	0	0	1	1	1
Read/Write	R(W)*	R/W	R/W	R/W	R/W	—	—	—

RTMCSR is an 8-bit readable/writable register that selects the refresh timer counter clock. When the refresh timer is used as an interval timer, RTMCSR also enables or disables interrupt requests. Bits 7 and 6 of RTMCSR are initialized to 0 by a reset and in the standby modes. Bits 5 to 3 are initialized to 0 by a reset and in hardware standby mode; they are not initialized in software standby mode.

Port 5 Data Register (P5DR): P5DR is an 8-bit readable/writable register that stores output data for port 5. When port 5 functions as an output port, the value of this register is output. When a bit in P5DDR is set to 1, if port 5 is read the value of the corresponding P5DR bit is returned. When a bit in P5DDR is cleared to 0, if port 5 is read the corresponding pin logic level is read.

Bits 7 to 4 are reserved. They are fixed at 1, and cannot be modified.

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	$P5_3$	$P5_2$	$P5_1$	$P5_0$
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Reserved bits

Port 5 data 3 to 0
These bits store data for port 5 pins

P5DR is initialized to H'F0 by a reset and in hardware standby mode. In software standby mode it retains its previous setting.

Port 5 Input Pull-Up MOS Control Register (P5PCR): P5PCR is an 8-bit readable/writable register that controls the MOS input pull-up transistors in port 5.

Bits 7 to 4 are reserved. They are fixed at 1, and cannot be modified.

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	$P5_3PCR$	$P5_2PCR$	$P5_1PCR$	$P5_0PCR$
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Reserved bits

Port 5 input pull-up control 3 to 0
These bits control input pull-up transistors built into port 5

In modes 5 and 7, when a P5DDR bit is cleared to 0 (selecting generic input), if the corresponding bit in P5PCR is set to 1, the input pull-up transistor is turned on.

P5PCR is initialized to H'F0 by a reset and in hardware standby mode. In software standby mode it retains its previous setting.

Table 8.9 summarizes the states of the input pull-ups in each mode.

Port B Data Register (PBDR): PBDR is an 8-bit readable/writable register that stores output data for pins port B. When port B functions as an output port, the value of this register is output. When a bit in PBDDR is set to 1, if port B is read the value of the corresponding PBDR bit is returned. When a bit in PBDDR is cleared to 0, if port B is read the corresponding pin logic level is read.

Bit	7	6	5	4	3	2	1	0
	PB_7	PB_6	PB_5	PB_4	PB_3	PB_2	PB_1	PB_0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Port B data 7 to 0
These bits store data for port B pins

PBDR is initialized to H'00 by a reset and in hardware standby mode. In software standby mode it retains its previous setting.

Pin	Pin Functions and Selection Method

$PB_1/TP_9/TMIO_1/\overline{DREQ}_0/\overline{CS}_6$

Bits OIS3/2 and OS1/0 in 8TCSR1, bits CCLR1 and CCLR0 in TCR1, bit CS6E in CSCR, bit NDER9 in NDERB, and bit PB_1DDR select the pin function as follows.

OIS3/2 and OS1/0	All 0				Not all 0
CS6E	0			1	—
PB_1DDR	0	1	1	—	—
NDER9	—	0	1	—	—
Pin function	PB_1 input	PB_1 output	TP_9 output	$\overline{CS}_6$ output	$TMIO_1$ output
	$TMIO_1$ input*1				
	$\overline{DREQ}_0$ input*2				

Notes: *1 $TMIO_1$ input when CCLR1 = CCLR0 = 1.

*2 When an external request is specified as a DMAC activation source, $\overline{DREQ}_0$ input regardless of bits OIS3/2 and OS1/0, bits CCLR1/0, bit CS6E, bit NDER9, and bit PB_1DDR.

$PB_0/TP_8/TMO_0/\overline{CS}_7$

Bits OIS3/2 and OS1/0 in 8TCSR0, bit CS7E in CSCR, bit NDER8 in NDERB, and bit PB_0DDR select the pin function as follows.

OIS3/2 and OS1/0	All 0				Not all 0
CS7E	0			1	—
PB_0DDR	0	1	1	—	—
NDER8	—	0	1	—	—
Pin function	PB_0 input	PB_0 output	TP_8 output	$\overline{CS}_7$ output	TMO_0 output

- Output triggering of programmable timing pattern controller (TPC)
  Compare match/input capture signals from channels 0 to 2 can be used as TPC output triggers.

Table 9.1 summarizes the 16-bit timer functions.

Table 9.1 16-bit timer Functions

Item		Channel 0	Channel 1	Channel 2
Clock sources		Internal clocks: φ, φ/2, φ/4, φ/8 External clocks: TCLKA, TCLKB, TCLKC, TCLKD, selectable independently		
General registers (output compare/input capture registers)		GRA0, GRB0	GRA1, GRB1	GRA2, GRB2
Input/output pins		$TIOCA_0$, $TIOCB_0$	$TIOCA_1$, $TIOCB_1$	$TIOCA_2$, $TIOCB_2$
Counter clearing function		GRA0/GRB0 compare match or input capture	GRA1/GRB1 compare match or input capture	GRA2/GRB2 compare match or input capture
Initial output value setting function		Available	Available	Available
Compare match output	0	Available	Available	Available
	1	Available	Available	Available
	Toggle	Available	Available	Not available
Input capture function		Available	Available	Available
Synchronization		Available	Available	Available
PWM mode		Available	Available	Available
Phase counting mode		Not available	Not available	Available
Interrupt sources		Three sources • Compare match/input capture A0 • Compare match/input capture B0 • Overflow	Three sources • Compare match/input capture A1 • Compare match/input capture B1 • Overflow	Three sources • Compare match/input capture A2 • Compare match/input capture B2 • Overflow

- 16TCNT count timing
  - — Internal clock source

    Bits TPSC2 to TPSC0 in 16TCR select the system clock (ϕ) or one of three internal clock sources obtained by prescaling the system clock (ϕ/2, ϕ/4, ϕ/8).
    Figure 9.15 shows the timing.

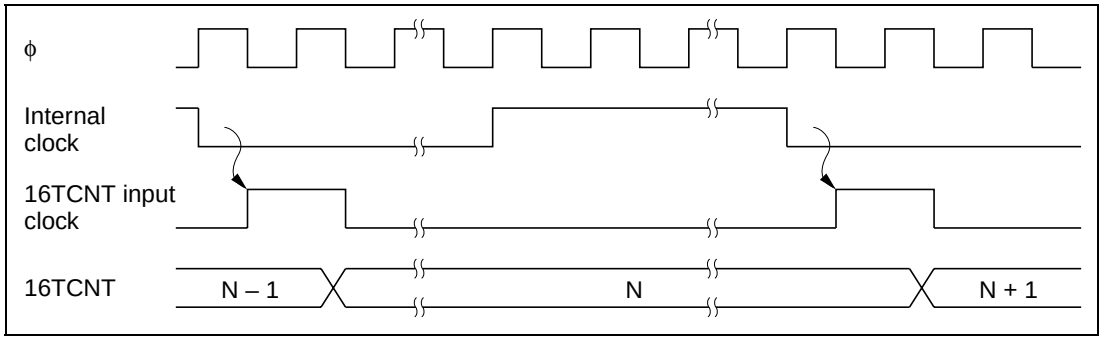


Figure 9.15 Count Timing for Internal Clock Sources

  - — External clock source

    The external clock pin (TCLKA to TCLKD) can be selected by bits TPSC2 to TPSC0 in 16TCR, and the detected edge by bits CKEG1 and CKEG0. The rising edge, falling edge, or both edges can be selected.

    The pulse width of the external clock signal must be at least 1.5 system clocks when a single edge is selected, and at least 2.5 system clocks when both edges are selected. Shorter pulses will not be counted correctly.

    Figure 9.16 shows the timing when both edges are detected.

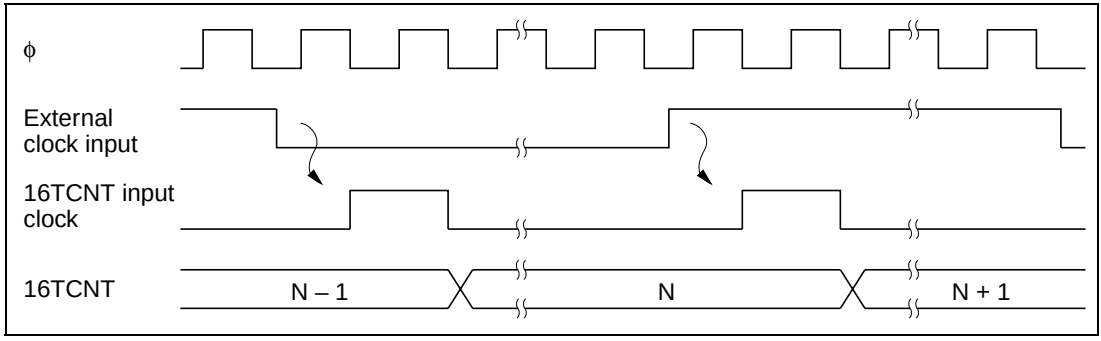


Figure 9.16 Count Timing for External Clock Sources (when Both Edges are Detected)

10.7.3 Contention between TCOR Write and Compare Match

If a compare match occurs in the T_3 state of a TCOR write cycle, writing takes priority and the compare match signal is inhibited. Figure 10.20 shows the timing in this case.

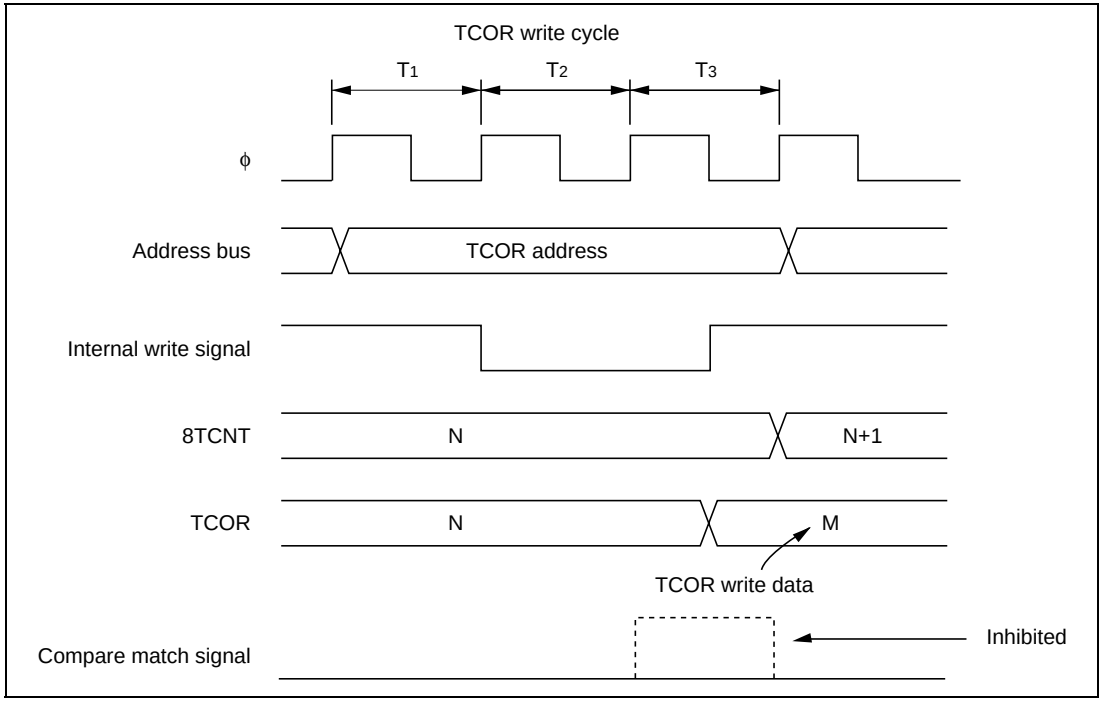
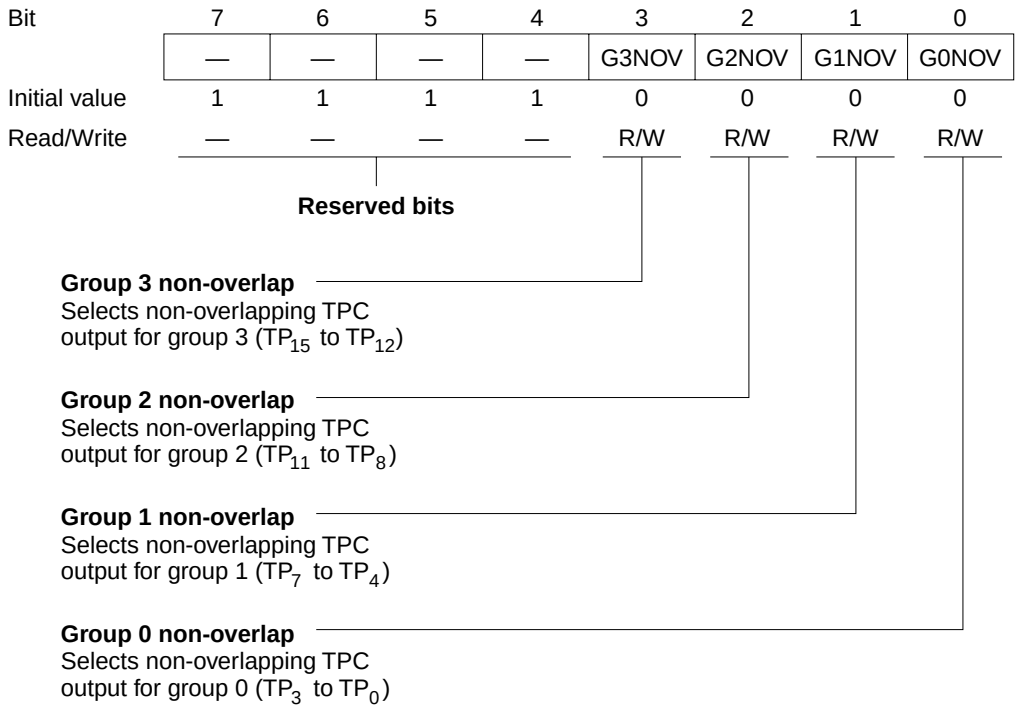


Figure 10.20 Contention between TCOR Write and Compare Match

11.2.10 TPC Output Mode Register (TPMR)

TPMR is an 8-bit readable/writable register that selects normal or non-overlapping TPC output for each group.



The output trigger period of a non-overlapping TPC output waveform is set in general register B (GRB) in the 16-bit timer channel selected for output triggering. The non-overlap margin is set in general register A (GRA). The output values change at compare match A and B. For details see section 11.3.4, Non-Overlapping TPC Output.

TPMR is initialized to H'F0 by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bits 7 to 4—Reserved: These bits cannot be modified and are always read as 1.

Writing to RSTCSR: RSTCSR must be written by a word transfer instruction. It cannot be written by byte transfer instructions. Figure 12.3 shows the format of data written to RSTCSR. To write 0 in the WRST bit, the write data must have H'A5 in the upper byte and H'00 in the lower byte. The data (H'00) in the lower byte is written to RSTCSR, clearing the WRST bit to 0.

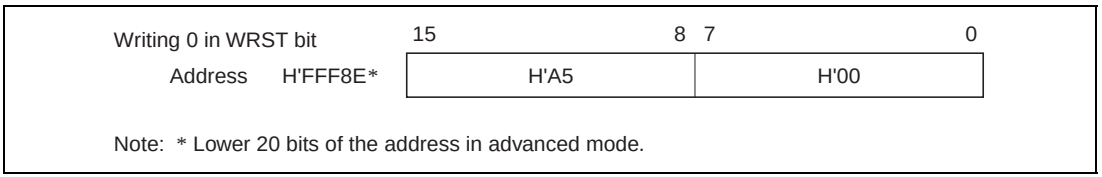


Figure 12.3 Format of Data Written to RSTCSR

Reading TCNT, TCSR, and RSTCSR: These registers are read like other registers. Reading TCNT, TCSR, and RSTCSR: These registers are read like other registers. Byte transfer instructions can be used. The read addresses are H'FFF8C for TCSR, H'FFF8D for TCNT, and H'FFF8F for RSTCSR, as listed in table 12.2.

Table 12.2 Read Addresses of TCNT, TCSR, and RSTCSR

Address*	Register
H'FFF8C	TCSR
H'FFF8D	TCNT
H'FFF8F	RSTCSR

Note: * Lower 20 bits of the address in advanced mode.

Bit 7—Transmit Data Register Empty (TDRE): Indicates that the SCI has loaded transmit data from TDR into TSR and the next serial data can be written in TDR.

Bit 7 TDRE	Description
0	TDR contains valid transmit data [Clearing conditions] Read TDRE when TDRE = 1, then write 0 in TDRE The DMAC writes data in TDR
1	TDR does not contain valid transmit data (Initial value) [Setting conditions] The chip is reset or enters standby mode The TE bit in SCR is cleared to 0 TDR contents are loaded into TSR, so new data can be written in TDR

Bit 6—Receive Data Register Full (RDRF): Indicates that RDR contains new receive data.

Bit 6 RDRF	Description
0	RDR does not contain new receive data (Initial value) [Clearing conditions] The chip is reset or enters standby mode Read RDRF when RDRF = 1, then write 0 in RDRF The DMAC reads data from RDR
1	RDR contains new receive data [Setting condition] Serial data is received normally and transferred from RSR to RDR

Note: The RDR contents and the RDRF flag are not affected by detection of receive errors or by clearing of the RE bit to 0 in SCR. They retain their previous values. If the RDRF flag is still set to 1 when reception of the next data ends, an overrun error will occur and the receive data will be lost.

Table 18.10 Software Protection

Item	Description	Function to be Protected	
		Download	Program/Erase
Protection by the SCO bit	• Clearing the SCO bit in the FCCS register makes the device enter a program/erase-protected state, and this disables the downloading of the programming/erasing programs.	○	○
Protection by the FKEY register	• Downloading and programming/erasing are disabled unless the required key code is written in the FKEY register. Different key codes are used for downloading and for programming/erasing.	○	○
Emulation protection	• Setting the RAMS bit in the RAM emulation register (RAMER) makes the device enter a program/erase-protected state.	○	○

18.6.3 Error Protection

Error protection is a mechanism for aborting programming or erasure when an error occurs, in the form of the microcomputer entering runaway during programming/erasing of the flash memory or operations that are not according to the established procedures for programming/erasing. Aborting programming or erasure in such cases prevents damage to the flash memory due to excessive programming or erasing.

If the microcomputer malfunctions during programming/erasing of the flash memory, the FLER bit in the FCCS register is set to 1 and the device enters the error-protection state, and this aborts the programming or erasure.

The FLER bit is set in the following conditions:

(1) When an interrupt, such as NMI, has occurred during programming/erasing

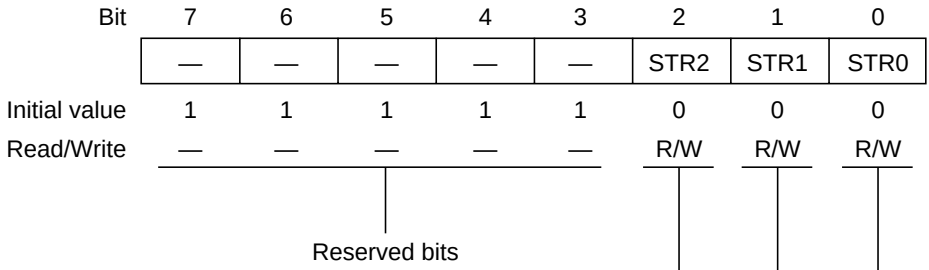
(2) When the relevant block area of flash memory is read during programming/erasing (including a vector read or an instruction fetch)

(3) When a SLEEP instruction (including software standby mode) is executed during programming/erasing

(4) When a bus master other than the CPU, such as DMAC or $\overline{\text{BREQ}}$, has obtained the bus right during programming/erasing

Address (Low)	Register Name	Data Bus Width	Bit Names								Module Name
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'EE0A0	—		—	—	—	—	—	—	—	—	
H'EE0A1	—		—	—	—	—	—	—	—	—	
H'EE0A2	—		—	—	—	—	—	—	—	—	
H'EE0A3	—		—	—	—	—	—	—	—	—	
H'EE0A4	—		—	—	—	—	—	—	—	—	
H'EE0A5	—		—	—	—	—	—	—	—	—	
H'EE0A6	—		—	—	—	—	—	—	—	—	
H'EE0A7	—		—	—	—	—	—	—	—	—	
H'EE0A8	—		—	—	—	—	—	—	—	—	
H'EE0A9	—		—	—	—	—	—	—	—	—	
H'EE0AA	—		—	—	—	—	—	—	—	—	
H'EE0AB	—		—	—	—	—	—	—	—	—	
H'EE0AC	—		—	—	—	—	—	—	—	—	
H'EE0AD	—		—	—	—	—	—	—	—	—	
H'EE0AE	—		—	—	—	—	—	—	—	—	
H'EE0AF	—		—	—	—	—	—	—	—	—	
H'EE0B0	FCCS	8	FWE	—	—	FLER	—	—	—	SCO	Flash memory*
H'EE0B1	FPCS	8	—	—	—	—	—	—	—	PPVS	
H'EE0B2	FECS	8	—	—	—	—	—	—	—	EPVB	
H'EE0B3	Reserved area (access prohibited)										
H'EE0B4	FKEY	8	K7	K6	K5	K4	K3	K2	K1	K0	
H'EE0B5	FMATS	8	MS7	MS6	MS5	MS4	MS3	MS2	MS1	MS0	
H'EE0B6	FTDAR	8	TDER	TDA6	TDA5	TDA4	TDA3	TDA2	TDA1	TDA0	
H'EE0B7	FVACR	8	FVCHGE	—	—	—	FVSEL3	FVSEL2	FVSEL1	FVSEL0	
H'EE0B8	FVADRR	8									
H'EE0B9	FVADRE	8									
H'EE0BA	FVADRH	8									
H'EE0BB	FVADRL	8									
H'EE0BC	Reserved area (access prohibited)										
H'EE0BD	—		—	—	—	—	—	—	—	—	
H'EE0BE	—		—	—	—	—	—	—	—	—	
H'EE0BF	—		—	—	—	—	—	—	—	—	

TSTR—Timer Start Register	H'FFF60	16-bit timer (all channels)



Counter start 0

0	TCNT0 is halted (Initial value)
1	TCNT0 is counting

Counter start 1

0	TCNT1 is halted (Initial value)
1	TCNT1 is counting

Counter start 2

0	TCNT2 is halted (Initial value)
1	TCNT2 is counting

Bit	7	6	5	4	3	2	1	0
	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock select

0	Conversion time = 134 states (maximum)
1	Conversion time = 70 states (maximum)

Channel select 2 to 0

Group Selection	Channel Selection		Description	
CH2	CH1	CH0	Single Mode	Scan Mode
0	0	0	AN_0	AN_0
		1	AN_1	AN_0, AN_1
	1	0	AN_2	AN_0 to AN_2
		1	AN_3	AN_0 to AN_3
1	0	0	AN_4	AN_4
		1	AN_5	AN_4, AN_5
	1	0	AN_6	AN_4 to AN_6
		1	AN_7	AN_4 to AN_7

Scan mode

0	Single mode
1	Scan mode

A/D start

0	A/D conversion is stopped
1	Single mode: A/D conversion starts; ADST is automatically cleared to 0 when conversion ends Scan mode: A/D conversion starts and continues, cycling among the selected channels ADST is cleared to 0 by software, by a reset, or by a transition to standby mode

A/D interrupt enable

0	A/D end interrupt request is disabled
1	A/D end interrupt request is enabled

A/D end flag

0	[Clearing conditions] Read ADF when ADF = 1, then write 0 in ADF The DMAC is activated by an ADI interrupt
1	[Setting conditions] Single mode: A/D conversion ends Scan mode: A/D conversion ends in all selected channels

Note: * Only 0 can be written, to clear the flag.

C.8 Port 8 Block Diagrams

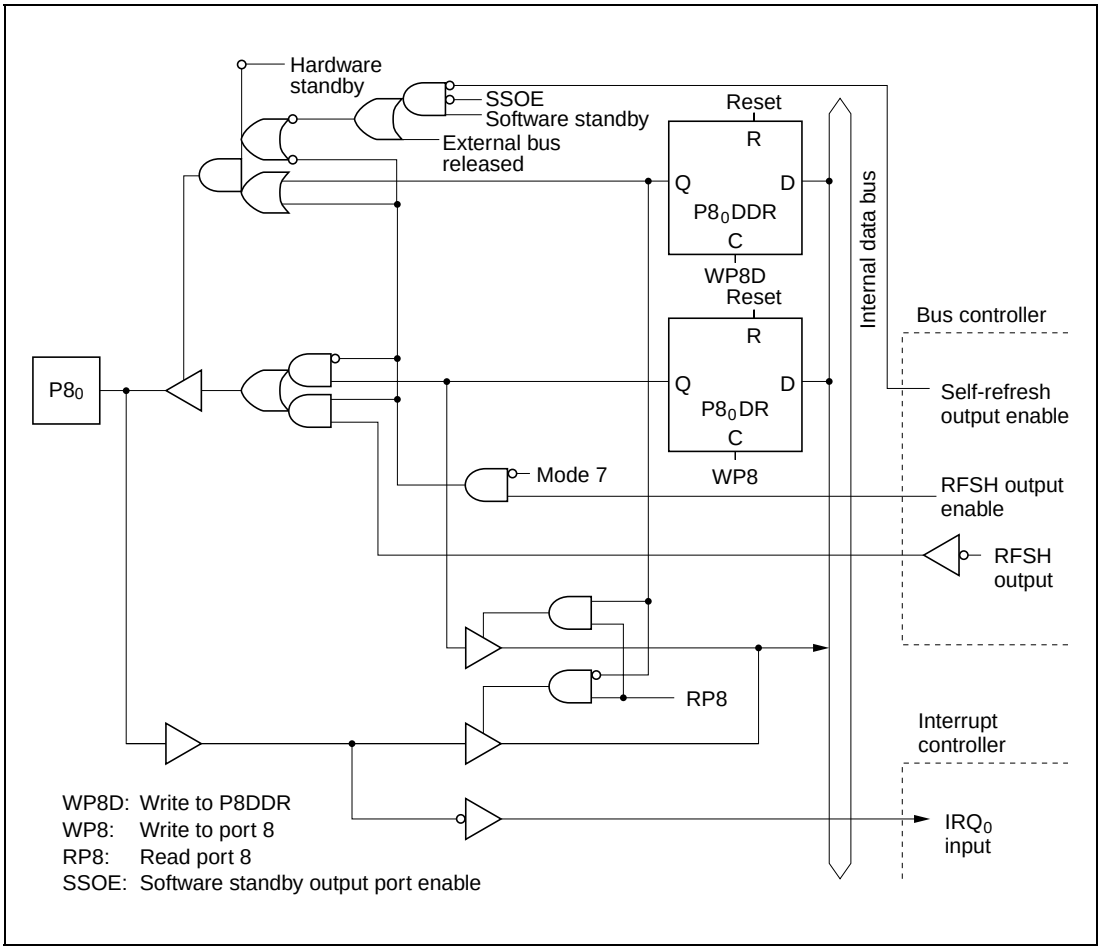


Figure C.8 (a) Port 8 Block Diagram (Pin P8$_0$)