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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 37 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 11x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303c6t6 |

- 96-bit unique ID
- All packages ECOPACK®2

**Table 1. Device summary**

| Reference | Part number |
|---|---|
| STM32F303x6 | STM32F303K6/C6/R6 |
| STM32F303x8 | STM32F303K8/C8/R8 |

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### 3.14.4 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### 3.14.5 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 3.14.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

## 3.15 Real-time clock (RTC) and backup registers

The RTC and the 5 backup registers are supplied through a switch that takes power from either the $V_{DD}$ supply when present or the VBAT pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when $V_{DD}$ power is not present.

They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be

woken up from Stop and Standby modes on timestamp event detection.

- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP/STANDBY capability.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

## 3.16 Communication interfaces

### 3.16.1 Inter-integrated circuit interface (I$^2$C)

The devices feature an I$^2$C bus interface which can operate in multimaster and slave mode. It can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes.

It supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). It also includes programmable analog and digital noise filters.

**Table 6. Comparison of I$^2$C analog and digital filters**

| - | Analog filter | Digital filter |
|---|---|---|
| Pulse width of suppressed spikes | ≥ 50 ns | Programmable length from 1 to 15 I$^2$C peripheral clocks |
| Benefits | Available in Stop mode | 1. Extra filtering capability vs. standard requirements.<br>2. Stable length |
| Drawbacks | Variations depending on temperature, voltage, process | Wakeup from Stop on address match is not available when digital filter is enabled. |

In addition, it provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. It also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I$^2$C interface can be served by the DMA controller.

The features available in I2C1 are showed below in *Table 7*.

**Table 7. STM32F303x6/8 I$^2$C implementation**

| I$^2$C features(1) | I2C1 |
|---|---|
| 7-bit addressing mode | X |
| 10-bit addressing mode | X |
| Standard mode (up to 100 kbit/s) | X |
| Fast mode (up to 400 kbit/s) | X |

### 3.16.3 Serial peripheral interface (SPI)

A SPI interface allows to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

The features available in SPI1 are showed below in *Table 9*.

**Table 9. STM32F303x6/8 SPI implementation**

| SPI features[(1)] | SPI1 |
|---|---|
| Hardware CRC calculation | X |
| Rx/Tx FIFO | X |
| NSS pulse mode | X |
| TI mode | X |

1. X = supported.

### 3.16.4 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

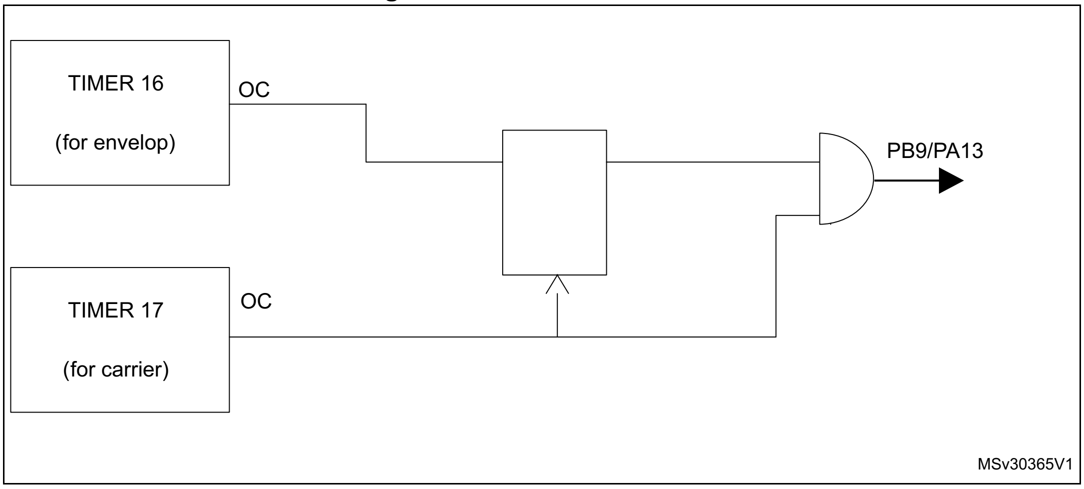
## 3.17 Infrared transmitter

The STM32F303x6/8 devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes is obtained by programming the two timers of the output compare channels (see *Figure 3*).

**Figure 3. Infrared transmitter**




## 3.18 Touch sensing controller (TSC)

The STM32F303x6/8 devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 18 capacitive sensing channels distributed over 6 analog I/Os group.

Capacitive sensing technology is able to detect the presence of a finger near an electrode which is protected from direct touch by a dielectric (glass, plastic,...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

**Table 10. Capacitive sensing GPIOs available on STM32F303x6/8 devices**

| Group | Capacitive sensing group name | Pin name |
|---|---|---|
| 1 | TSC_G1_IO1 | PA0 |
| | TSC_G1_IO2 | PA1 |
| | TSC_G1_IO3 | PA2 |
| | TSC_G1_IO4 | PA3 |
| 2 | TSC_G2_IO1 | PA4 |
| | TSC_G2_IO2 | PA5 |
| | TSC_G2_IO3 | PA6 |
| | TSC_G2_IO4 | PA7 |

**Table 14. STM32F303x6/8 pin definitions (continued)**

| Pin Number | | | Pin name (function after reset) | Pin type | I/O structure | Pin functions | |
|---|---|---|---|---|---|---|---|
| LQFP 32 | LQFP 48 | LQFP 64 | | | | Alternate functions | Additional functions |
| 3 | 6 | 6 | PF1 / OSC_OUT | I/O | FT | - | OSC_OUT |
| 4 | 7 | 7 | NRST | I/O | RST | Device reset input / internal reset output (active low) | |
| - | - | 8 | PC0 | I/O | TTa | EVENTOUT, TIM1_CH1 | ADC12_IN6 |
| - | - | 9 | PC1 | I/O | TTa | EVENTOUT, TIM1_CH2 | ADC12_IN7 |
| - | - | 10 | PC2 | I/O | TTa | EVENTOUT, TIM1_CH3 | ADC12_IN8 |
| - | - | 11 | PC3 | I/O | TTa | EVENTOUT, TIM1_CH4, TIM1_BKIN2 | ADC12_IN9 |
| - | 8 | 12 | VSSA/VREF- | S | - | Analog ground/Negative reference voltage | |
| 5 | 9 | 13 | VDDA/VREF+ | S | - | Analog power supply/Positive reference voltage | |
| 6 | 10 | 14 | PA0 | I/O | TTa | TIM2_CH1/ TIM2_ETR, TSC_G1_IO1, USART2_CTS, EVENTOUT | ADC1_IN1(2), RTC_TAMP2/WKUP1 |
| 7 | 11 | 15 | PA1 | I/O | TTa | TIM2_CH2, TSC_G1_IO2, USART2_RTS_DE, TIM15_CH1N, EVENTOUT | ADC1_IN2(2), RTC_REFIN |
| 8 | 12 | 16 | PA2 | I/O | TTa | TIM2_CH3, TSC_G1_IO3, USART2_TX, COMP2_OUT, TIM15_CH1, EVENTOUT | ADC1_IN3(2), COMP2_INM |
| 9 | 13 | 17 | PA3 | I/O | TTa | TIM2_CH4, TSC_G1_IO4, USART2_RX, TIM15_CH2, EVENTOUT | ADC1_IN4(2) |
| - | - | 18 | VSS | S | - | - | - |
| - | - | 19 | VDD | S | - | - | - |
| 10 | 14 | 20 | PA4(3) | I/O | TTa | TIM3_CH2, TSC_G2_IO1, SPI1_NSS, USART2_CK, EVENTOUT | ADC2_IN1(2), DAC1_OUT1, COMP2_INM4, COMP4_INM4, COMP6_INM4 |
| 11 | 15 | 21 | PA5(3) | I/O | TTa | TIM2_CH1/ TIM2_ETR, TSC_G2_IO2, SPI1_SCK, EVENTOUT | ADC2_IN2(2), DAC1_OUT2, OPAMP2_VINM |

Table 14. STM32F303x6/8 pin definitions (continued)

| Pin Number | | | Pin name (function after reset) | Pin type | I/O structure | Pin functions | |
|---|---|---|---|---|---|---|---|
| LQFP 32 | LQFP 48 | LQFP 64 | | | | Alternate functions | Additional functions |
| - | 28 | 36 | PB15 | I/O | TTa | TIM15_CH2, TIM15_CH1N, TIM1_CH3N, EVENTOUT | ADC2_IN15, COMP6_INM, RTC_REFIN |
| - | - | 37 | PC6 | I/O | FT | EVENTOUT, TIM3_CH1, COMP6_OUT | - |
| - | - | 38 | PC7 | I/O | FT | EVENTOUT, TIM3_CH2, | - |
| - | - | 39 | PC8 | I/O | FT | EVENTOUT, TIM3_CH3, | - |
| - | - | 40 | PC9 | I/O | FT | EVENTOUT, TIM3_CH4, | - |
| 18 | 29 | 41 | PA8 | I/O | FT | MCO, TIM1_CH1, USART1_CK, EVENTOUT | - |
| 19 | 30 | 42 | PA9 | I/O | FT | TSC_G4_IO1, TIM1_CH2, USART1_TX, TIM15_BKIN, TIM2_CH3, EVENTOUT | - |
| 20 | 31 | 43 | PA10 | I/O | FT | TIM17_BKIN, TSC_G4_IO2, TIM1_CH3, USART1_RX, COMP6_OUT, TIM2_CH4, EVENTOUT | - |
| 21 | 32 | 44 | PA11 | I/O | FT | TIM1_CH1N, USART1_CTS, CAN_RX, TIM1_CH4, TIM1_BKIN2, EVENTOUT | - |
| 22 | 33 | 45 | PA12 | I/O | FT | TIM16_CH1, TIM1_CH2N, USART1_RTS_DE, COMP2_OUT, CAN_TX, TIM1_ETR, EVENTOUT | - |
| 23 | 34 | 46 | PA13 | I/O | FT | JTMS/SWDAT, TIM16_CH1N, TSC_G4_IO3, IR_OUT, USART3_CTS, EVENTOUT | - |
| - | 35 | 47 | VSS | S | - | - | - |
| - | 36 | 48 | VDD | S | - | - | - |
| 24 | 37 | 49 | PA14 | I/O | FTf | JTCK/SWCLK, TSC_G4_IO4, I2C1_SDA, TIM1_BKIN, USART2_TX, EVENTOUT | - |

**Table 14. STM32F303x6/8 pin definitions (continued)**

| Pin Number | | | Pin name (function after reset) | Pin type | I/O structure | Pin functions | |
|---|---|---|---|---|---|---|---|
| LQFP 32 | LQFP 48 | LQFP 64 | | | | Alternate functions | Additional functions |
| 25 | 38 | 50 | PA15 | I/O | FTf | JTDI, TIM2_CH1/TIM2_ETR, TSC_SYNC, I2C1_SCL, SPI1_NSS, USART2_RX, TIM1_BKIN, EVENTOUT | - |
| - | - | 51 | PC10 | I/O | FT | EVENTOUT, USART3_TX | - |
| - | - | 52 | PC11 | I/O | FT | EVENTOUT, USART3_RX | - |
| - | - | 53 | PC12 | I/O | FT | EVENTOUT, USART3_CK | - |
| - | - | 54 | PD2 | I/O | FT | EVENTOUT, TIM3_ETR | - |
| 26 | 39 | 55 | PB3 | I/O | FT | JTDO/TRACE SWO, TIM2_CH2, TSC_G5_IO1, SPI1_SCK, USART2_TX, TIM3_ETR, EVENTOUT | - |
| 27 | 40 | 56 | PB4 | I/O | FT | NJTRST, TIM16_CH1, TIM3_CH1, TSC_G5_IO2, SPI1_MISO, USART2_RX, TIM17_BKIN, EVENTOUT | - |
| 28 | 41 | 57 | PB5 | I/O | FT | TIM16_BKIN, TIM3_CH2, I2C1_SMBA, SPI1_MOSI, USART2_CK, TIM17_CH1, EVENTOUT | - |
| 29 | 42 | 58 | PB6 | I/O | FTf | TIM16_CH1N, TSC_G5_IO3, I2C1_SCL, USART1_TX, EVENTOUT | - |
| 30 | 43 | 59 | PB7 | I/O | FTf | TIM17_CH1N, TSC_G5_IO4, I2C1_SDA, USART1_RX, TIM3_CH4, EVENTOUT | - |
| 31 | 44 | 60 | BOOT0 | I | B | - | - |
| - | 45 | 61 | PB8 | I/O | FTf | TIM16_CH1, TSC_SYNC, I2C1_SCL, USART3_RX, CAN_RX, TIM1_BKIN, EVENTOUT | - |

## 6.3 Operating conditions

### 6.3.1 General operating conditions

**Table 20. General operating conditions**

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | - | 0 | 72 | MHz |
| $f_{PCLK1}$ | Internal APB1 clock frequency | - | 0 | 36 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | - | 0 | 72 | |
| $V_{DD}$ | Standard operating voltage | - | 2 | 3.6 | V |
| $V_{DDA}$ | Analog operating voltage (OPAMP and DAC not used) | Must have a potential equal to or higher than $V_{DD}$ | 2 | 3.6 | |
| | Analog operating voltage (OPAMP and DAC used) | | 2.4 | 3.6 | |
| $V_{BAT}$ | Backup operating voltage | - | 1.65 | 3.6 | V |
| $V_{IN}$ | I/O input voltage | TC I/O | –0.3 | $V_{DD}$+0.3 | V |
| | | TT I/O | -0.3 | 3.6 | |
| | | TTa I/O | –0.3 | $V_{DDA}$+0.3 | |
| | | FT and FTf I/O(1) | –0.3 | 5.5 | |
| | | BOOT0 | 0 | 5.5 | |
| PD | Power dissipation at $T_A$ = 85 °C for suffix 6 or $T_A$ = 105 °C for suffix 7(2) | LQFP64 | - | 444 | mW |
| PD | Power dissipation at $T_A$ = 85 °C for suffix 6 or $T_A$ = 105 °C for suffix 7(3) | LQFP48 | - | 364 | mW |
| TA | Ambient temperature for 6 suffix version | Maximum power dissipation | –40 | 85 | °C |
| | | Low power dissipation(4) | –40 | 105 | |
| | Ambient temperature for 7 suffix version | Maximum power dissipation | –40 | 105 | °C |
| | | Low power dissipation(4) | –40 | 125 | |
| TJ | Junction temperature range | 6 suffix version | –40 | 105 | °C |
| | | 7 suffix version | –40 | 125 | |

1. To sustain a voltage higher than $V_{DD}$+0.3 V, the internal pull-up/pull-down resistors must be disabled.
2. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_{Jmax}$ (see *Section 7.5: Thermal characteristics*).
3. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_{Jmax}$ (see *Section 7.5: Thermal characteristics*).
4. In low power dissipation state, $T_A$ can be extended to this range as long as $T_J$ does not exceed $T_{Jmax}$ (see *Section 7.5: Thermal characteristics*).

**Figure 19. TC and TTa I/O input characteristics - TTL port**

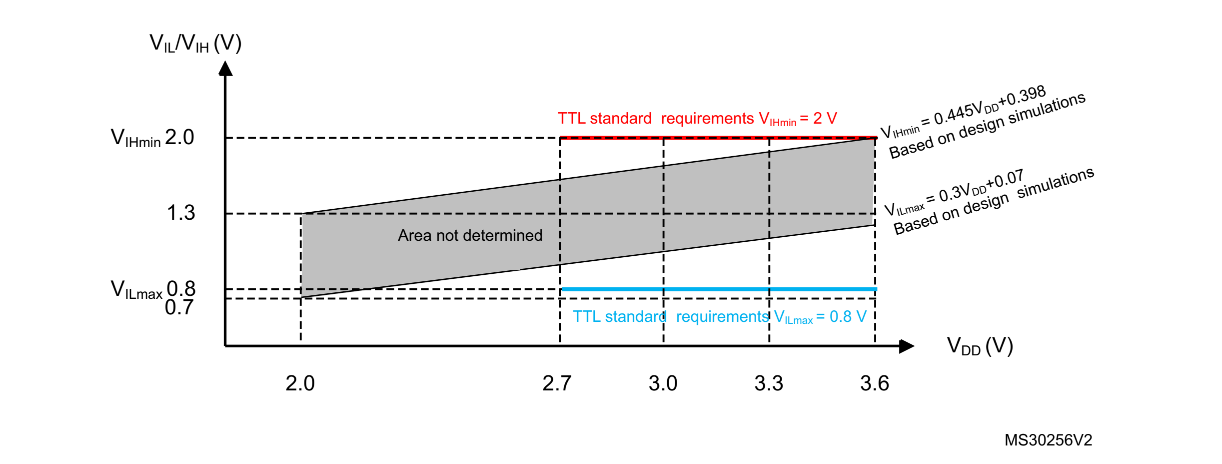



**Figure 20. 5V- tolerant (FT and FTf) I/O input characteristics - CMOS port**

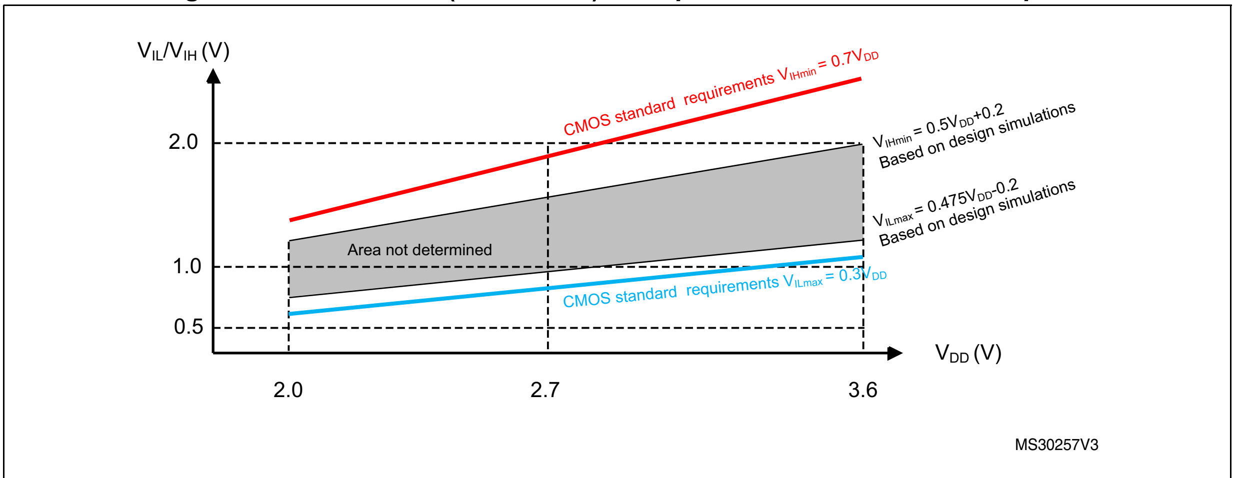



**Figure 21. 5V-tolerant (FT and FTf) I/O input characteristics - TTL port**

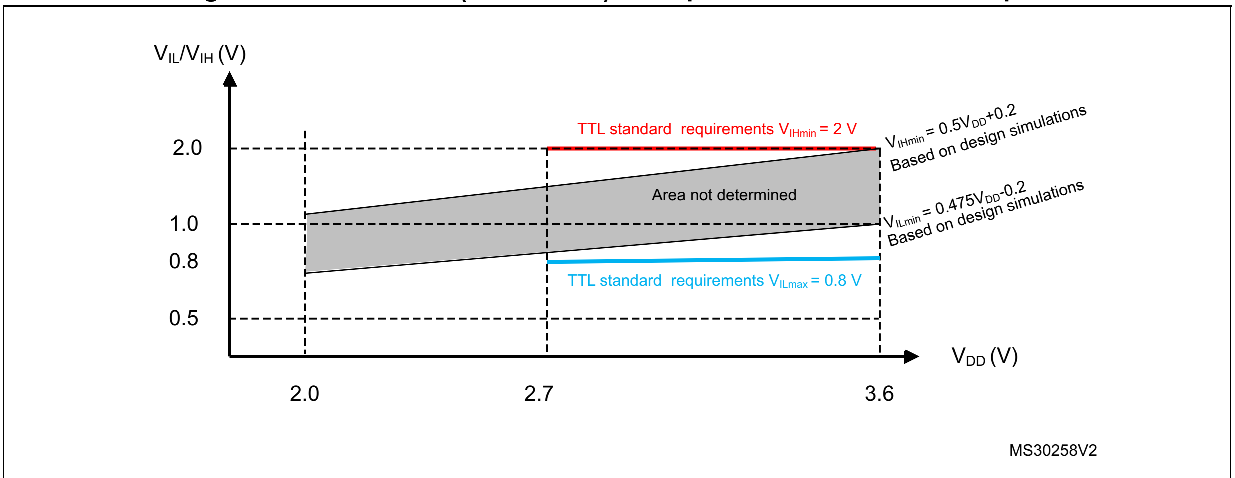


**Table 57. IWDG min./max. timeout period at 40 kHz (LSI) (1)**

| Prescaler divider | PR[2:0] bits | Min. timeout (ms) RL[11:0]= 0x000 | Max. timeout (ms) RL[11:0]= 0xFFF |
|---|---|---|---|
| /4 | 0 | 0.1 | 409.6 |
| /8 | 1 | 0.2 | 819.2 |
| /16 | 2 | 0.4 | 1638.4 |
| /32 | 3 | 0.8 | 3276.8 |
| /64 | 4 | 1.6 | 6553.6 |
| /128 | 5 | 3.2 | 13107.2 |
| /256 | 7 | 6.4 | 26214.4 |

1. These timings are given for a 40 kHz clock but the microcontroller's internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

**Table 58. WWDG min./max. timeout value at 72 MHz (PCLK)(1)**

| Prescaler | WDGTB | Min. timeout value | Max. timeout value |
|---|---|---|---|
| 1 | 0 | 0.05687 | 3.6409 |
| 2 | 1 | 0.1137 | 7.2817 |
| 4 | 2 | 0.2275 | 14.564 |
| 8 | 3 | 0.4551 | 29.127 |

1. Guaranteed by design, not tested in production.

## 6.3.17 Communication interfaces

### I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 Kbit/s
- Fast-mode (Fm): with a bit rate up to 400 Kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I²C timings requirements are guaranteed by design when the I²C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDD is disabled, but is still present. Only FTf I/O pins support Fm+ low-level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics* for the I²C I/O characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

**Table 61. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{CONV}$ | Total conversion time (including sampling time) | $f_{ADC}$ = 72 MHz<br>Resolution = 12 bits | 0.19 | - | 8.52 | µs |
| | | Resolution = 12 bits | 14 to 614 ($t_S$ for sampling + 12.5 for successive approximation) | | | $1/f_{ADC}$ |
| CMIR | Common Mode Input signal | ADC differential mode | $(V_{SSA}+V_{REF}+)/2$ -0.18 | $(V_{SSA} + V_{REF}+)/2$ | $(V_{SSA} + V_{REF}+)/2$ + 0.18 | V |

**Figure 27. ADC typical current consumption in single-ended and differential modes**

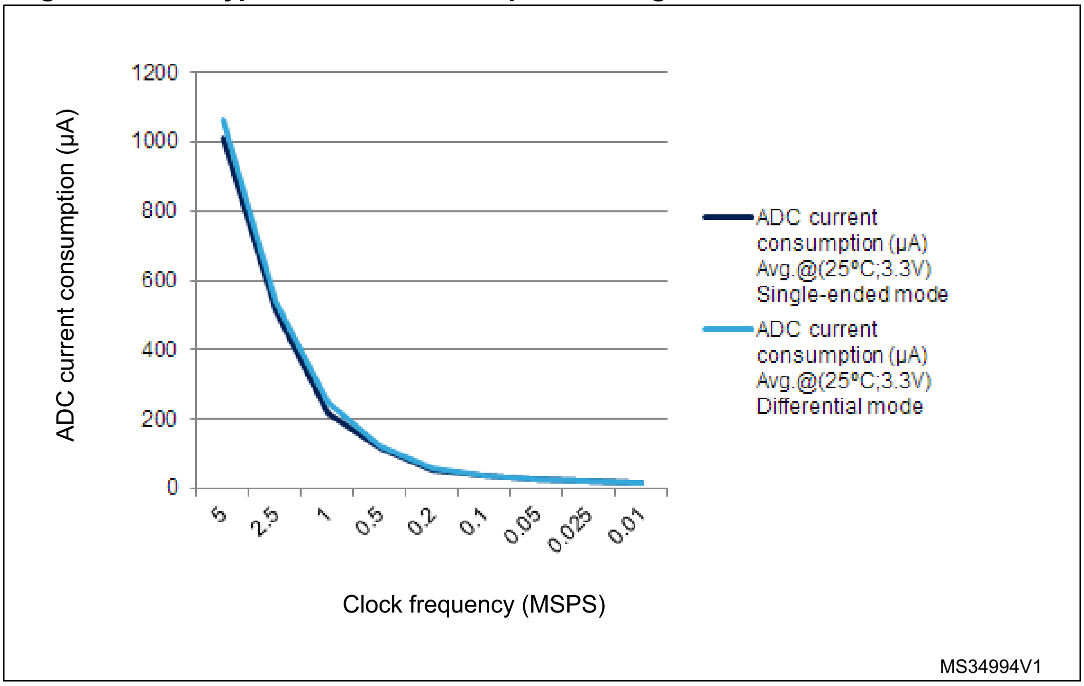
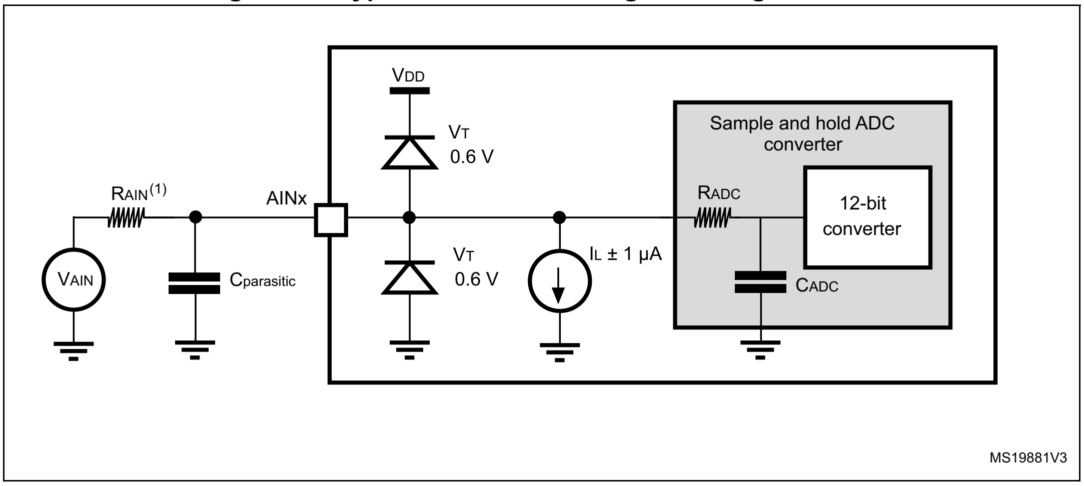



**Table 62. Maximum ADC $R_{AIN}$(1)**

| Resolution | Sampling cycle @ 72 MHz | Sampling time [ns] @ 72 MHz | $R_{AIN}$ max. (kΩ) | | |
|---|---|---|---|---|---|
| | | | Fast channels(2) | Slow channels | Other channels(3) |
| 12 bits | 1.5 | 20.83 | 0.018 | NA | NA |
| | 2.5 | 34.72 | 0.150 | NA | 0.022 |
| | 4.5 | 62.50 | 0.470 | 0.220 | 0.180 |
| | 7.5 | 104.17 | 0.820 | 0.560 | 0.470 |
| | 19.5 | 270.83 | 2.70 | 1.80 | 1.50 |
| | 61.5 | 854.17 | 8.20 | 6.80 | 4.70 |
| | 181.5 | 2520.83 | 22.0 | 18.0 | 15.0 |
| | 601.5 | 8354.17 | 82.0 | 68.0 | 47.0 |

**Figure 29. Typical connection diagram using the ADC**




1. Refer to *Table 61* for the values of $R_{AIN}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

### General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 10: Power-supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

## 6.3.19 DAC electrical specifications

**Table 66. DAC characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | 2.4 | - | 3.6 | V |
| $R_{LOAD}$(1) | Resistive load | DAC output buffer ON (to $V_{SSA}$ ) | 5 | - | - | kΩ |
| $R_{LOAD}$(1) | Resistive load | DAC output buffer ON (to $V_{DDA}$) | 25 | - | - | kΩ |
| $R_O$(1) | Output impedance | DAC output buffer OFF | - | - | 15 | kΩ |
| $C_{LOAD}$(1) | Capacitive load | DAC output buffer ON | - | - | 50 | pF |
| $V_{DAC\_OUT}$(1) | Voltage on DAC_OUT output | Corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{DDA}$ = 3.6 V and (0x155) and (0xEAB) at $V_{DDA}$ = 2.4 V | 0.2 | - | $V_{DDA}$ – 0.2 | V |
| | | DAC output buffer OFF | - | 0.5 | - | mV |
| | | | - | - | $V_{DDA}$– 1LSB | V |
| $I_{DDA}$(3) | DAC DC current consumption in quiescent mode(2) | With no load, middle code (0x800) on the input | - | - | 380 | μA |
| | | With no load, worst code (0xF1C) on the input. | - | - | 480 | μA |

# 7 Package information

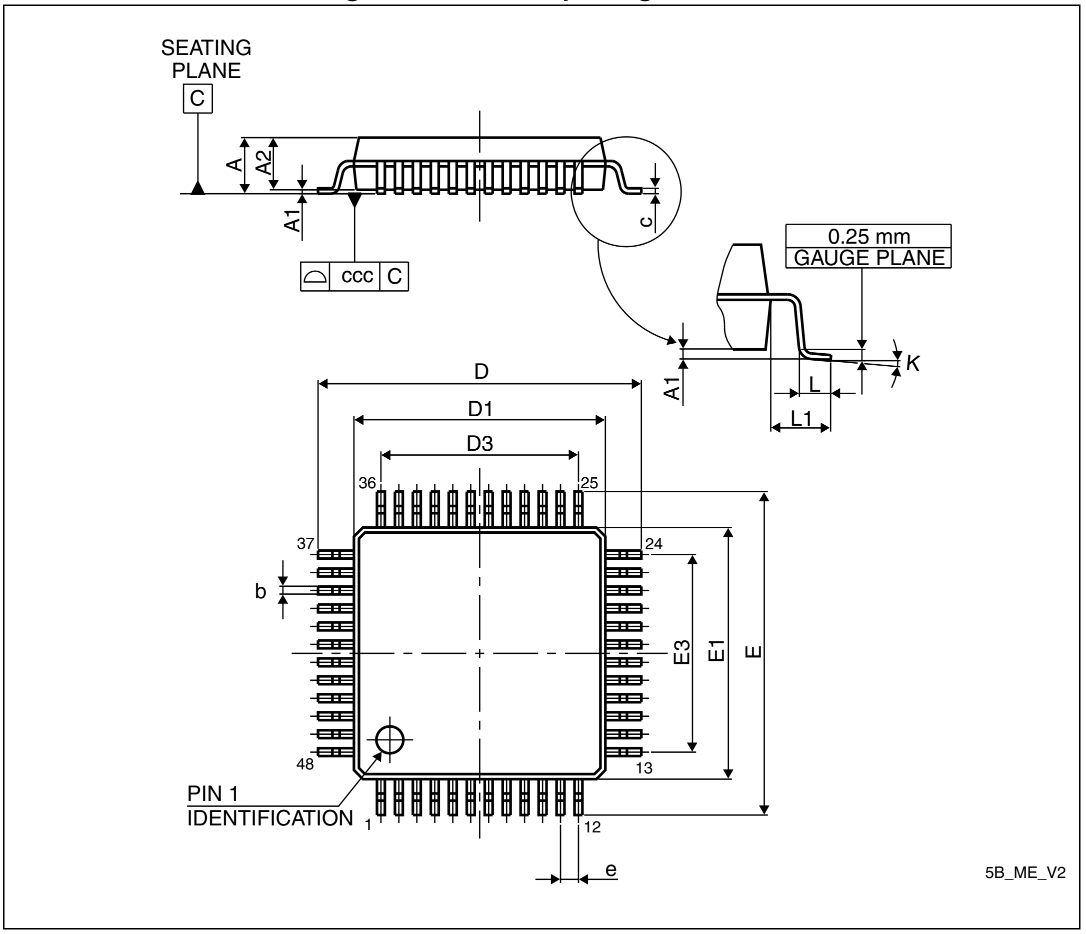
## 7.1 Package mechanical data

To meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 7.3 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7mm low-profile quad flat package.

**Figure 36. LQFP48 package outline**




1. Drawing is not to scale.

**Table 73. LQFP48 package mechanical data**

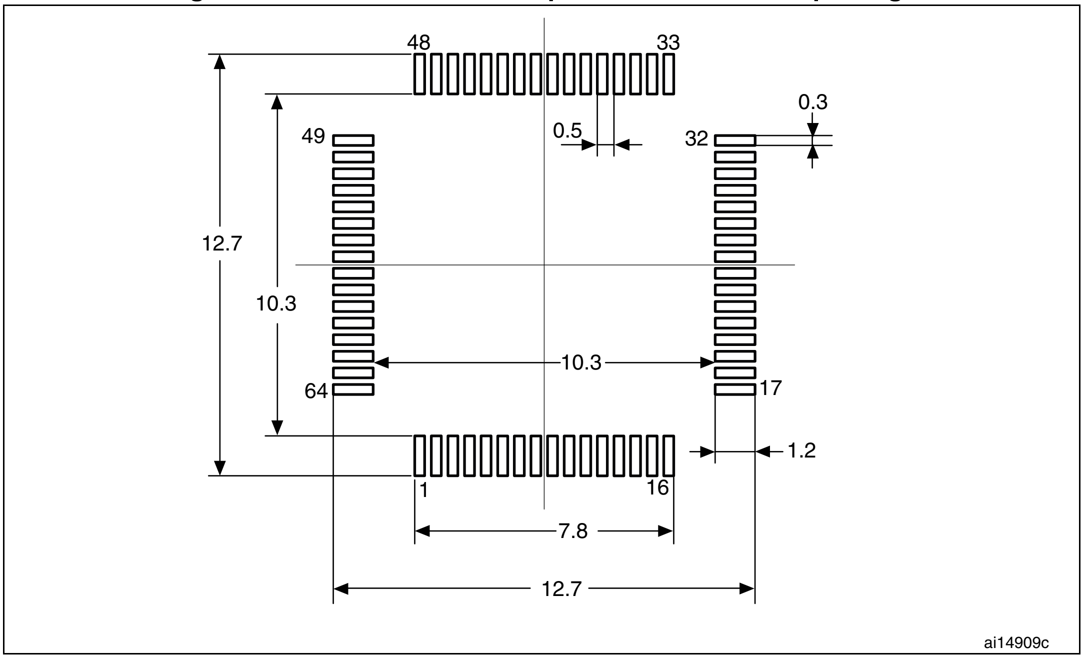
| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.500 | - | - | 0.2165 | - |

**Table 74. LQFP64 package mechanical data (continued)**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| N | Number of pins | | | | | |
| | 64 | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 40. Recommended footprint for the LQFP64 package**




1. Drawing is not to scale.
2. Dimensions are in millimeters.

## 7.5 Thermal characteristics

The maximum chip-junction temperature, $T_J$ max, in degrees Celsius, may be calculated using the following equation:

$T_J$ max = $T_A$ max + ($P_D$ max x $\Theta_{JA}$)

Where:

- $T_A$ max is the maximum ambient temperature in °C,
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D$ max is the sum of $P_{INT}$ max and $P_{I/O}$ max ($P_D$ max = $P_{INT}$ max + $P_{I/O}$ max),
- $P_{INT}$ max is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = $\Sigma$ ($V_{OL}$ × $I_{OL}$) + $\Sigma$(($V_{DD}$ – $V_{OH}$) × $I_{OH}$),

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low and high level in the application.

**Table 75. Package thermal characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | **Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch | 45°C/W | °C/W |
| $\Theta_{JA}$ | **Thermal resistance junction-ambient** LQFP32 - 7 × 7 mm / 0.8 mm pitch | 60°C/W | °C/W |

### 7.5.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

### 7.5.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 76: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F303x6/8 at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

#### Example: high-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax}$ = 82 °C (measured according to JESD51-2), $I_{DDmax}$ = 50 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low