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What Are Embedded - Microcontrollers - Application Specific?

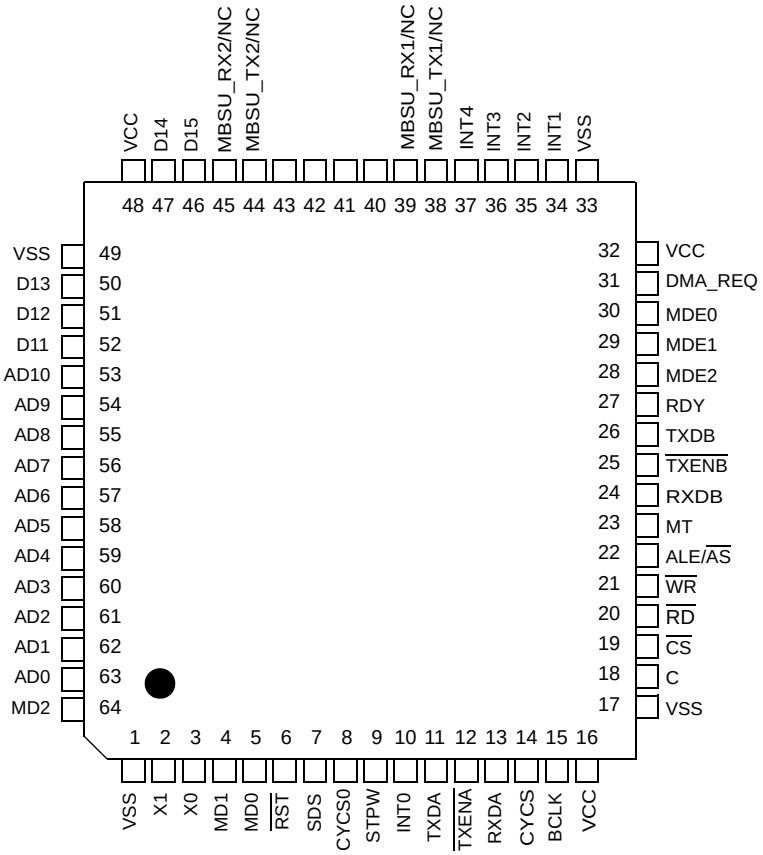
Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	External
Program Memory Type	External Program Memory
Controller Series	-
RAM Size	8K x 8
Interface	Parallel Host, SPI
Number of I/O	-
Voltage - Supply	3V ~ 5.5V
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb88121cpmc1-ge1

■ PIN ASSIGNMENTS

1. Pin assignment in 16 bit multiplexed parallel mode (MB88121B/C only)

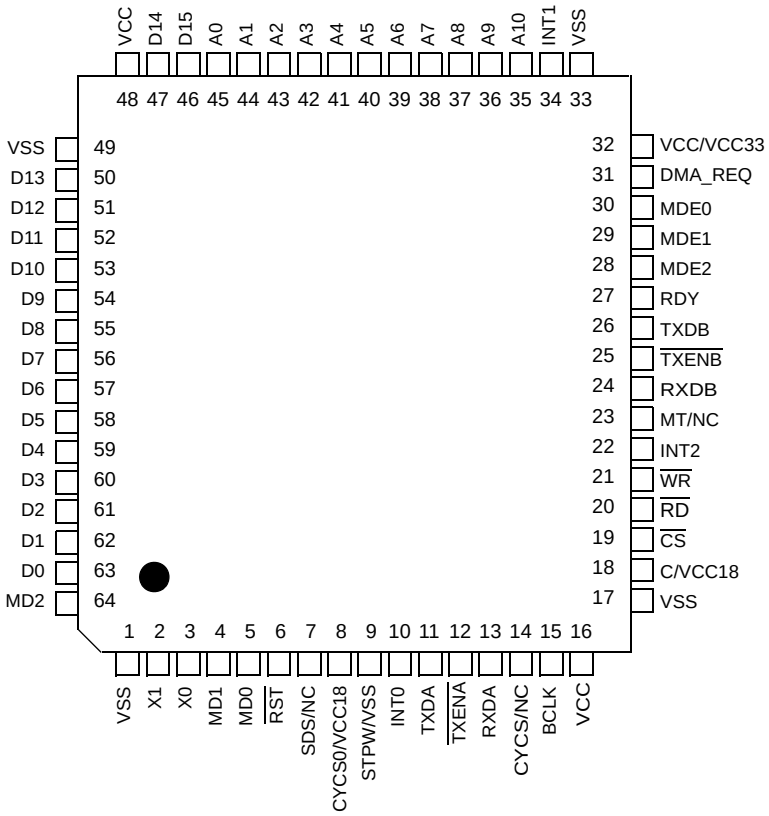
(TOP VIEW)



(FPT-64P-M03/M24)

2. Pin assignment in 16 bit non-multiplexed parallel mode

(TOP VIEW)



(FPT-64P-M03/M24)

■ PIN DESCRIPTION

Pin No.	Pin name	Circuit type	Function
1, 17, 33, 49	VSS	—	These are power supply ground (0 V) input pins
16, 48	VCC	—	MB88121B/C: These are power supply (3.3 - 5.0 V) input pins. MB88121(A): These are power supply (5.0 V) input pins
32	VCC/VCC33	—	MB88121B/C: This is a power supply (3.3 - 5.0 V) input pin. MB88121(A): 3.3V supply voltage for the level converters.
18	C/VCC18	—	MB88121B/C: This is the power supply stabilization capacitor pin. It should be connected to higher than or equal to 0.1 µF ceramic capacitor. MB88121(A): 1.8V core supply input pin.
2	X1	D	Oscillation output pin.
3	X0		Oscillation input pin. If external clock is used, it is connected here.
4 - 5	MD1 - MD0	A	Input pins for the mode selection.
6	$\overline{RST}$	A	Reset input pin.
7	SDS/NC	B/-	MB88121B/C: Debug pin: Start of dynamic segment, when function is disabled, this pin outputs 'L'-Level MB88121(A): Do not connect!
8	CYCS0/VCC18	B/-	MB88121B/C: Debug pin: Cycle 0 start output, when function is disabled, this pin outputs 'L'-Level MB88121(A): 1.8V core supply input pin.
9	STPWT/VSS	C/-	MB88121B/C: Stop Watch Trigger Input pin MB88121(A): Power supply ground (0 V) input pin.
10	INT0	B	Output pin for the Interrupt 0 output.
11	TXDA	B	Output pin for the data transmitter output channel A.
12	$\overline{TXENA}$	B	Output pin for the transmission enable output channel A.
13	RXDA	A	Input pin for the data receiver input channel A.
14	CYCS/NC	B/-	MB88121B/C: Debug pin: Cycle start output, when function is disabled, this pin outputs 'L'-Level MB88121(A): Do not connect!
15	BCLK	A	Input pin for the Bus Clock input. This function is enabled in all parallel modes.
	-		This pin is unused in SPI mode.
19	$\overline{CS}$	A	Input pin for the chip select input.
20	$\overline{RD}$	A	Input pin for the read enable input. This function is enabled in all parallel modes.
	-		This pin is unused in SPI mode.
21	$\overline{WR}$	A	Input pin for the write enable input. This function is enabled in all parallel modes.
	-		This pin is unused in SPI mode.

■ PIN FUNCTIONS VS. MODES

Pin No.	16bit mux mode (MB88121B/C only)	16bit non mux mode	SPI mode (MB88121B/C only)
1	VSS		
2	X1		
3	X0		
4	MD1		
5	MD0		
6	$\overline{\text{RST}}$		
7	MB88121B/C: SDS; MB88121(A):NC		
8	MB88121B/C: CYCS0 ; MB88121(A): VCC18		
9	MB88121B/C: STPWT; MB88121(A): VSS		
10	INT0		
11	TXDA		
12	$\overline{\text{TXENA}}$		
13	RXDA		
14	MB88121B/C: CYCS; MB88121(A): NC		
15	BCLK		-
16	VCC		
17	VSS		
18	MB88121B/C: C; MB88121(A): VCC18		
19	$\overline{\text{CS}}$		
20	$\overline{\text{RD}}$		-
21	$\overline{\text{WR}}$		-
22	ALE/$\overline{\text{AS}}$	INT2	-
23	MB88121B/C: MT; MB88121(A): NC		
24	RXDB		
25	$\overline{\text{TXENB}}$		
26	TXDB		
27	RDY		-
28	MDE2		
29	MDE1		
30	MDE0		
31	DMA_REQ		-
32	MB88121B/C: VCC; MB88121(A): VCC33		
33	VSS		

■ Used Clock for X0/X1

Input frequency of X0 and X1 is described Table below.

	MD[2:0]		
	100	101	110
Oscillator	4MHz/5MHz/8MHz	-	4MHz/5MHz/8MHz
External Clock	-	4MHz/5MHz/8MHz/ 10MHz/16MHz/20MHz/ 80MHz	4MHz/5MHz/8MHz/ 10MHz

11. Pin level at interrupt pins

In case that the interrupt pin is enabled following level is output

Level	Description
0	default value, no interrupt request is pending
1	Interrupt request is pending

The output changes to Low-Level when the corresponding flag in the E-Reay register is cleared.

For timer0 and timer1 interrupt pin(s) the High level is output only a dedicated time and set back to Low-Level.

See E-Ray User Manual for details. It is recommended to use egde detection at host side for these pins.

12. Data Accessing of MB88121 series

The MB88121 series includes a parallel bus Interface using 16-bit data width. However the internal Communication Controller requires a 32-bit data access. Therefore always access the MB88121 using 32-bit data access. The Bus Interface expect two 16-bit data transfer from the Host MCU.

The order of the transfer is important, otherwise data can be lost.

First 16-bit write cycle must be the lower, the second 16-bit write cycle the higher 16-bit address of the 32-bit address. As soon as data is written to the higher 16-bit Address, the Communication Controller is writing the 32-bit value to the address.

Example:

Write access to Input buffer: First 32-bit register WRDS1: (Address: 0x400 - 0x403)

Value of WRDS1 register: 0x0000 0000

First 16-bit write cycle via Bus interface to address 0x400-401: Value: 1234

Value of WRDS1 register: 0x0000 0000

Second 16 bit write cycle via Bus Interface to address 0x402 - 0x403: Value 5678

32-bit data written to WRDS1 address.

Value of WRDS1 register: 0x1234 5678

■ I/O MAP

Address	Symbol	Name	Reset	Access
Customer Registers				
0x0000	VER	Version Information Register	MB88121: 0410 7905 MB88121A: 0420 7906 MB88121B: 0430 79FF MB88121C: 0440 79FF	r
0x0004	CCNT	Clock Control Register	0000 0000	r/w
0x0008	CUS2	*reserved* Customer 2 Register (DBGS & DMAS)	MB88121: 0000 0000 MB88121A/B/C:0000 0000	r r/w
0x000C	- INT	*reserved* Interrupt Register	MB88121(A): 0000 0000 MB88121B/C: 0000 0000	r r/w
Special Registers				
0x0010	-	*reserved (1) (don't write)*	MB88121: 0000 0000 MB88121A/B/C: 0000 0300	r
0x0014	-	*reserved (1) (don't write)*	0000 0000	r
0x0018	-	*reserved (1)*	0000 0000	r
0x001C	LCK	Lock Register	0000 0000	r/w
Interrupt Registers				
0x0020	EIR	Error Interrupt Register	0000 0000	r/w
0x0024	SIR	Status Interrupt Register	0000 0000	r/w
0x0028	EILS	Error Interrupt Line Select	0000 0000	r/w
0x002C	SILS	Status Interrupt Line Select	MB88121: 0303 7FFF MB88121A/B/C: 0303 FFFF	r/w
0x0030	EIES	Error Interrupt Enable Set	0000 0000	r/w
0x0034	EIER	Error Interrupt Enable Reset	0000 0000	r/w
0x0038	SIES	Status Interrupt Enable Set	0000 0000	r/w
0x003C	SIER	Status Interrupt Enable Reset	0000 0000	r/w
0x0040	ILE	Interrupt Line Enable	0000 0000	r/w
0x0044	T0C	Timer 0 Configuration	0000 0000	r/w
0x0048	T1C	Timer 1 Configuration	0002 0000	r/w
0x004C	STPW STPW1	Stop Watch Register Stop Watch Register 1	MB88121/A: 0000 0000 MB88121B/C: 0000 0000	r/w
0x0050	- STPW2	*reserved* Stop Watch Register 2	MB88121/A: 0000 0000 MB88121B/C: 0000 0000	r
0x0054 - 0x007C	-	*reserved (11)*	0000 0000	r

(Continued)

Address	Symbol	Name	Reset	Access
CC Control Registers				
0x0080	SUCC	SUC Configuration Register 1	MB88121: 0C40 0000 MB88121A/B/C: 0C40 1000	r/w
0x0084	SUCC2	SUC Configuration Register 2	MB88121: 0100 05A4 MB88121A/B/C: 0100 0504	r/w
0x0088	SUCC3	SUC Configuration Register 3	0000 0011	r/w
0x008C	NEMC	NEM Configuration Register	0000 0000	r/w
0x0090	PRTC1	PRT Configuration Register 1	MB88121: 084C 0005 MB88121A/B/C: 084C 0633	r/w
0x0094	PRTC2	PRT Configuration Register 2	MB88121: 0F2D 0E0E MB88121A/B/C:0F2D 0A0E	r/w
0x0098	MHDC	MHD Configuration Register	MB88121: 0001 0000 MB88121A/B/C: 0000 0000	r/w
0x009C	-	*reserved (1)*	0000 0000	r
0x00A0	GTUC1	GTU Configuration Register 1	MB88121: 0000 02D0 MB88121A/B/C: 0000 0280	r/w
0x00A4	GTUC2	GTU Configuration Register 2	MB88121: 0002 000C MB88121A/B/C: 0002 000A	r/w
0x00A8	GTUC3	GTU Configuration Register 3	MB88121: 0001 0000 MB88121A/B/C: 0202 0000	r/w
0x00AC	GTUC4	GTU Configuration Register 4	MB88121: 000A 0009 MB88121A/B/C: 0008 0007	r/w
0x00B0	GTUC5	GTU Configuration Register 5	MB88121: 0A01 0000 MB88121A/B/C: 0E00 0000	r/w
0x00B4	GTUC6	GTU Configuration Register 6	0002 0000	r/w
0x00B8	GTUC7	GTU Configuration Register 7	MB88121: 0002 0005 MB88121A/B/C: 0002 0004	r/w
0x00BC	GTUC8	GTU Configuration Register 8	0000 0002	r/w
0x00C0	GTUC9	GTU Configuration Register 9	MB88121: 0001 0101 MB88121A/B/C: 0000 0101	r/w
0x00C4	GTUC10	GTU Configuration Register 10	MB88121: 0002 0001 MB88121A/B/C: 0002 0005	r/w
0x00C8	GTUC11	GTU Configuration Register 11	0000 0000	r/w
0x00CC - 0x00FC	-	*reserved (13)*	0000 0000	r

(Continued)

Address	Symbol	Name	Reset	Access
Input Buffer				
0x0400 - 0x04FC	WRDSn	Write Data Section [1...64]	0000 0000	r/w
0x0500	WRHS1	Write Header Section 1	0000 0000	r/w
0x0504	WRHS2	Write Header Section 2	0000 0000	r/w
0x0508	WRHS3	Write Header Section 3	0000 0000	r/w
0x050C	-	*reserved (1)*	0000 0000	r/w
0x0510	IBCM	Input Buffer Command Mask	0000 0000	r/w
0x0514	IBCR	Input Buffer Command Request	0000 0000	r/w
0x0518 - 0x05FC	-	*reserved (58)*	0000 0000	r
Output Buffer				
0x0600 - 0x06FC	RDDSn	Read Data Section [1 ...64]	0000 0000	r
0x0700	RDHS1	Read Header Section 1	0000 0000	r
0x0704	RDHS2	Read Header Section 2	0000 0000	r
0x0708	RDHS3	Read Header Section 3	0000 0000	r
0x070C	MBS	Message Buffer Status	0000 0000	r
0x0710	OBCM	Output Buffer Command Mask	0000 0000	r/w
0x0714	OBCR	Output Buffer Command Request	0000 0000	r/w
0x0718 - 0x07FC	-	*reserved (58)*	0000 0000	r

- Explanation on read/write
  r/w: Readable and Writable
  r: Read only
  w: Write only

Note : Any write access to reserved addresses in I/O map may result in unexpected behaviour. A read access to reserved address results in reading “X”.

<table>
<tr><th>Bit</th><th>Name</th><th>Function</th></tr>
<tr><td>bit31 - bit14</td><td>RSV: Reserved</td><td>These bits are reserved. “0” is read. Write “0”.</td></tr>
<tr><td>bit13 - bit12</td><td>SRST[1:0]</td><td>These bits initialize Communication Controller. When "00", "01", "10", "11" are written to these bits continuously, Communication Controller is initialized.
First : write "00" to SRST[1:0]
Second: Write "01" to SRST[1:0]
Third : Write "10" to SRST[1:0]
Forth : Write "11" to SRST[1:0] <- Initialize
If the condition isn't full, Communication Controller isn't initialized.
These bits are invalid for MB88121, MB88121A and MB88121B.</td></tr>
<tr><td>bit10 - bit 9</td><td>RSV Reserved</td><td>This bit is reserved. Always write “0”.</td></tr>
<tr><td>bit8 - bit7</td><td>SDIV[1:0]:
Division for system clock</td><td>These bits control the division for system clock. This function is supported in MB88121A, MB88121B and MB88121C. These bits are reserved in MB88121. In MB88121, “0” is read and write “0”.

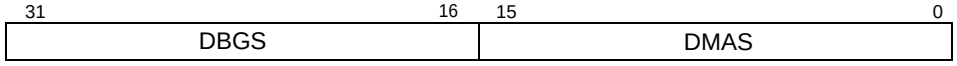
<table><tr><th>SDIV[1]</th><th>SDIV[0]</th><th>Function</th></tr><tr><td>0</td><td>0</td><td>System clock is divided by 1</td></tr><tr><td>0</td><td>1</td><td>System clock is divided by 2</td></tr><tr><td>1</td><td>0</td><td>System clock is divided by 4</td></tr><tr><td>1</td><td>1</td><td>System clock is divided by 8</td></tr></table>
<<Note>>
When FlexRay controller can receive or transmit data, these bits must not be changed.</td></tr>
<tr><td>bit6</td><td>RSV: Reserved</td><td>This bit is reserved. Always write “0”.</td></tr>
</table>

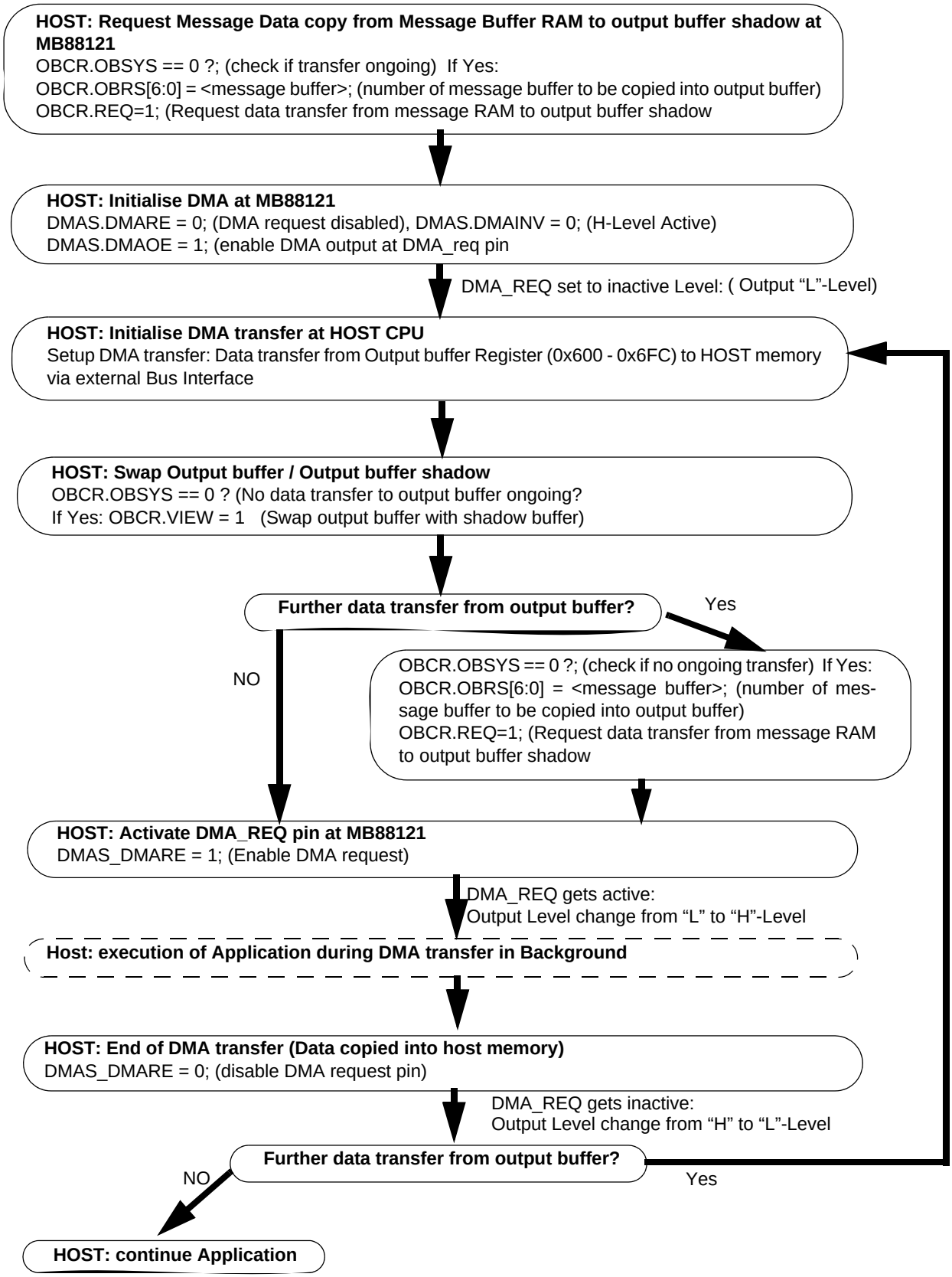
Bit	Name	Function
bit0	PON: PLL Oscillator Enable	This bit controls PLL oscillator. "0": Stop PLL oscillator "1": PLL oscillator enable In MB88121 and MB88121A, the functionality of the PLL is not guaranteed. <<Note>> This bit must be changed when SSEL bit is "0".

■ Customer 2 Register

The Customer2 Register (CUS2) is a 32-bit register, at address 0x0008.
The upper 16 bit (B16..31) are called Debug support Register (DBGS).
The lower 16 bit (Bit 0..15) are called DMA support register (DMAS)
Always access the customer 2 register 32-bit wise

Address
0x0008




HOST: Request Message Data copy from Message Buffer RAM to output buffer shadow at MB88121
OBCR.OBSYS == 0 ?; (check if transfer ongoing) If Yes:
OBCR.OBRS[6:0] = <message buffer>; (number of message buffer to be copied into output buffer)
OBCR.REQ=1; (Request data transfer from message RAM to output buffer shadow
HOST: Initialise DMA at MB88121
DMAS.DMARE = 0; (DMA request disabled), DMAS.DMAINV = 0; (H-Level Active)
DMAS.DMAOE = 1; (enable DMA output at DMA_req pin
DMA_REQ set to inactive Level: (Output "L"-Level)
HOST: Initialise DMA transfer at HOST CPU
Setup DMA transfer: Data transfer from Output buffer Register (0x600 - 0x6FC) to HOST memory via external Bus Interface
HOST: Swap Output buffer / Output buffer shadow
OBCR.OBSYS == 0 ? (No data transfer to output buffer ongoing?
If Yes: OBCR.VIEW = 1 (Swap output buffer with shadow buffer)
Further data transfer from output buffer?
Yes
NO
OBCR.OBSYS == 0 ?; (check if no ongoing transfer) If Yes:
OBCR.OBRS[6:0] = <message buffer>; (number of message buffer to be copied into output buffer)
OBCR.REQ=1; (Request data transfer from message RAM to output buffer shadow
HOST: Activate DMA_REQ pin at MB88121
DMAS_DMARE = 1; (Enable DMA request)
DMA_REQ gets active:
Output Level change from "L" to "H"-Level
Host: execution of Application during DMA transfer in Background
HOST: End of DMA transfer (Data copied into host memory)
DMAS_DMARE = 0; (disable DMA request pin)
DMA_REQ gets inactive:
Output Level change from "H" to "L"-Level
Further data transfer from output buffer?
NO
Yes
HOST: continue Application

2. Wait states caused by the RDY pin

The maximum low width of RDY is as follows.
1) BCLK=32MHz, RAM clock=80MHz

MODE	Low width of RDY during read operation	Low width of RDY during writing operation
FR460	Maximum 5BCLK	Maximum 5BCLK
16FX	Maximum 5BCLK + Low width of BCLK	Maximum 5BCLK + Low width of BCLK

2) BCLK=32MHz, RAM clock=40MHz

MODE	Low width of RDY during read operation	Low width of RDY during writing operation
FR460	Maximum 7BCLK	Maximum 7BCLK
16FX	Maximum 7BCLK + Low width of BCLK	Maximum 7BCLK + Low width of BCLK

3. The read timing for the register

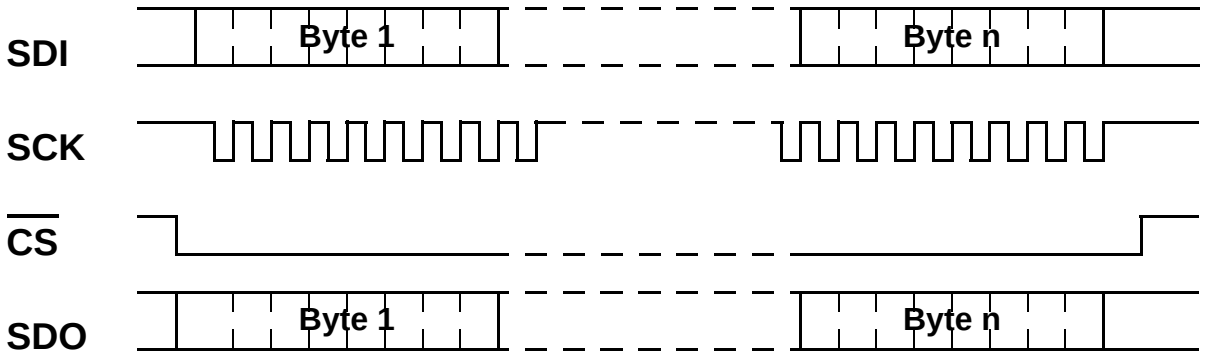
The FlexRay Controller registers have a width of 32bit. A 32bit temporary read register is available to save read data. In the case of reading in 16bit multiplexted parallel bus mode, data of the register selected by the address data latched by the AS pin or ALE pin is written to the temporary register by the first read access, and the data of temporary register is output to the D[15:11] pins and AD[10:0] pins as follows.

FR460 mode: Data of the 16bit upper temporary register is output to the D[15:11] pins and AD[10:0] in case of the first read access, and data of the 16bit lower temporary register is output to the D[15:11] pins and AD[10:0] pins in case of the second read access.

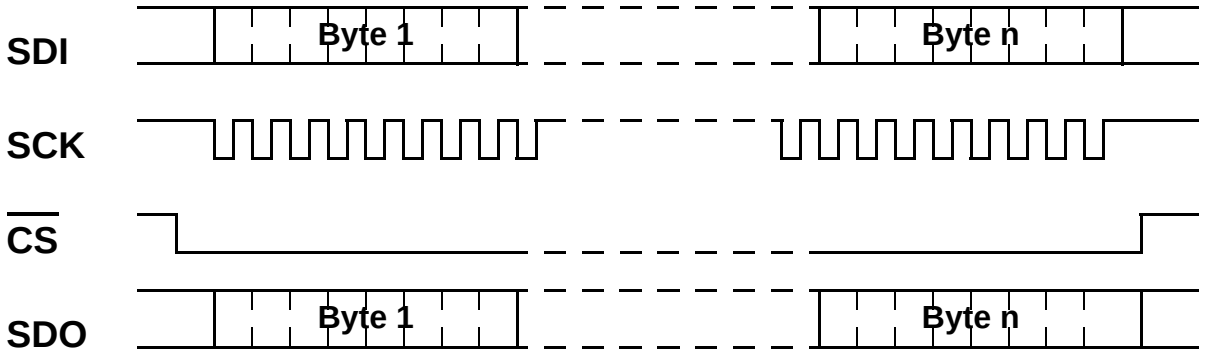
16FX mode: Data of the 16bit lower temporary register is output to the D[15:11] pins and AD[10:0] in case of the first read access, and data of the 16bit upper temporary register is output to the D[15:11] pins and AD[10:0] pins in case of the second read access.

Read operation in FR460 mode

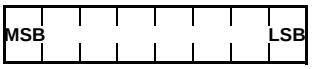
MDS[1:0] = 10: Active-low clock, sampling on odd (falling) edge



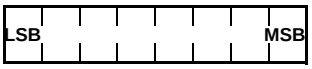
MDS[1:0] = 11: Active-low clock, sampling on even (rising) edge



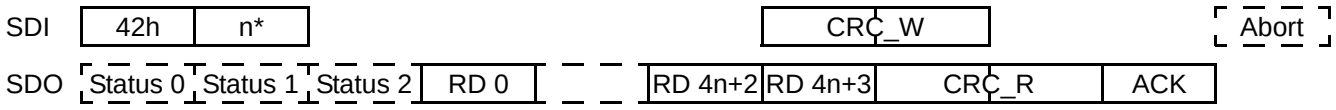
MDS[2] = 0: MSB first



MDS[2] = 1: LSB first



RBI: Read Output Buffer, Initialize OBP, Command Byte = 42h

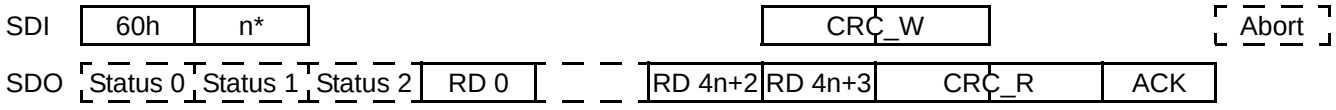


*: n = word count - 1; 0 ≤n ≤63

Clear OBP and read data starting at address 600h (OBP = Output Buffer Pointer). After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, OBP is incremented by n+1 if CS has a rising edge immediately after ACK. If there is no rising CS edge immediately after ACK, OBP is not incremented. The SPI master can transmit an extra byte (Abort) after it has received the ACK. In this case, MB88121 will detect clock edges when it expects a rising CS edge and will not increment OBP.

Payload:	4*(n+1) bytes
Command length:	6 + 4*(n+1) bytes
Overhead:	150% / (n+1)
Efficiency:	100% * (1 - 3/(2n+5))

RBC: Read Output Buffer, Continue, Command Byte = 60h

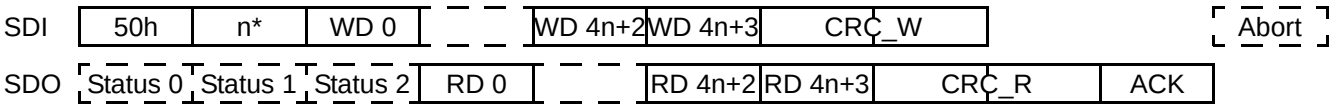


*: n = word count - 1; 0 ≤n ≤63

Read data starting at address 600h+4*OBP (OBP = Output Buffer Pointer). After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, OBP is incremented by n+1 if CS has a rising edge immediately after ACK. If there is no rising CS edge immediately after ACK, OBP is not incremented. The SPI master can transmit an extra byte (Abort) after it has received the ACK. In this case, MB88121 will detect clock edges when it expects a rising CS edge and will not increment OBP.

Payload:	4*(n+1) bytes
Command length:	6 + 4*(n+1) bytes
Overhead:	150% / (n+1)
Efficiency:	100% * (1 - 3/(2n+5))

RBIWBI: Combination of RBI and WBI, Command Byte = 50h

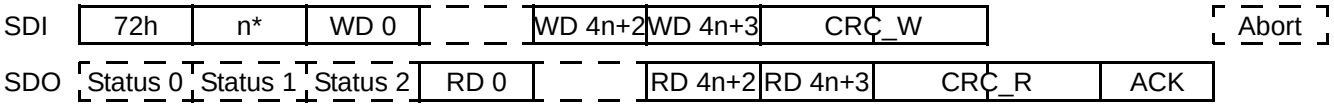


*: n = word count - 1; 0 ≤n ≤63

Clear IBP and write data starting at address 400h (IBP = Input Buffer Pointer). Clear OBP and read data starting at address 600h (OBP = Output Buffer Pointer). After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, IBP and OBP are incremented by n+1 if $\overline{CS}$ has a rising edge immediately after ACK. If there is no rising $\overline{CS}$ edge immediately after ACK, IBP and OBP are not incremented. The SPI master can transmit an extra byte (Abort) after it has received the ACK. In this case, MB88121 will detect clock edges when it expects a rising $\overline{CS}$ edge and will not increment IBP and OBP.

Payload:	8*(n+1) bytes
Command length:	6 + 4*(n+1) bytes
Overhead:	75% / (n+1) - 50%
Efficiency:	200% * (1 - 3/(2n+5))

RBCWBI: Combination of RBC and WBI, Command Byte = 72h

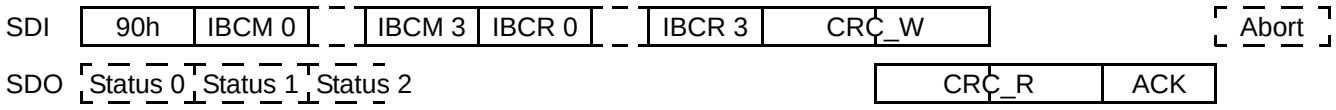


*: n = word count - 1; 0 ≤n ≤63

Clear IBP and write data starting at address 400h (IBP = Input Buffer Pointer). Read data starting at address 600h+4*OBP (OBP = Output Buffer Pointer). After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, IBP and OBP are incremented by n+1 if $\overline{CS}$ has a rising edge immediately after ACK. If there is no rising $\overline{CS}$ edge immediately after ACK, IBP and OBP are not incremented. The SPI master can transmit an extra byte (Abort) after it has received the ACK. In this case, MB88121 will detect clock edges when it expects a rising $\overline{CS}$ edge and will not increment IBP and OBP.

Payload:	8*(n+1) bytes
Command length:	6 + 4*(n+1) bytes
Overhead:	75% / (n+1) - 50%
Efficiency:	200% * (1 - 3/(2n+5))

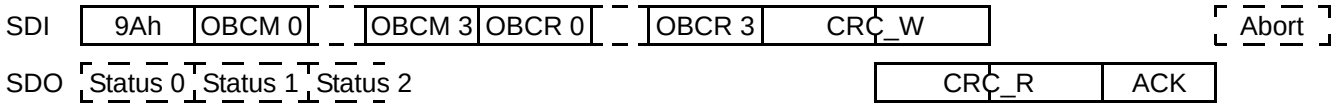
WRIBC: Write Input Buffer Command, Command Byte = 90h



Write IBCM[3:0] to IBCM register. After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, IBCR[3:0] is written to IBCR register if $\overline{CS}$ has a rising edge immediately after ACK. If there is no rising $\overline{CS}$ edge immediately after ACK, the IBCR register is not written. The SPI master can transmit an extra byte (Abort) after it has received the ACK. In this case, MB88121 will detect clock edges when it expects a rising $\overline{CS}$ edge and will not write the IBCR register.
It is no problem that IBCM register may be written even in the case of a communication problem: IBCM is only a configuration register, it does not trigger an action. On the other hand, writing the IBCR register triggers an action. For this reason, IBCR is written only after it has been confirmed that there has been no communication problem.

Payload:	8 bytes
Command length:	13 bytes
Overhead:	62.5%
Efficiency:	61.5%

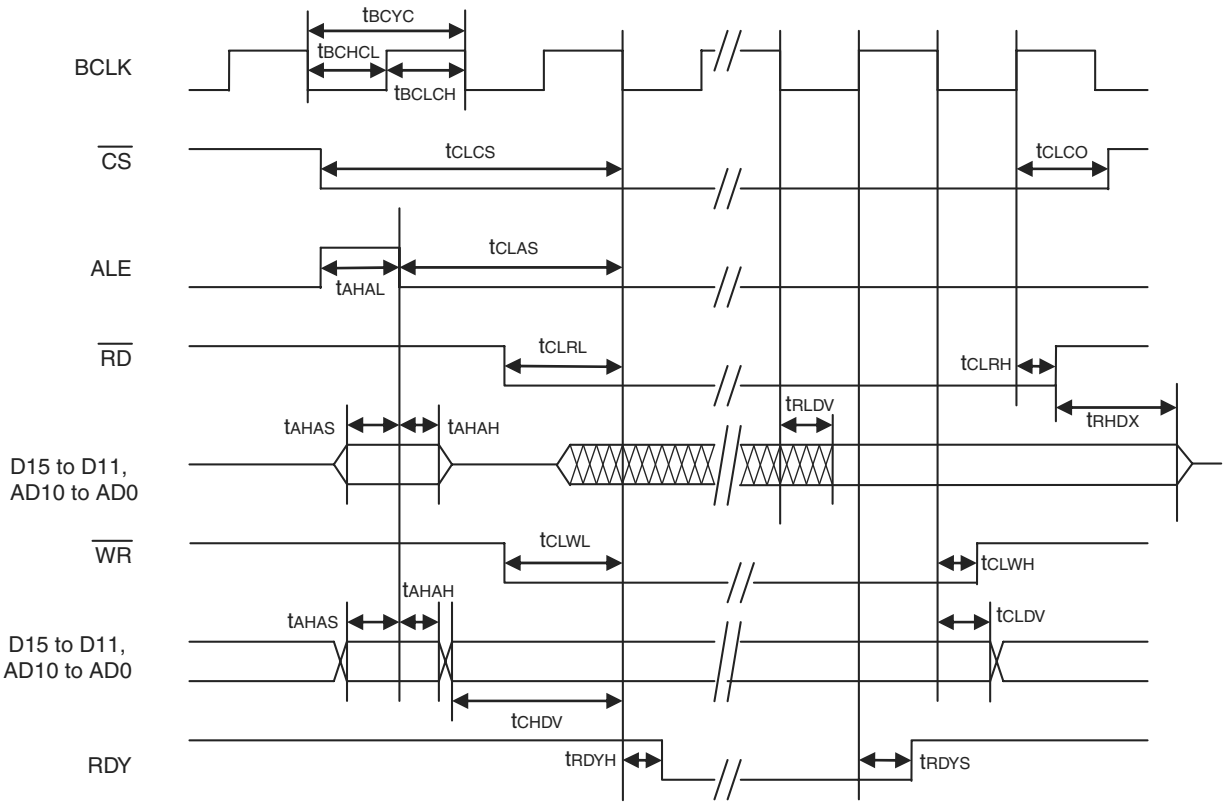
WROBC: Write Output Buffer Command, Command Byte = 9Ah



Write OBCM[3:0] to OBCM register. After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, OBCR[3:0] is written to OBCR register if $\overline{CS}$ has a rising edge immediately after ACK. If there is no rising $\overline{CS}$ edge immediately after ACK, the OBCR register is not written. The SPI master can transmit an extra byte (Abort) after it has received the ACK. In this case, MB88121 will detect clock edges when it expects a rising $\overline{CS}$ edge and will not write the OBCR register.
It is no problem that OBCM register may be written even in the case of a communication problem: OBCM is only a configuration register, it does not trigger an action. On the other hand, writing the OBCR register triggers an action. For this reason, OBCR is written only after it has been confirmed that there has been no communication problem.

Payload:	8 bytes
Command length:	13 bytes
Overhead:	62.5%
Efficiency:	61.5%

■16bit multiplexed mode(16FX mode)



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