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What Are Embedded - Microcontrollers - Application Specific?

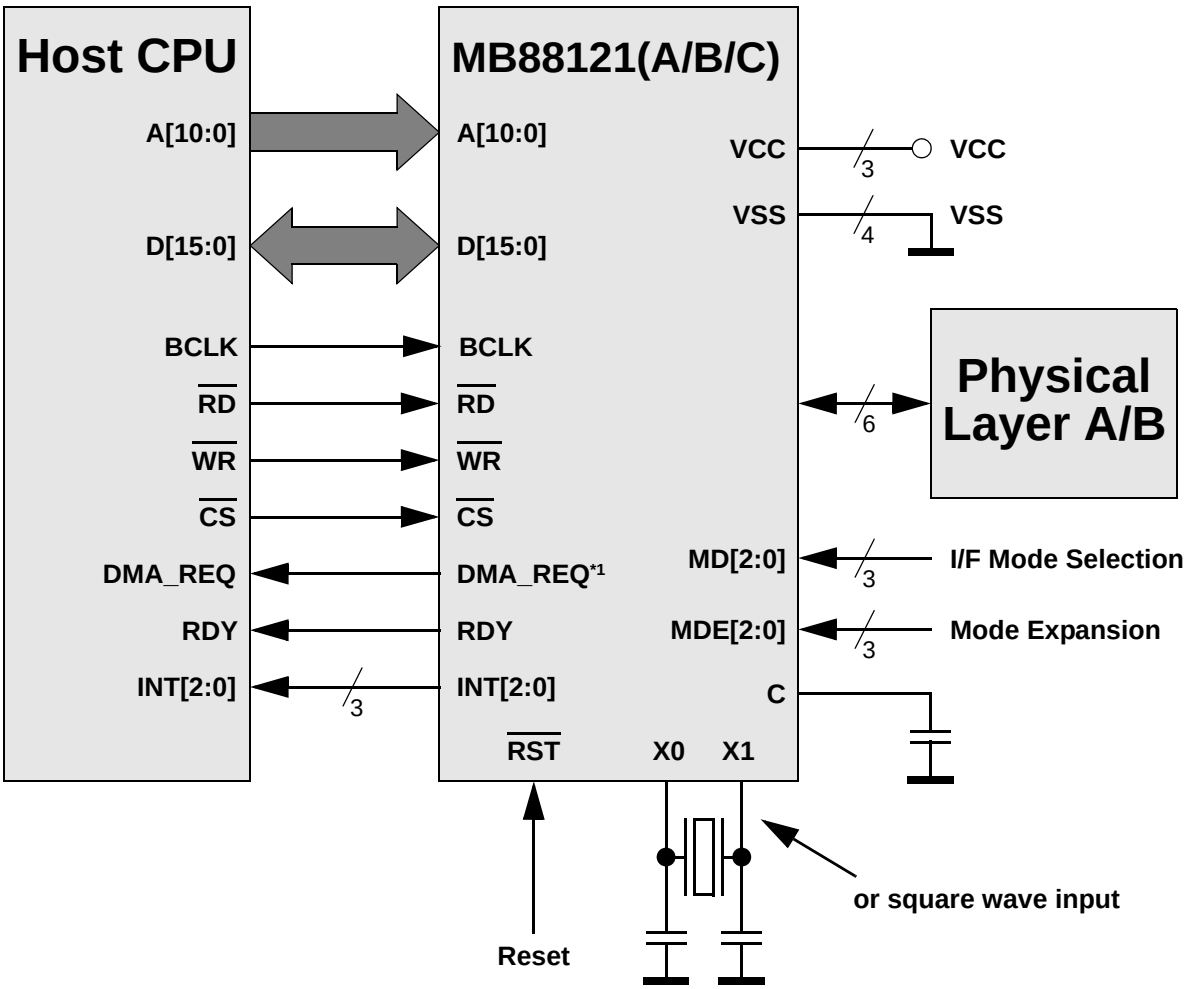
Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	External
Program Memory Type	External Program Memory
Controller Series	-
RAM Size	8K x 8
Interface	Parallel Host, SPI
Number of I/O	-
Voltage - Supply	3V ~ 5.5V
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb88121cpmc1-gs-n2e2

Pin No.	Pin name	Circuit type	Function
22	ALE	C	Input pin for the address latch enable input (high active). This function is enabled in the multiplexed parallel modes for 16FX and for other devices to be defined later.
	$\overline{AS}$		Input pin for the address strobe input (low active). This function is enabled in the multiplexed parallel modes. Timing meets FR core devices (460 series) and other devices.
	INT2		Output pin for the Interrupt 2 output. This function is enabled in 16-bit non-multiplexed parallel mode.
	-		This pin is Hi-Z in in SPI mode.
23	MT/NC	B/-	MB88121B/C: Debug pin; Macrotick start output, when function is disabled, this pin outputs 'L'-Level MB88121(A): Do not connect!
24	RXDB	A	Input pin for the data receiver input channel B.
25	$\overline{TXENB}$	B	Output pin for the transmission enable output channel B.
26	TXDB	B	Output pin for the data transmitter output channel B.
27	RDY	B	Output pin for the ready output. This function is enabled in all parallel modes.
	-		This pin is Hi-Z in SPI mode.
28-30	MDE2 - MDE0	A	Input pins for the extended mode selection.
31	DMA_REQ	B	Output pin for the DMA request output (MB88121A/B/C only). On MB88121, this pin outputs "L" level. This function is enabled in all parallel modes
	-	B	This pin is Hi-Z in SPI mode.
34	INT1	B	Output pin for the Interrupt 1 output.
35	A10	C	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	INT2		Output pin for the Interrupt 2 output. This function is enabled in 16-bit multiplexed parallel mode.
	-		This pin is Hi-Z in SPI mode.
36	A9	C	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	INT3		Output pin for the Interrupt 3 output. This function is enabled in 16-bit multiplexed parallel mode.
	-		This pin is Hi-Z in SPI mode.
37	A8	C	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed multiplexed parallel mode.
	INT4		Output pin for the Interrupt 4 output This function is enabled in 16-bit multiplexed parallel mode
	-		This pin is Hi-Z inSPI mode.

Pin No.	Pin name	Circuit type	Function
38	A7	C	Input pins for the address bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	MBSU_TX1		MB88121B/C: Debug pin, when function is disabled, this pin outputs 'L'-Level MB88121(A): Not supported. This function is enabled in 16-bit multiplexed parallel and SPI mode.
39	A6	C	Input pins for the address bus. This function is enabled in 16-bit non-multiplexed parallel mode.
	MBSU_RX1		MB88121B/C: Debug pin, when function is disabled, this pin outputs 'L'-Level MB88121(A): Not supported. This function is enabled in 16-bit multiplexed parallel and SPI mode.
40	A5	A	Input pin for the address bus. This function is enabled 16-bit non-multiplexed parallel modes.
	SCK		Input pin for the serial clock input. This function is enabled in SPI mode.
	-		This pin is unused in 16-bit multiplexed parallel modes.
41	A4	A	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel modes.
	SDI		Input pin for the serial data input. This function is enabled in SPI mode.
	-		This pin is unused in 16-bit multiplexed parallel modes.
42	A3	C	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel modes.
	SDO		Output pin for the serial data output. When CS is "H" SDO is High-Z. This function is enabled in SPI mode.
	-		This pin is Hi-Z in 16-bit multiplexed parallel modes.
43	A2	A	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel modes.
	-		This pin is unused in 16-bit multiplexed parallel mode and in SPI mode.
44	A1	C	Input pin for the address bus. This function is enabled in 16-bit non-multiplexed parallel modes.
	MBSU_TX2		MB88121B/C: Debug pin, when function is disabled, this pin outputs 'L'-Level MB88121(A): Not supported. This function is enabled in 16-bit multiplexed parallel and SPI mode.

Connection to Host CPU in 16-bit non-multiplexed Mode



*1: MB88121A/B/C only

(Continued)

Address	Symbol	Name	Reset	Access
CC Control Registers				
0x0080	SUCC	SUC Configuration Register 1	MB88121: 0C40 0000 MB88121A/B/C: 0C40 1000	r/w
0x0084	SUCC2	SUC Configuration Register 2	MB88121: 0100 05A4 MB88121A/B/C: 0100 0504	r/w
0x0088	SUCC3	SUC Configuration Register 3	0000 0011	r/w
0x008C	NEMC	NEM Configuration Register	0000 0000	r/w
0x0090	PRTC1	PRT Configuration Register 1	MB88121: 084C 0005 MB88121A/B/C: 084C 0633	r/w
0x0094	PRTC2	PRT Configuration Register 2	MB88121: 0F2D 0E0E MB88121A/B/C:0F2D 0A0E	r/w
0x0098	MHDC	MHD Configuration Register	MB88121: 0001 0000 MB88121A/B/C: 0000 0000	r/w
0x009C	-	*reserved (1)*	0000 0000	r
0x00A0	GTUC1	GTU Configuration Register 1	MB88121: 0000 02D0 MB88121A/B/C: 0000 0280	r/w
0x00A4	GTUC2	GTU Configuration Register 2	MB88121: 0002 000C MB88121A/B/C: 0002 000A	r/w
0x00A8	GTUC3	GTU Configuration Register 3	MB88121: 0001 0000 MB88121A/B/C: 0202 0000	r/w
0x00AC	GTUC4	GTU Configuration Register 4	MB88121: 000A 0009 MB88121A/B/C: 0008 0007	r/w
0x00B0	GTUC5	GTU Configuration Register 5	MB88121: 0A01 0000 MB88121A/B/C: 0E00 0000	r/w
0x00B4	GTUC6	GTU Configuration Register 6	0002 0000	r/w
0x00B8	GTUC7	GTU Configuration Register 7	MB88121: 0002 0005 MB88121A/B/C: 0002 0004	r/w
0x00BC	GTUC8	GTU Configuration Register 8	0000 0002	r/w
0x00C0	GTUC9	GTU Configuration Register 9	MB88121: 0001 0101 MB88121A/B/C: 0000 0101	r/w
0x00C4	GTUC10	GTU Configuration Register 10	MB88121: 0002 0001 MB88121A/B/C: 0002 0005	r/w
0x00C8	GTUC11	GTU Configuration Register 11	0000 0000	r/w
0x00CC - 0x00FC	-	*reserved (13)*	0000 0000	r

<table>
<tr><th>Bit</th><th>Name</th><th>Function</th></tr>
<tr><td>bit 11
bit3 – bit2</td><td>PMUL[2:0]:
PLL Multiplier Selection</td><td>These bits control the PLL multiplier. These bits must set up so that the PLL clock is set to 80MHz.

In MB88121 and MB88121A, the functionality of the PLL is not guaranteed.

For MB88121B/C, the evaluation of the PLL performance is pending. For this reason, do not use other settings than PMUL[1:0] = “11”.

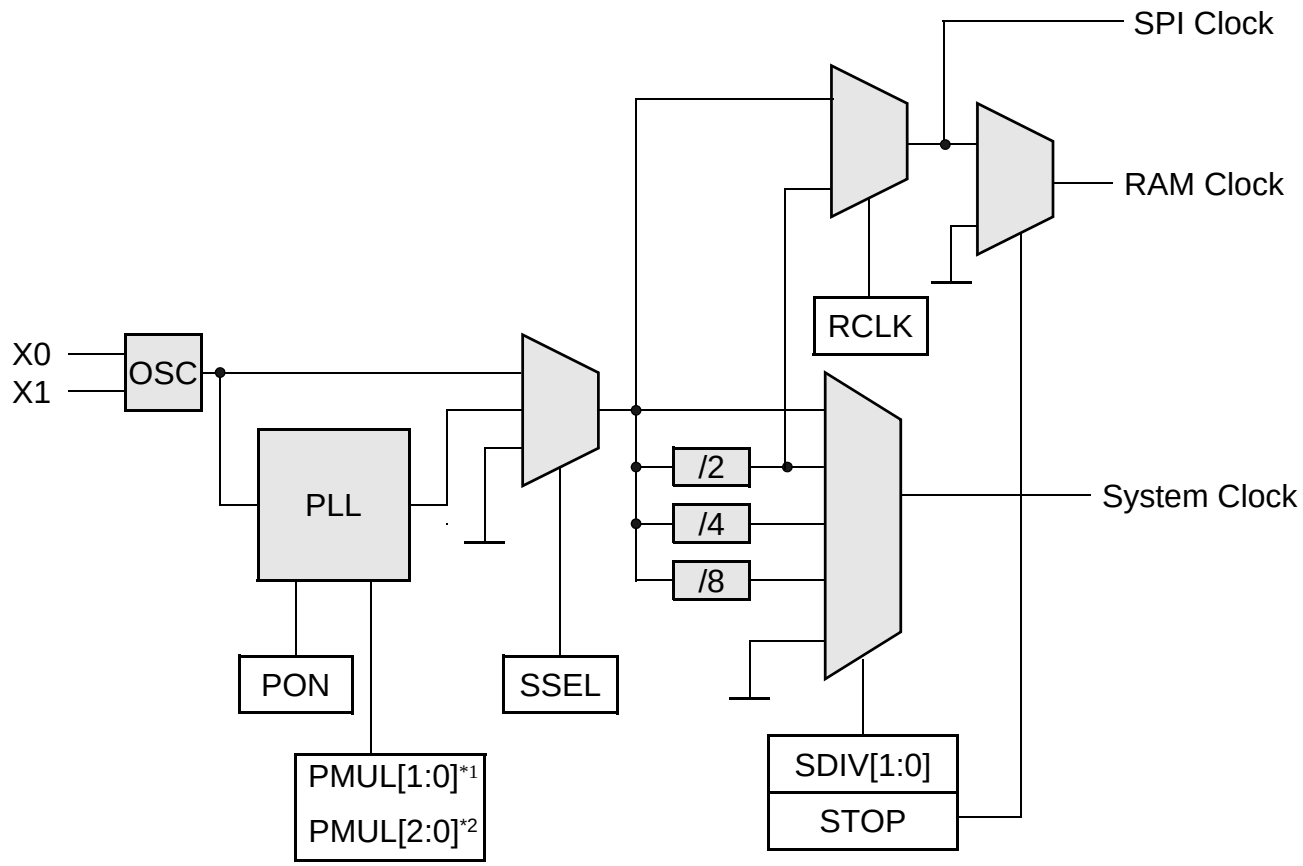
<table>
<tr><th>PMUL[2]</th><th>PMUL[1]</th><th>PMUL[0]</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>X0/X1 (4MHz) x 20 (80MHz)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>X0/X1 (5MHz) x 16 (80MHz)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>X0/X1 (8MHz) x 10 (80MHz)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>X0/X1 (10MHz) x 8 (80MHz)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>X0/X1 (16MHz) x 5 (80MHz)*1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>X0/X1 (20MHz) x 4 (80MHz)*1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>reserved</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>reserved</td></tr>
</table>
*1: MB88121C only

<<Note>>
These bits must be changed before PON bit is set to “1”.
When 16 bit parallel bus and external clock are used(MD2="1", MD1="0", MD0=“1"), the clock for X0/X1 pins can be used from 4MHz to 20MHz.
When 16 bit parallel bus and oscillator are used(MD2="1", MD1="0", MD0="0”), the clock for X0/X1 pins can be used from 4MHz to 8MHz.
When serial bus is used(MD="1", MD1="1", MD0="0") on external clock, the clock for X0/X1 pins can't be used at 16MHz and 20MHz, and on oscillator, the clock for X0/X1 pins can be used from 4MHz to 8MHz. And PMUL[2:0] bits shouldn’t be set to ”100” and “101”.
Setting to be resered is prohibition.</td></tr>
<tr><td>bit1</td><td>SSEL:
System Clock Selection</td><td>This bit selects the system clock.
"0": Select the clock of X0/X1
"1": Select the clock of PLL

In MB88121 and MB88121A, the functionality of the PLL is not guaranteed.

<<Note>>
• Must be changed into "1" from "0" after "1" is set as a PON bit and PLL lock-up time (600us) passes.
• If the oscillater of PLL is stopped, PON bit is set to "0" after this bit is changed to "0".
• When FlexRay controller can receive or transmit data, these bits must not be changed.</td></tr>
</table>

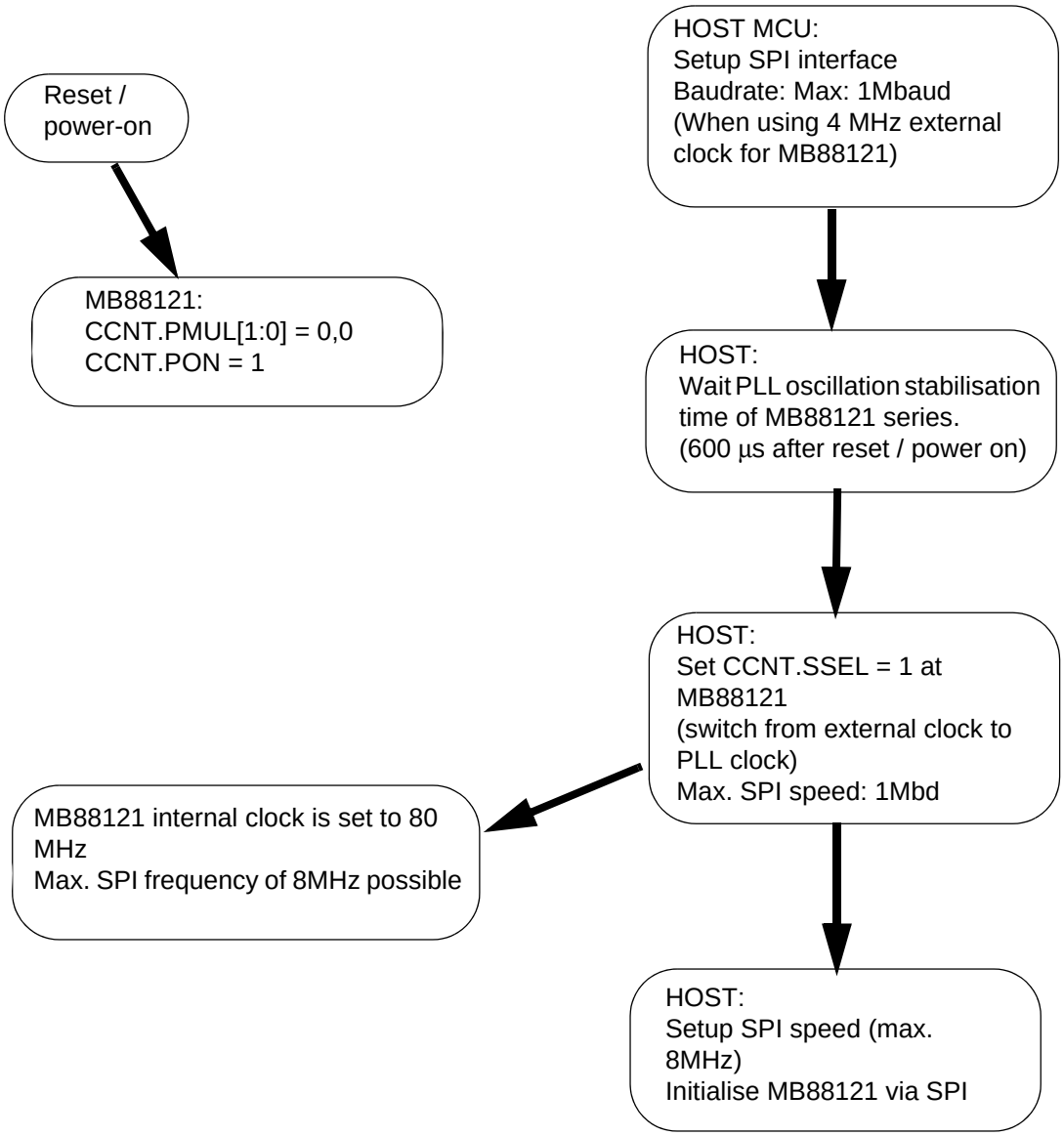
Clock supply circuit of MB88121B/C for SPI mode (MD[2:0] = 1 1 0)



*1 **MB88121B**
*2 **MB88121C**

Clock Settings after power-on / reset in SPI mode

Use of 4 MHz external crystal

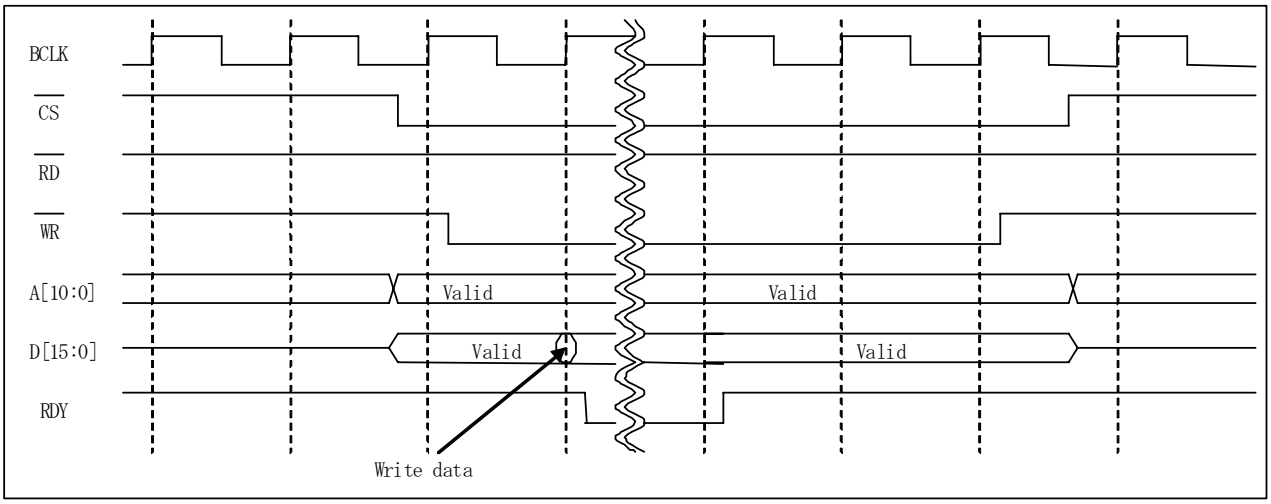


Bit	Name	Function
bit15 - bit4	RSV: Reserved	These bits are reserved. "0" is read. Write "0".
bit3	SWAP: Byte Swap Enable Bit	This bit selects whether to exchange the data handled with input/output buffer by each byte.In the case of MB88121A and MB88121B, this bit is dealt with for "0". When this bit set to "0": In this case, writing and reading are done as it is. When this bit set to "1": <460, 360 mode> When writing it in the input buffer, the data of bit 7-0 is written in bit31-24 in the input buffer. The data of bit 15-8 is written in bit23-16 in the input buffer. The data of bit 23-16 is written in bit15-8 in the input buffer. The data of bit 31-24 is written in bit7-0 in the input buffer. When it is read from the input/output buffer, the data of bit 7-0 of the input/output buffer is read as bit 31-24. The data of bit 15-8 of the input/output buffer is read as bit 23-16. The data of bit 23-16 of the input/output buffer is read as bit 15-8. The data of bit 31-24 of the input/output buffer is read as bit 7-0 <16FX mode> When writing it in the input buffer, the data of bit 7-0 is written in bit15-8 in the input buffer. The data of bit 15-8 is written in bit7-0 in the input buffer. The data of bit 23-16 is written in bit31-24 in the input buffer. The data of bit 31-24 is written in bit23-16 in the input buffer. When it is read from the input/output buffer, the data of bit 7-0 of the input/output buffer is read as bit 15-8. The data of bit 15-8 of the input/output buffer is read as bit 7-0. The data of bit 23-16 of the input/output buffer is read as bit 31-24. The data of bit 31-24 of the input/output buffer is read as bit 23-16 <<Note>> This bit is invalid serial bus mode. This bit is valid for the 16-bit parallel (non-multiplex and multi-plex).
bit2	DMAINV: DMA Request Level Inverted	This bit controls the DMA request level. "0": Active level for DMA request is "H" "1": Active level for DMA request is "L" <<Note>> It is valid when DMAOE bit is "1".
bit1	DMARE: DMA Request enable	This bit controls the DMA request. "0": Disabled "1": Enabled <<Note>> It is valid when DMAOE bit is "1".

Bit	Name	Function
Bit 31-8	*reserved*	These bits are reserved. "0" is read. Write "0".
Bit 7	LVD18CL: LVD18 clear bit	This bit clears the LVD18 bit by writing “1” “0”: LVD18 Flag not changed “1”: LVD18 Flag cleared to “0” <<Note>>: This Bit is always read as “0”
Bit 6	LVD5CL: LVD5 clear bit	This bit clears the LVD5 bit by writing “1” “0”: LVD5 Flag not changed “1”: LVD5 Flag cleared to “0” <<Note>>: This Bit is always read as “0”
Bit 5	TINTE1: TINT1 enable bit	This bit enables the Timer interrupt 1 (TINT1) signal output via the corresponding INT pin. “0”: Interrupt disabled “1”: Interrupt enabled
Bit 4	TINTE0: TINT0 enable bit	This bit enables the Timer interrupt 0 (TINT0) signal output via the corresponding INT pin. “0”: Interrupt disabled “1”: Interrupt enabled
Bit 3	LVD18E: Interrupt enable bit for LVD18	This bit enables the LVD18 flag signal output via the corresponding INT pin: “0”: Interrupt disabled “1”: Interrupt enabled
Bit 2	LVD5E: Interrupt enable bit for LVD5	This bit enables the LVD5 flag signal output via the corresponding INT pin: “0”: Interrupt disabled “1”: Interrupt enabled
Bit 1	LVD18: Low voltage detector Flag for 1.8V	This bit indicates a lov voltage detection of internal 1.8V: “0”: No undervoltage occured “1”: undervoltage occured <<Note>> This Flag is cleared by writing “1” to Bit 7 LVD18CL
Bit 0	LVD5: Low voltage detector Flag for 5V	This bit indicates a lov voltage detection of Vcc input voltage: “0”: No undervoltage occured “1”: undervoltage occured <<Note>> This Flag is cleared by writing “1” to Bit 6 LVD5CL

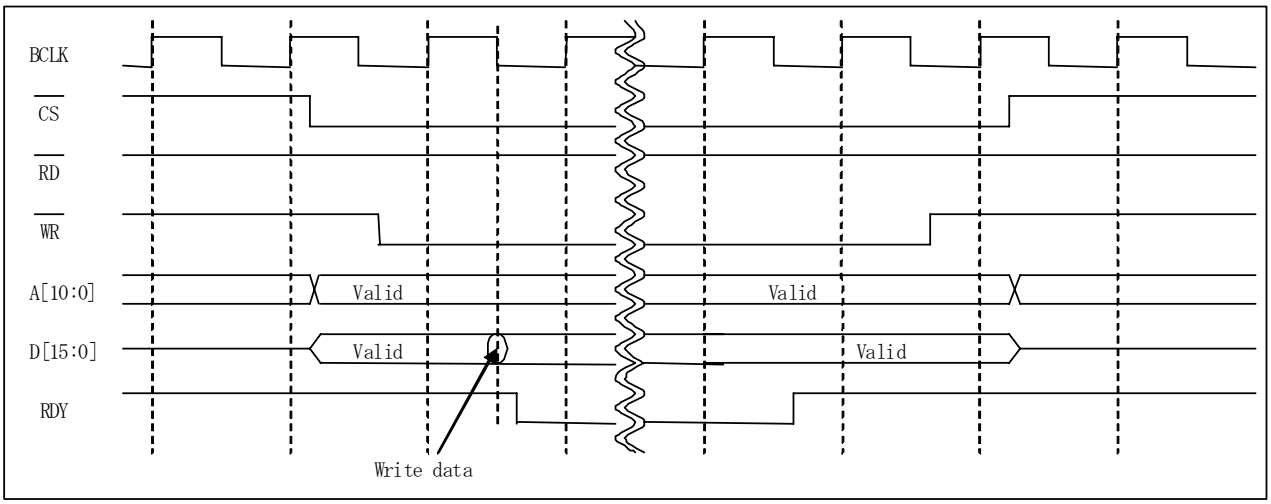
Note: In 16/bit none-multiplexed mode the LVD5, LVD18, TINT0 and TINT1 are assigned to INT2 pin. In 16 bit multiplexed or SPI mode the assignment is: TINT0 to INT2; TINT1 to INT3, LVD5 and LVD18 to INT4 pin. See also chapter “Handling Devices” topic 10 Interrupt pin assignment

Write timing in FR460 mode



When the CS pin and the WR pin become "L", the data on the D[15:0] pins is written to a temporary register at the next rising edge of the BCLK pin, and the RDY pin becomes "L", causing the CPU to wait. When the data of the temporary register is written to the register addressed by the A[10:0] pins, the RDY pin becomes "H".

Write timing in FR360 mode



When the CS pin and the WR pin become "L", the data on the D[15:0] pins is written to a temporary register at the next falling edge of the BCLK pin, and the RDY pin becomes "L", causing the CPU to wait. When the data of the temporary register is written to the register addressed by the A[10:0] pins, the RDY pin becomes "H".

4. The write timing for the register

The FlexRay Controller registers have a width of 32bit. A 32bit temporary read register is available to save write data. In the case of writing in 16bit multiplexted parallel bus mode, the temporary register is written as follows.

FR460 mode: Data of the D[15:11] pins and AD[10:0] pins is written to the 16bit upper temporary register in case of the first write access, and it is written to the 16 bit lower temporary register in case of the second write access. Then the data of the temporary register is written to the register of FlexRay controller.

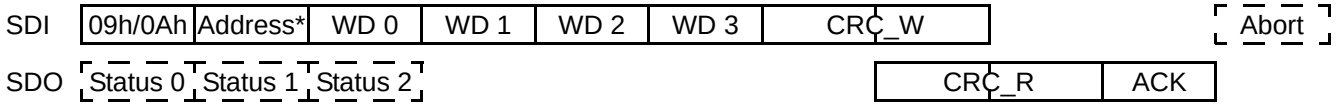
16FX mode: Data of the D[15:11] pins and AD[10:0] pins is written to the 16bit lower temporary register in case of the first write access, and it is written to the 16 bit upper temporary register in case of the second write access. Then the data of the temporary register is written to the register of FlexRay controller.

Write operation in FR460 mode

Write operation in 16FX mode

<<Note>>
As the register of the FlexRay Controller is 32bit, it must be accessed at 16bit twice continuously.

WR: Write one Word, Command Byte = 09h/0Ah

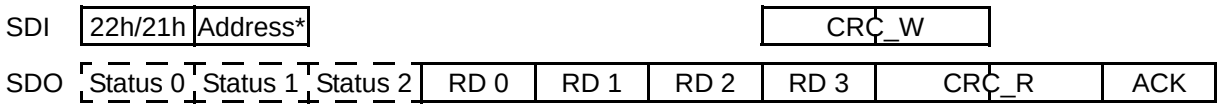


*: A[10] = bit 0 of command byte, A[9:2] = Address byte, A[1:0] = 00.

After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, 32bit of data WD[3:0] is written to the address A[10:0] if $\overline{CS}$ has a rising edge immediately after ACK. If there is no rising $\overline{CS}$ edge immediately after ACK, data is not written. The SPI master can transmit an extra byte (Abort) after it has received the ACK. MB88121 will detect clock edges when it expects a rising $\overline{CS}$ edge and will not write the data.

Payload:	4 bytes
Command length:	10 bytes
Overhead:	150%
Efficiency:	40%

RD: Read one Word, Command Byte = 22h/21h

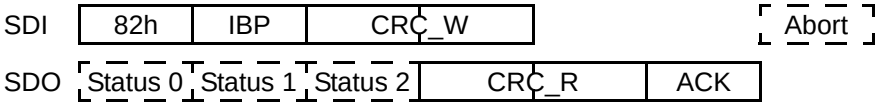


*: A[10] = bit 0 of command byte, A[9:2] = Address byte, A[1:0] = 00.

Data RD[3:0] is read from address A[10:0].
After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent.

Payload:	4 bytes
Command length:	10 bytes
Overhead:	150%
Efficiency:	40%

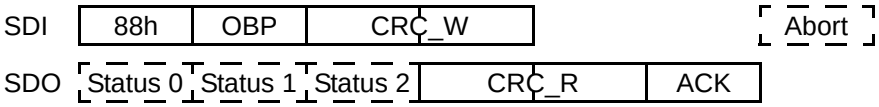
WIP: Write Input Buffer Pointer, Command Byte = 82h



After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, IBP is written if $\overline{CS}$ has a rising edge immediately after ACK. If there is no rising $\overline{CS}$ edge immediately after ACK, IBP is not written. The SPI master can transmit an extra byte (Abort) after it has received the ACK. MB88121 will detect clock edges when it expects a rising $\overline{CS}$ edge and will not write IBP. IBP is used by commands WBC, RBIWBC and RBCWBC.

Payload:	0 bytes
Command length:	6 bytes
Overhead:	6 bytes
Efficiency:	0%

WOP: Write Output Buffer Pointer, Command Byte = 88h



After successful check of CRC_W, ACK=FFh is sent. Otherwise, ACK=00h is sent. If ACK=FFh was sent, OBP is written if $\overline{CS}$ has a rising edge immediately after ACK. If there is no rising $\overline{CS}$ edge immediately after ACK, OBP is not written. The SPI master can transmit an extra byte (Abort) after it has received the ACK. MB88121 will detect clock edges when it expects a rising $\overline{CS}$ edge and will not write OBP. OBP is used by commands RBC, RBCWBI and RBCWBC.

Payload:	0 bytes
Command length:	6 bytes
Overhead:	6 bytes
Efficiency:	0%

4. Default Status Read Out

With this protocol MB88121 transmits 24 bits of status information at the beginning of each command frame.
Status Byte Overview:

STATUS 0

7	6	5	4	3	2	1	0
ST07	ST06	ST05	ST04	ST03	ST02	ST01	ST00

STATUS 1

7	6	5	4	3	2	1	0
ST17	ST16	ST15	ST14	ST13	ST12	ST11	ST10

STATUS 2

7	6	5	4	3	2	1	0
ST27	ST26	ST25	ST24	ST23	ST22	ST21	ST20

STATUS 0 Definition

Bit	Name	Function
7	ST07	reserved
6	ST06	reserved
5	ST05	reserved
4	ST04	reserved
3	ST03	reserved
2	ST02	reserved
1	ST01	eray_obusy ‘1’: Output buffer busy flag. If it is set, the output buffer is busy (0x600-0x6fc).Write access to OBCR register should not be performed. After confirming this bit is '0' by NOP command, write it in the OBCM and OBCR registers. ‘0’: Output buffer not busy
0	ST00	eray_ibusy ‘1’: Input buffer busy flag.If it is when input buffer is busy.(0x400-0x4fc).Write access to the input buffer shoud not be performed. After confirming this bit is '0' by NOP command, write it in the IBCM and IBCR registers. ‘0’: Input buffer not busy

Note: STATUS 0 register shows status of e-ray core(bit2-bit7=0). The status value is changed at falling edge of CSX.

STATUS 1 Definition

Bit	Name	Function
7	ST17	Parity error ‘1’: Parity error occured during last tranmission. ‘0’: No parity error.

Bit	Name	Function
6	ST16	Command format error ‘1’: Command format error occured at last transmission. (ie. bit2/bit0 of command first byte) is 1 (exception : command that has A[10] bit)) ‘0’: No command format error.
5	ST15	reserved
4	ST14	Undefined error ‘1’: Undifiened Command used at last transmission. ‘0’: no undefiened error.
3	ST13	Busy error ‘1’: E-Ray Communication Controller was busy and command is not executed. ‘0’: No tbusy error.
2	ST12	Long message error ‘1’: Message was too long at last transmission. ‘0’: No long message error occured
1	ST11	Short message error ‘1’: Message was too short at last transmission. ‘0’: No short message error.
0	ST10	Crc error ‘1’: CRC error at last transmission ‘0’: No CRC error.

Note: STATUS 1 register shows the status of previous SPI session. This status is cleared by eray_reset.

STATUS 2 Definition

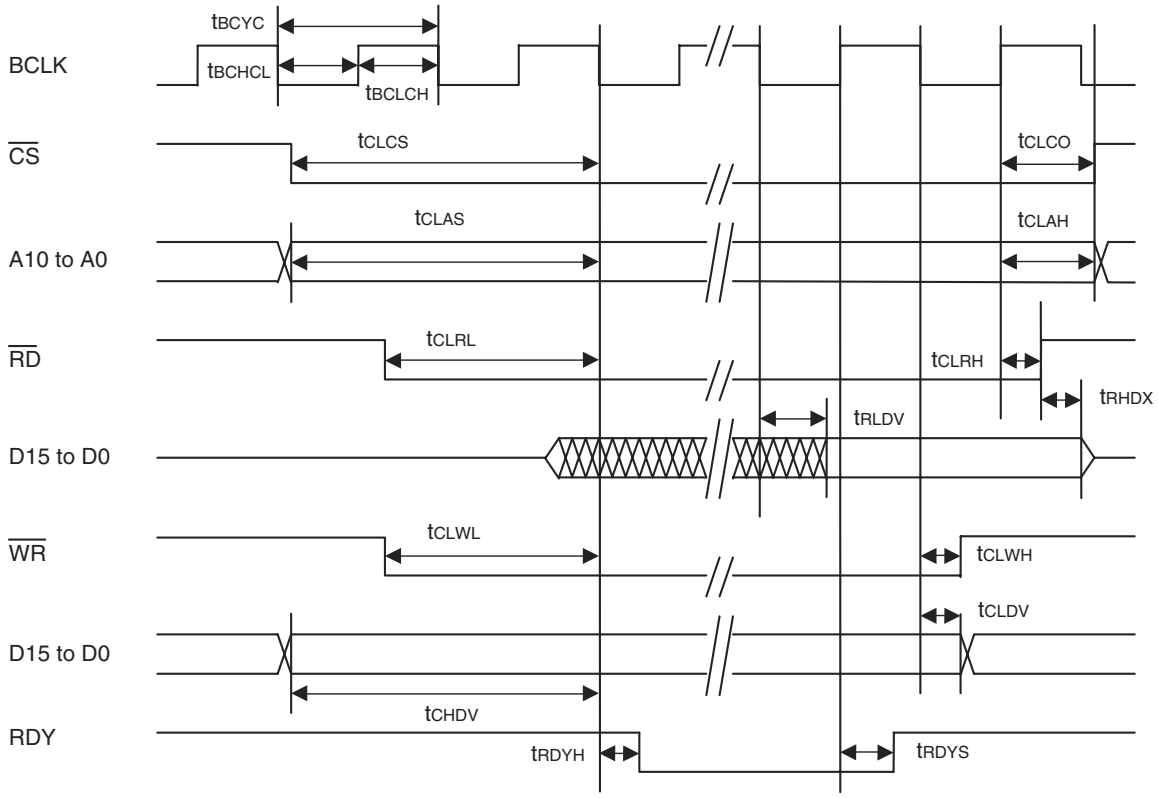
Bit	Name	Function
7	ST27	reserved
6	ST26	reserved
5	ST25	E-Ray timer 1 interrupt flag (tint1) ‘1’: E-Ray timer 1 interrupt flag is set ‘0’: No E-Ray timer 1 flag is set
4	ST24	E-Ray timer 0 interrupt flag (tint0) ‘1’: E-Ray timer 0 interrupt flag is set ‘0’: No E-Ray timer 0 flag is set
3	ST23	E-Ray interrupt lin1 (int1) flag ‘1’: E-Ray interrupt line 1 flag is set. At least one of the E-Ray line 1 assigned interrupt (EILS, SILS, EIES, SIES,ILE) flag is set. ‘0’: No E-Ray line1 interrupt.
2	ST22	E-Ray interrupt line0 (int0) flag ‘1’: E-Ray interupt line 0 flag is set. At least one of the E-Ray line 0 assigned interrupt (EILS, SILS, EIES, SIES,ILE) flag is set. ‘0’: No E-Ray line0 interrupt.
1	ST21	Status Interrupt register (SIR) flag ‘1’: At least one flag int the E-Ray Satuts interrupt register (SIR) is set to “1”. ‘0’: No SIR interrupt flag is set.

(2) 16 bit non-multiplexed mode

(MB88121/MB88121A: T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ±0.5V, V_{CC33} = 3.3 V ±0.3V, V_{CC18} = 1.8 V ±0.15V)
(MB88121B: T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)
(MB88121C: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)

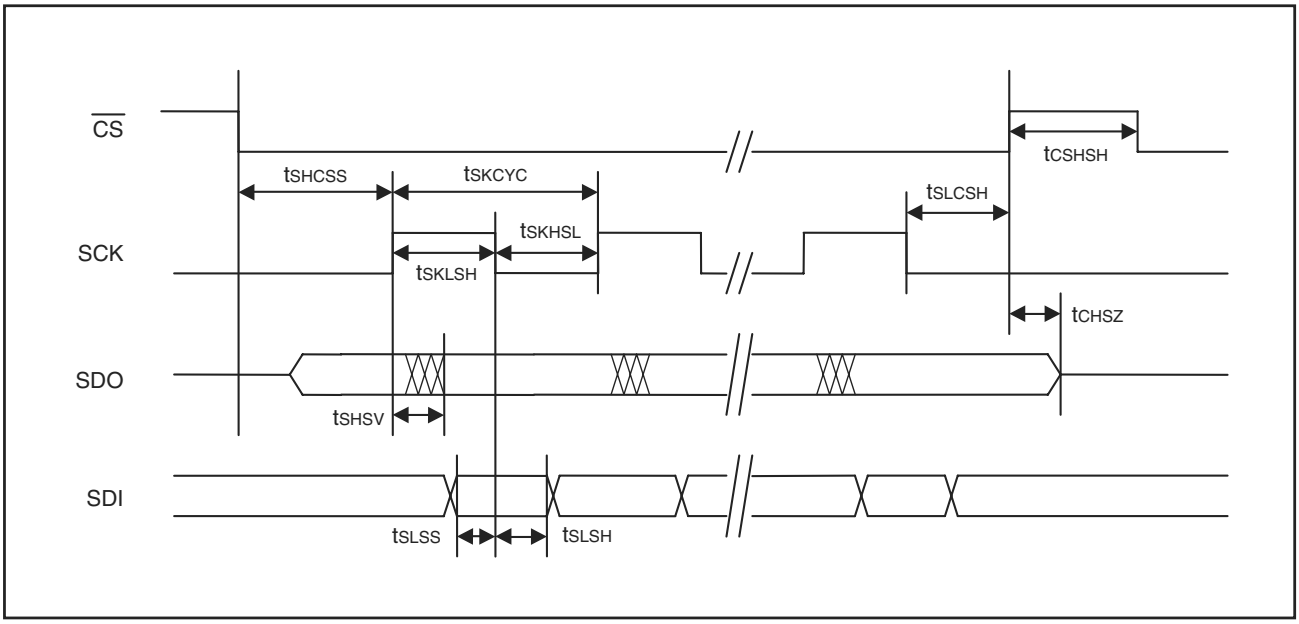
Parameter	Symbol	Condition	Timing		Unit
			Min	Max	
Bus Clock Cycle	t_{BCYC}	—	31.25	—	ns
High width of BCLK	t_{BCLCH}	—	5.0	—	ns
Low width of BCLK	t_{BCHCL}	—	5.0	—	ns
System Clock Cycle	t_{SCYC}	MB88121, MB88121A	12.5	100	ns
		MB88121B	100	250	ns
		MB88121C(Oscillator)	125	250	ns
		MB88121C(External Clock Input)	12.5	250	ns
High width of SCLK	t_{SCLCH}	MB88121, MB88121A	4.8	—	ns
		MB88121B	10	—	ns
		MB88121C(Oscillator)	10	—	ns
		MB88121C(External Clock Input)	4.8	—	ns
Low width of SCLK	t_{SCHCL}	MB88121, MB88121A	4.8	—	ns
		MB88121B	10	—	ns
		MB88121C(Oscillator)	10	—	ns
		MB88121C(External Clock Input)	4.8	—	ns
CS setup	t_{CLCS}	—	18.0	—	ns
CS hold	t_{CLCO}	—	0	—	ns
Address setup	t_{CLAS}	—	13.0	—	ns
Address hold	t_{CLAH}	—	0	—	ns
RD setup time	t_{CLRL}	—	14.0	—	ns
RD hold time	t_{CLRH}	—	0	—	ns
Data Valid delay	t_{RLDV}	C_f = 20pF (VCC = 5V)	3.0	19.0	ns
		C_f = 20pF (VCC = 3V)	3.0	30.0	ns
Data Valid hold	t_{RHDX}	C_f = 20pF	3.0	18.5	ns
WR setup time	t_{CLWL}	—	14.0	—	ns
WR hold time	t_{CLWH}	—	0	—	ns
Data setup	t_{CHDV}	—	18.0	—	ns
Data hold	t_{CLDV}	—	0	—	ns
RDY output delay	t_{RDYS}	C_f = 20pF (VCC = 5V)	—	15.4	ns
	t_{RDYS}	C_f = 20pF (VCC = 3V)	—	25.4	ns
RDY output hold	t_{RDYH}	C_f = 20pF	3.0	—	ns
RST input time	t_{RSTL}	—	200.0	—	ns

■ 16bit non-multiplexed mode(16fx)



MDS1 = 0, MDS0 = 1

(MB88121B: T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)
(MB88121C: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)



Parameter	Symbol	Condition	Timing		Unit
			Min	Max	
Cycle of SCK	t_{SKCYC}	—	6trp	—	ns
			100	—	ns
Low width of SCK	t_{SKHSL}	—	30	—	ns
High width of SCK	t_{SKLSH}	—	30	—	ns
SDO valid delay for SCK	t_{SHSV}	C_f = 20pF	—	20	ns
SDI setup time	t_{SLSS}	—	20	—	ns
SDI hold time	t_{SLSH}	—	20	—	ns
CS setup	t_{SHCSS}	—	30	—	
CS hold time	t_{SLCSH}	—	30	—	
SDO Hi-impedance delay	t_{CHSZ}	—	—	30	ns
CS recovery time	t_{CSHSH}	—	50	—	ns

*1: trp shows the RAM cycle for FlexRay

MDS1 = 1, MDS0 = 0

(MB88121B: T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)
(MB88121C: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ±0.5V / V_{CC} = 3.3 V ±0.3V)

Parameter	Symbol	Condition	Timing		Unit
			Min	Max	
Cycle of SCK	t_{SKCYC}	—	6trp	—	ns
			100	—	ns
Low width of SCK	t_{SKHSL}	—	30	—	ns
High width of SCK	t_{SKLSH}	—	30	—	ns
SDO valid delay for CS	t_{CLSV}	C_f = 20pF	—	25	ns
SDO valid delay for SCK	t_{SHSV}		—	20	ns
SDI setup time	t_{SLSS}	—	20	—	ns
SDI hold time	t_{SLSH}	—	20	—	ns
CS setup time	t_{SLCSS}	—	30	—	
CS hold time	t_{SHCSH}	—	30	—	
SDO Hi-impedance delay	t_{CHSZ}	—	—	30	ns
CS recovery time	t_{CSHSH}	—	50	—	ns

*1: trp shows the RAM cycle for FlexRay

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