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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HC08
Core Size	8-Bit
Speed	6MHz
Connectivity	I²C, USB
Peripherals	POR, PWM
Number of I/O	32
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 6x8b
Oscillator Type	Internal
Operating Temperature	0°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	42-SDIP (0.600", 15.24mm)
Supplier Device Package	42-PDIP
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc908bd48ibe

Section 12. Analog-to-Digital Converter (ADC)

Section 13. Universal Serial Bus Module (USB)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0046	Sync Processor Control Register 1 (SPCR1)	Read:	LVSIE	LVSIF	HPS1	HPS0	R	R	ATPOL	FSHF
		Write:		0						
		Reset:	0	0	0	0	0	0	0	0
$0047	H&V Sync Output Control Register (HVOCR)	Read:	R	0	0	0	0	HVOCR2	HVOCR1	HVOCR0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0048	Unimplemented	Read:								
		Write:								
		Reset:								
$0049	Port D Configuration Register (PDCR)	Read:	0	IICDATE	IICSCLE	CLAMPE	DDCSCLE	DDCDATE	USBD–E	USBD+E
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$004A	Multi-Master IIC Master Control Register (MIMCR)	Read:	MMALIF	MMNAKIF	MMBB	MMAST	MMRW	MMBR2	MMBR1	MMBR0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$004B	Multi-Master IIC Address Register (MMADR)	Read:	MMAD7	MMAD6	MMAD5	MMAD4	MMAD3	MMAD2	MMAD1	MMEXTAD
		Write:								
		Reset:	1	0	1	0	0	0	0	0
$004C	Multi-Master IIC Control Register (MMCR)	Read:	MMEN	MMIEN	0	0	MMTXAK	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$004D	Multi-Master IIC Status Register (MMSR)	Read:	MMRXIF	MMTXIF	MMATCH	MMSRW	MMRXAK	0	MMTXBE	MMRXBF
		Write:	0	0						
		Reset:	0	0	0	0	1	0	1	0
$004E	Multi-Master IIC Data Transmit Register (MMDTR)	Read:	MMTD7	MMTD6	MMTD5	MMTD4	MMTD3	MMTD2	MMTD1	MMTD0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$004F	Multi-Master IIC Data Receive Register (MMDRR)	Read:	MMRD7	MMRD6	MMRD5	MMRD4	MMRD3	MMRD2	MMRD1	MMRD0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved

Figure 2-2. Control, Status, and Data Registers (Sheet 8 of 12)

Section 3. Random-Access Memory (RAM)

3.1 Contents

3.2 Introduction

This section describes the 1,024 bytes of RAM (random-access memory).

3.3 Functional Description

Addresses $0080 through $047F are RAM locations. The location of the stack RAM is programmable. The 16-bit stack pointer allows the stack to be anywhere in the 64-Kbyte memory space.

NOTE: *For correct operation, the stack pointer must point only to RAM locations.*

Within page zero are 128 bytes of RAM. Because the location of the stack RAM is programmable, all page zero RAM locations can be used for I/O control and user data or code. When the stack pointer is moved from its reset location at $00FF out of page zero, direct addressing mode instructions can efficiently access all page zero RAM locations. Page zero RAM, therefore, provides ideal locations for frequently accessed global variables.

Before processing an interrupt, the CPU uses five bytes of the stack to save the contents of the CPU registers.

NOTE: *For M6805 compatibility, the H register is not stacked.*

4.7 FLASH Program Operation

Programming of the FLASH memory is done on a row basis. A row consists of 64 consecutive bytes starting from addresses $XX00, $XX40, $XX80, and $XXC0. Use this step-by-step procedure to program a row of FLASH memory (**Figure 4-2** is a flowchart representation):

NOTE: *In order to avoid program disturbs, the row must be erased before any byte on that row is programmed.*

1. Set the PGM bit. This configures the memory for program operation and enables the latching of address and data for programming.
2. Write any data to any FLASH address within the row address range desired.
3. Wait for a time, t_{nvs} (min. 5µs).
4. Set the HVEN bit.
5. Wait for a time, t_{pgs} (min. 10µs).
6. Write data to the FLASH address to be programmed.
7. Wait for time, t_{PROG} (min. 20µs).
8. Repeat step 6 and 7 until all the bytes within the row are programmed.
9. Clear the PGM bit.
10. Wait for time, t_{nvh} (min. 5µs).
11. Clear the HVEN bit.
12. After time, t_{rcv} (min 1µs), the memory can be accessed in read mode again.

This program sequence is repeated throughout the memory until all data is programmed.

NOTE: *Programming and erasing of FLASH locations cannot be performed by code being executed from the FLASH memory. While these operations must be performed in the order shown, other unrelated operations may occur between the steps. Do not exceed t_{PROG} maximum. See **21.15 Memory Characteristics**.*

6.3 Features

- Object code fully upward-compatible with M68HC05 Family
- 16-bit stack pointer with stack manipulation instructions
- 16-bit index register with x-register manipulation instructions
- 8-MHz CPU internal bus frequency
- 64-Kbyte program/data memory space
- 16 addressing modes
- Memory-to-memory data moves without using accumulator
- Fast 8-bit by 8-bit multiply and 16-bit by 8-bit divide instructions
- Enhanced binary-coded decimal (BCD) data handling
- Modular architecture with expandable internal bus definition for extension of addressing range beyond 64 Kbytes
- Low-power stop and wait modes

6.4 CPU Registers

Figure 6-1 shows the five CPU registers. CPU registers are not part of the memory map.

I — Interrupt Mask

When the interrupt mask is set, all maskable CPU interrupts are disabled. CPU interrupts are enabled when the interrupt mask is cleared. When a CPU interrupt occurs, the interrupt mask is set automatically after the CPU registers are saved on the stack, but before the interrupt vector is fetched.

1 = Interrupts disabled
0 = Interrupts enabled

NOTE: *To maintain M6805 Family compatibility, the upper byte of the index register (H) is not stacked automatically. If the interrupt service routine modifies H, then the user must stack and unstack H using the PSHH and PULH instructions.*

After the I bit is cleared, the highest-priority interrupt request is serviced first.

A return-from-interrupt (RTI) instruction pulls the CPU registers from the stack and restores the interrupt mask from the stack. After any reset, the interrupt mask is set and can be cleared only by the clear interrupt mask software instruction (CLI).

N — Negative flag

The CPU sets the negative flag when an arithmetic operation, logic operation, or data manipulation produces a negative result, setting bit 7 of the result.

1 = Negative result
0 = Non-negative result

Z — Zero flag

The CPU sets the zero flag when an arithmetic operation, logic operation, or data manipulation produces a result of $00.

1 = Zero result
0 = Non-zero result

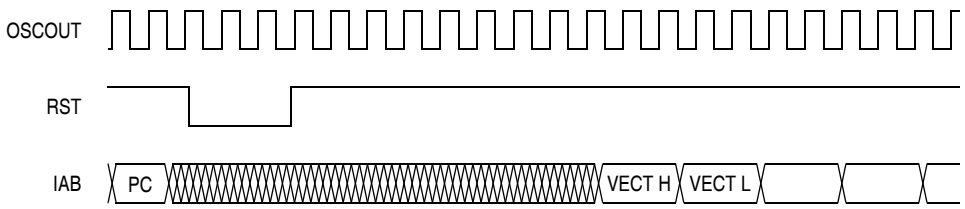


Figure 7-3. External Reset Timing

7.4.2 Active Resets from Internal Sources

SIM module in HC08 has the capability to drive the $\overline{\text{RST}}$ pin low when internal reset events occur.

All internal reset sources actively pull the $\overline{\text{RST}}$ pin low for 32 OSCXCLK cycles to allow resetting of external peripherals. The internal reset signal IRST continues to be asserted for an additional 32 cycles (see **Figure 7-4. Internal Reset Timing)**. An internal reset can be caused by an illegal address, illegal opcode, COP timeout, or POR (see **Figure 7-5. Sources of Internal Reset)**. Note that for POR resets, the SIM cycles through 4096 OSCXCLK cycles during which the SIM forces the $\overline{\text{RST}}$ pin low. The internal reset signal then follows the sequence from the falling edge of $\overline{\text{RST}}$ shown in **Figure 7-4**.

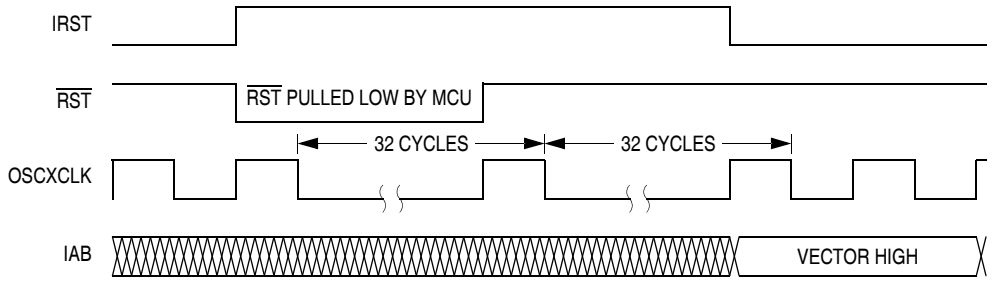


Figure 7-4. Internal Reset Timing

The COP reset is asynchronous to the bus clock.

7.8 SIM Registers

The SIM has three memory mapped registers. **Table 7-5** shows the mapping of these registers.

Table 7-5. SIM Registers Summary

Address	Register	Access Mode
$FE00	SBSR	User
$FE01	SRSR	User
$FE03	SBFCR	User

7.8.1 SIM Break Status Register (SBSR)

The SIM break status register contains a flag to indicate that a break caused an exit from stop or wait mode.

Address: $FE00

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R	R	R	R	R	R	SBSW	R
Write:							Note	
Reset:	0	0	0	0	0	0	0	0

Note: Writing a logic 0 clears SBSW. R = Reserved

Figure 7-18. SIM Break Status Register (SBSR)

SBSW — SIM Break Stop/Wait Bit

This status bit is useful in applications requiring a return to wait or stop mode after exiting from a break interrupt. Clear SBSW by writing a logic 0 to it. Reset clears SBSW.

1 = Stop mode or wait mode was exited by break interrupt
0 = Stop mode or wait mode was not exited by break interrupt

MSxB — Mode Select Bit B

This read/write bit selects buffered output compare/PWM operation. MSxB exists only in the TIM channel 0 status and control register.

Setting MS0B disables the channel 1 status and control register and reverts TCH1 to general-purpose I/O.

Reset clears the MSxB bit.

1 = Buffered output compare/PWM operation enabled
0 = Buffered output compare/PWM operation disabled

MSxA — Mode Select Bit A

When ELSxB:A ≠ 00, this read/write bit selects either input capture operation or unbuffered output compare/PWM operation. See **Table 10-4**.

1 = Unbuffered output compare/PWM operation
0 = Input capture operation

When ELSxB:A = 00, this read/write bit selects the initial output level of the TCHx pin. (See **Table 10-4**.). Reset clears the MSxA bit.

1 = Initial output level low
0 = Initial output level high

NOTE: *Before changing a channel function by writing to the MSxB or MSxA bit, set the TSTOP and TRST bits in the TIM status and control register (TSC).*

ELSxB and ELSxA — Edge/Level Select Bits

When channel x is an input capture channel, these read/write bits control the active edge-sensing logic on channel x.

When channel x is an output compare channel, ELSxB and ELSxA control the channel x output behavior when an output compare occurs.

When ELSxB and ELSxA are both clear, channel x is not connected to an I/O port , and pin TCHx is available as a general-purpose port I/O pin. **Table 10-4** shows how ELSxB and ELSxA work. Reset clears the ELSxB and ELSxA bits.

Section 11. Pulse Width Modulator (PWM)

11.1 Contents

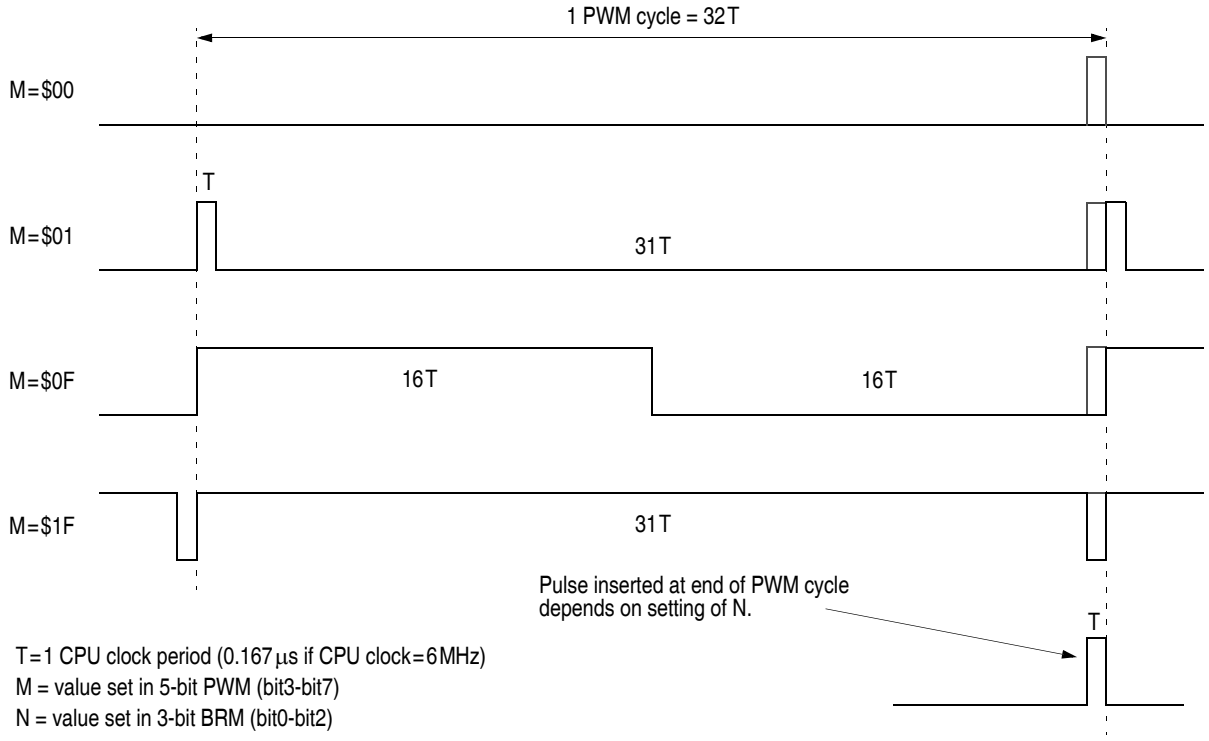
11.2 Introduction

Sixteen 8-bits PWM channels are available on the MC68HC908BD48. Channels 0 to 7 are shared with port-B I/O pins under the control of the PWM control register 1. Channels 8 to 15 are shared with port-A I/O pins under the control of the PWM control register 2.

11.3 Functional Description

Each 8-bit PWM channel is composed of an 8-bit register which contains a 5-bit PWM in MSB portion and a 3-bit binary rate multiplier (BRM) in LSB portion. There are 16 PWM data registers as shown in **Table 11-1**. The value programmed in the 5-bit PWM portion will determine the pulse length of the output. The clock to the 5-bit PWM portion is the system clock, the repetition rate of the output is hence 187.5KHz at 6MHz clock.

The 3-bit BRM will generate a number of narrow pulses which are equally distributed among an 8-PWM-cycle frame. The number of pulses generated is equal to the number programmed in the 3-bit BRM portion. Examples of the waveforms are shown in **Figure 11-3**.



N	PWM cycles where pulses are inserted in a 8-cycle frame	Number of inserted pulses in a 8-cycle frame
xx1	4	1
x1x	2, 6	2
1xx	1, 3, 5, 7	4

Figure 11-3. 8-Bit PWM Output Waveforms

12.7.1 ADC Voltage In (ADCVIN)

ADCVIN is the input voltage signal from one of the 6 ADC channels to the ADC module.

12.8 I/O Registers

Three I/O registers control and monitor ADC operation:

- ADC status and control register (ADSCR, $005D)
- ADC data register (ADR, $005E)
- ADC clock register (ADICLK, $005F)

12.8.1 ADC Status and Control Register

The following paragraphs describe the function of the ADC status and control register.

Address: $005D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	COCO	AIEN	ADCO	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
Write:								
Reset:	0	0	0	1	1	1	1	1

= Unimplemented

Figure 12-2. ADC Status and Control Register (ADSCR)

COCO — Conversions Complete Bit

When the AIEN bit is a logic 0, the COCO is a read-only bit which is set each time a conversion is completed. This bit is cleared whenever the ADC status and control register is written or whenever the ADC data register is read. Reset clears this bit.

1 = conversion completed (AIEN = 0)

0 = conversion not completed (AIEN = 0)

When the AIEN bit is a logic 1 (CPU interrupt enabled), the COCO is a read-only bit, and will always be logic 0 when read.

Section 13. Universal Serial Bus Module (USB)

13.1 Contents

13.2 Introduction

This USB module is designed to serve as a low-speed (LS) USB device per the *Universal Serial Bus Specification* Rev 1.0.

Three types of USB data transfers are supported: control, interrupt, and bulk (transmit only). Endpoint 0 functions as a receive/transmit control endpoint. Endpoints 1 and 2 can function as interrupt or bulk, but only in transmit direction.

SRW — DDC Slave Read/Write

This bit indicates the data direction when the module is in slave mode. It is updated after the calling address is received from a master device. SRW = 1 when the calling master is reading data from the module (slave transmit mode). SRW = 0 when the master is writing data to the module (receive mode).

1 = Slave mode transmit
0 = Slave mode receive

RXAK — DDC Receive Acknowledge

When this bit is cleared, it indicates an acknowledge signal has been received after the completion of 8 data bits transmission on the bus. When RXAK is set, it indicates no acknowledge signal has been detected at the 9th clock; the module will release the SDA line for the master to generate "stop" or "repeated start" condition. Reset sets this bit.

1 = No acknowledge signal received at 9th clock bit
0 = Acknowledge signal received at 9th clock bit

SCLIF — SCL Interrupt Flag

This flag is set when a falling edge is detected on the SCL line, only if DDC1EN bit is set. SCLIF generates an interrupt request to CPU if the SCLIEN bit in DCR is also set. SCLIF is cleared by writing "0" to it or when the DCC1EN = 0, or DEN = 0. Reset clears this bit.

1 = Falling edge detected on SCL line
0 = No falling edge detected on SCL line

TXBE — DDC Transmit Buffer Empty

This flag indicates the status of the data transmit register (DDTR). When the CPU writes the data to the DDTR, the TXBE flag will be cleared. TXBE is set when DDTR is emptied by a transfer of its data to the output circuit. Reset sets this bit.

1 = Data transmit register empty
0 = Data transmit register full

16.5.1 Polarity Detection

16.5.1.1 Hsync Polarity Detection

The Hsync polarity detection circuit measures the length of high and low period of the HSYNC input. If the length of high is longer than *L* and the length of low is shorter than *S*, the HPOL bit will be "0", indicating a negative polarity HSYNC input. If the length of low is longer than *L* and the length of high is shorter than *S*, the HPOL bit will be "1", indicating a positive polarity HSYNC input. The table below shows three possible cases for HSYNC polarity detection — the conditions are selected by the HPS[1:0] bits in the Sync Processor Control Register 1 (SPCR1).

Polarity Detection Pulse Width		**SPCR1 ($0046)**	
Long is greater than (*L*)	**Short is less than (*S*)**	**HPS1**	**HPS0**
7µs	6µs	0	0
3.5µs	3µs	1	X
14µs	12µs	0	1

16.5.1.2 Vsync Polarity Detection

The Vsync polarity detection circuit performs a similar function as for Hsync. If the length of high is longer than 4ms and the length of low is shorter than 2ms, the VPOL bit will be "0", indicating a negative polarity VSYNC input. If the length of low is longer than 4ms and the length of high is shorter than 2ms, the VPOL bit will be "1", indicating a positive polarity VSYNC input.

16.5.1.3 Composite Sync Polarity Detection

When a composite sync signal is the input (COMP = 1 for composite sync processing), the HPOL bit = VPOL bit, and the polarity is detected using the VSYNC polarity detection criteria described in section **16.5.1.2**.

16.5.5 Low Vertical Frequency Detect

Logic monitors the value of the Vsync Frequency Register (VFR), and sets the low vertical frequency flag (LVSIF) when the value of VFR is higher than $C00 (frequency below 40.7Hz). LVSIF bit can generate an interrupt request to the CPU when the LVSIE bit is set and I-bit in the Condition Code Register is "0". The LVSIF bit can help the system to detect video off mode fast.

16.6 Registers

Eight registers are associated with the Sync Processor, they outlined in the following sections.

16.6.1 Sync Processor Control & Status Register (SPCSR)

Address: $0040

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	VSIE	VEDGE	VSIF	COMP	VINVO	HINVO	VPOL	HPOL
Write:			0					
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 16-3. Sync Processor Control & Status Register (SPCSR)

VSIE — VSync Interrupt Enable

When this bit is set, the VSIF flag is enabled to generate an interrupt request to the CPU. When VSIE is cleared, the VSIF flag is prevented from generating an interrupt request to the CPU. Reset clears this bit.

1 = VSIF bit set will generate interrupt request to CPU

0 = VSIF bit set does not generate interrupt request to CPU

20.3 Features

Features of the break module include:

- Accessible input/output (I/O) registers during the break interrupt
- CPU-generated break interrupts
- Software-generated break interrupts
- COP disabling during break interrupts

20.4 Functional Description

When the internal address bus matches the value written in the break address registers, the break module issues a breakpoint signal to the CPU. The CPU then loads the instruction register with a software interrupt instruction (SWI) after completion of the current CPU instruction. The program counter vectors to $FFFC and $FFFD ($FEFC and $FEFD in monitor mode).

The following events can cause a break interrupt to occur:

- A CPU-generated address (the address in the program counter) matches the contents of the break address registers.
- Software writes a logic 1 to the BRKA bit in the break status and control register.

When a CPU-generated address matches the contents of the break address registers, the break interrupt begins after the CPU completes its current instruction. A return-from-interrupt instruction (RTI) in the break routine ends the break interrupt and returns the MCU to normal operation. **Figure 20-1** shows the structure of the break module.

21.4 Functional Operating Range

Characteristic	Symbol	Value	Unit
Operating Temperature Range	T_A	0 to 85	°C
Operating Voltage Range	V_{DD}	4.5 to 5.5	V

21.5 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance QFP (44 Pins) SDIP (42 Pins)	θ_{JA}	 95 60	°C/W
I/O Pin Power Dissipation	$P_{I/O}$	User Determined	W
Power Dissipation(1)	P_D	$P_D = (I_{DD} \times V_{DD}) + P_{I/O} = K/(T_J + 273\ °C)$	W
Constant(2)	K	$P_D \times (T_A + 273\ °C) + P_D^2 \times \theta_{JA}$	W/°C
Average Junction Temperature	T_J	$T_A + (P_D \times \theta_{JA})$	°C
Maximum Junction Temperature	T_{JM}	100	°C

NOTES:

1. Power dissipation is a function of temperature.
2. K is a constant unique to the device. K can be determined for a known T_A and measured P_D. With this value of K, P_D and T_J can be determined for any value of T_A.

21.9 ADC Characteristics

Characteristic[1]	Symbol	Min	Max	Unit	Comments
Supply voltage	V_{DDAD}	4.5 (V_{DD} min)	5.5 (V_{DD} max)	V	
Input voltages	V_{ADIN}	0	$\frac{2}{3} V_{DD}$	V	
Resolution	B_{AD}	8	8	Bits	
Absolute accuracy (V_{SS} = 0 V, V_{DD} = 5 V ± 10%)	A_{AD}	—	± 2	LSB	Includes quantization
ADC internal clock	f_{ADIC}	0.375	6	MHz	$t_{AIC} = 1/f_{ADIC}$, tested only at 1.5 MHz
Conversion range	R_{AD}	V_{SS}	$\frac{2}{3} V_{DD}$	V	
Power-up time	t_{ADPU}	16		t_{AIC} cycles	
Conversion time	t_{ADC}	12	13	t_{AIC} cycles	
Sample time[2]	t_{ADS}	4	—	t_{AIC} cycles	
Zero input reading[3]	Z_{ADI}	00	02	Hex	
Full-scale reading[3]	F_{ADI}	FD	FF	Hex	
Input capacitance	C_{ADI}	—	8	pF	Not tested
Input leakage[4] Port C	—	—	± 1	µA	

NOTES:
1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted.
2. Source impedances greater than 10 kΩ adversely affect internal RC charging time during input sampling.
3. Zero-input/full-scale reading requires sufficient decoupling measures for accurate conversions.
4. The external system error caused by input leakage current is approximately equal to the product of R source and input current.