Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	EE PLD
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	8
Number of Gates	-
Number of I/O	-
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	24-DIP (0.300", 7.62mm)
Supplier Device Package	24-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/gal20v8b-15lpni

GAL20V8

High Performance E²CMOS PLD Generic Array Logic™

Lead-Free Package Options Available!

Features

- HIGH PERFORMANCE E²CMOS® TECHNOLOGY
  - 5 ns Maximum Propagation Delay
  - Fmax = 166 MHz
  - 4 ns Maximum from Clock Input to Data Output
  - UltraMOS® Advanced CMOS Technology
- 50% to 75% REDUCTION IN POWER FROM BIPOLAR
  - 75mA Typ Icc on Low Power Device
  - 45mA Typ Icc on Quarter Power Device
- ACTIVE PULL-UPS ON ALL PINS
- E² CELL TECHNOLOGY
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention
- EIGHT OUTPUT LOGIC MACROCELLS
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity
  - Also Emulates 24-pin PAL® Devices with Full Function/ Fuse Map/Parametric Compatibility
- PRELOAD AND POWER-ON RESET OF ALL REGISTERS
  - 100% Functional Testability
- APPLICATIONS INCLUDE:
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- ELECTRONIC SIGNATURE FOR IDENTIFICATION
- LEAD-FREE PACKAGE OPTIONS

Functional Block Diagram

Description

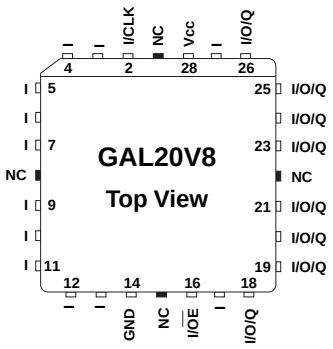
The GAL20V8C, at 5ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL20V8 are the PAL architectures listed in the table of the macrocell description section. GAL20V8 devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

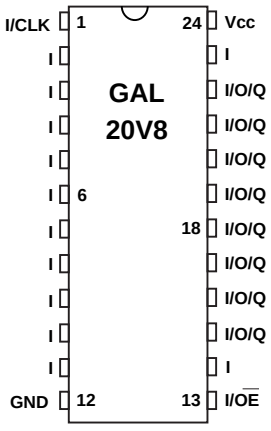
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Pin Configuration

PLCC



DIP



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
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August 2006

GAL20V8 Ordering Information

Conventional Packaging
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
5	3	4	115	GAL20V8C-5LJ[1]	28-Lead PLCC
7.5	7	5	115	GAL20V8C-7LJ	28-Lead PLCC
			115	GAL20V8B-7LP[1]	24-Pin Plastic DIP
10	10	7	115	GAL20V8C-10LJ	28-Lead PLCC
			115	GAL20V8B-10LP	24-Pin Plastic DIP
15	12	10	55	GAL20V8B-15QP	24-Pin Plastic DIP
			55	GAL20V8B-15QJ	28-Lead PLCC
			90	GAL20V8B-15LP	24-Pin Plastic DIP
			90	GAL20V8B-15LJ	28-Lead PLCC
25	15	12	55	GAL20V8B-25QP	24-Pin Plastic DIP
			55	GAL20V8B-25QJ	28-Lead PLCC
			90	GAL20V8B-25LP	24-Pin Plastic DIP
			90	GAL20V8B-25LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	10	7	130	GAL20V8C-10LJI	28-Lead PLCC
			130	GAL20V8B-10LPI[1]	24-Pin Plastic DIP
			130	GAL20V8B-10LJI	28-Lead PLCC
15	12	10	130	GAL20V8B-15LPI	24-Pin Plastic DIP
			130	GAL20V8B-15LJI	28-Lead PLCC
20	13	11	65	GAL20V8B-20QPI	24-Pin Plastic DIP
			65	GAL20V8B-20QJI	28-Lead PLCC
25	15	12	65	GAL20V8B-25QPI	24-Pin Plastic DIP
			65	GAL20V8B-25QJI	28-Lead PLCC
			130	GAL20V8B-25LPI	24-Pin Plastic DIP
			130	GAL20V8B-25LJI	28-Lead PLCC

1. Discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

Lead-Free Packaging
Commercial Grade Specifications

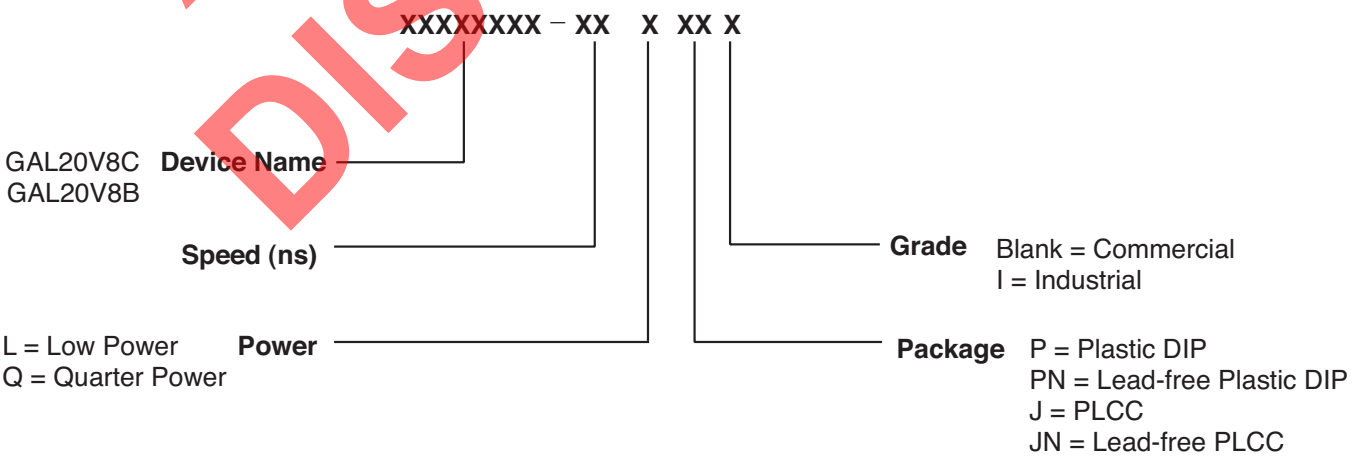
Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
5	3	4	115	GAL20V8C-5LJN[1]	Lead-Free 28-Lead PLCC
7.5	7	5	115	GAL20V8C-7LJN	Lead-Free 28-Lead PLCC
			115	GAL20V8B-7LPN[1]	Lead-Free 24-Pin Plastic DIP
10	10	7	115	GAL20V8C-10LJN	Lead-Free 28-Lead PLCC
			115	GAL20V8B-10LPN	Lead-Free 24-Pin Plastic DIP
15	12	10	55	GAL20V8B-15QJN	Lead-Free 28-Lead PLCC
			55	GAL20V8B-15QPN	Lead-Free 24-Pin Plastic DIP
			90	GAL20V8B-15LJN	Lead-Free 28-Lead PLCC
			90	GAL20V8B-15LPN	Lead-Free 24-Pin Plastic DIP
25	15	12	55	GAL20V8B-25QJN	Lead-Free 28-Lead PLCC
			55	GAL20V8B-25QPN	Lead-Free 24-Pin Plastic DIP
			90	GAL20V8B-25LJN	Lead-Free 28-Lead PLCC
			90	GAL20V8B-25LPN	Lead-Free 24-Pin Plastic DIP

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	10	7	130	GAL20V8C-10LJNI	Lead-Free 28-Pin Plastic DIP
			130	GAL20V8B-10LPNI[1]	Lead-Free 24-Pin Plastic DIP
15	12	10	130	GAL20V8B-15LJNI	Lead-Free 28-Lead PLCC
			130	GAL20V8B-15LPNI	Lead-Free 24-Pin Plastic DIP
20	13	11	65	GAL20V8B-20QJNI	Lead-Free 28-Lead PLCC
			65	GAL20V8B-20QPNI	Lead-Free 24-Pin Plastic DIP
25	15	12	65	GAL20V8B-25QJNI	Lead-Free 28-Lead PLCC
			65	GAL20V8B-25QPNI	Lead-Free 24-Pin Plastic DIP
			130	GAL20V8B-25LJNI	Lead-Free 28-Lead PLCC
			130	GAL20V8B-25LPNI	Lead-Free 24-Pin Plastic DIP

1. Discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

Part Number Description



Registered Mode

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

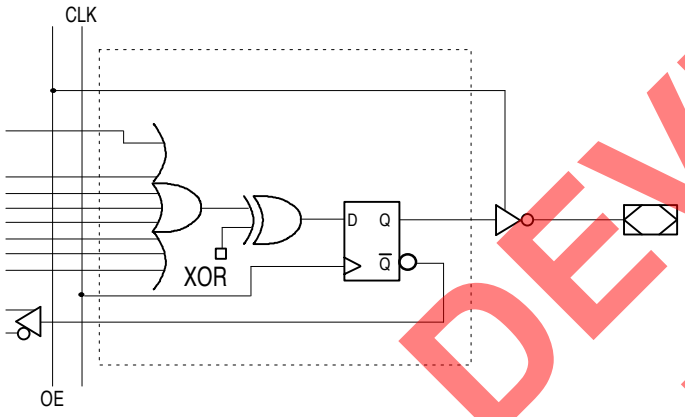
Architecture configurations available in this mode are similar to the common 20R8 and 20RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/Os are possible in this mode.

Dedicated input or output functions can be implemented as subsets of the I/O function.

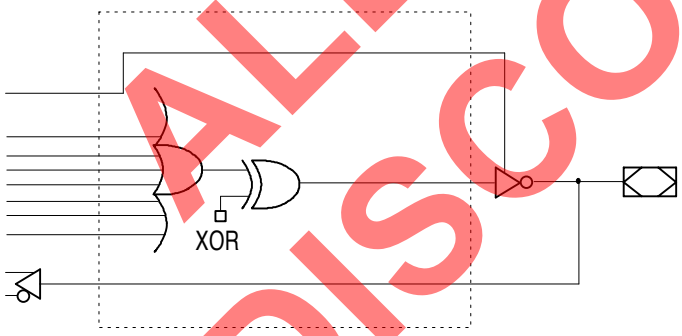
Registered outputs have eight product terms per output. I/Os have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 1 controls common CLK for the registered outputs.
- Pin 13 controls common $\overline{OE}$ for the registered outputs.
- Pin 1 & Pin 13 are permanently configured as CLK & $\overline{OE}$ for registered output configuration.



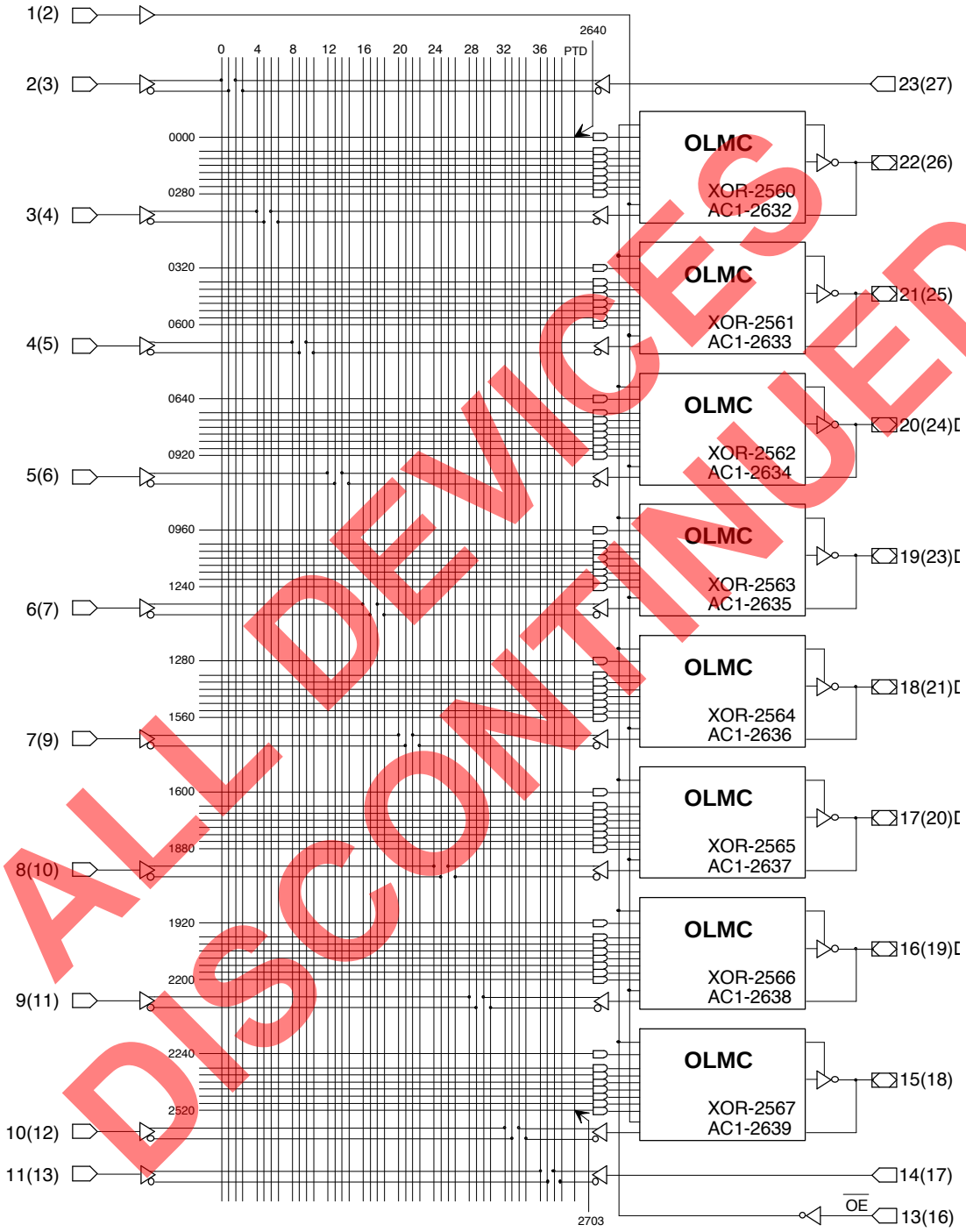
Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 1 & Pin 13 are permanently configured as CLK & $\overline{OE}$ for registered output configuration..

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Registered Mode Logic Diagram

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte 7 | Byte 6	.... Byte 1 | Byte 0

MSB LSB

SYN-2704
AC0-2705

Complex Mode

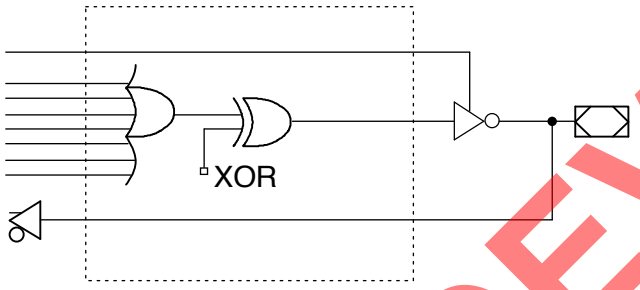
In the Complex mode, macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 20L8 and 20P8 devices with programmable polarity in each macrocell.

Up to six I/Os are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 15 & 22) do not have input capability. Designs requiring eight I/Os can be implemented in the Registered mode.

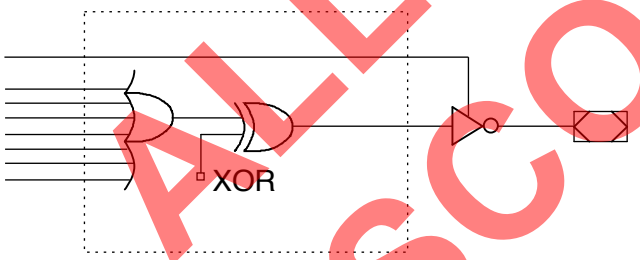
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 13 are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 16 through Pin 21 are configured to this function.



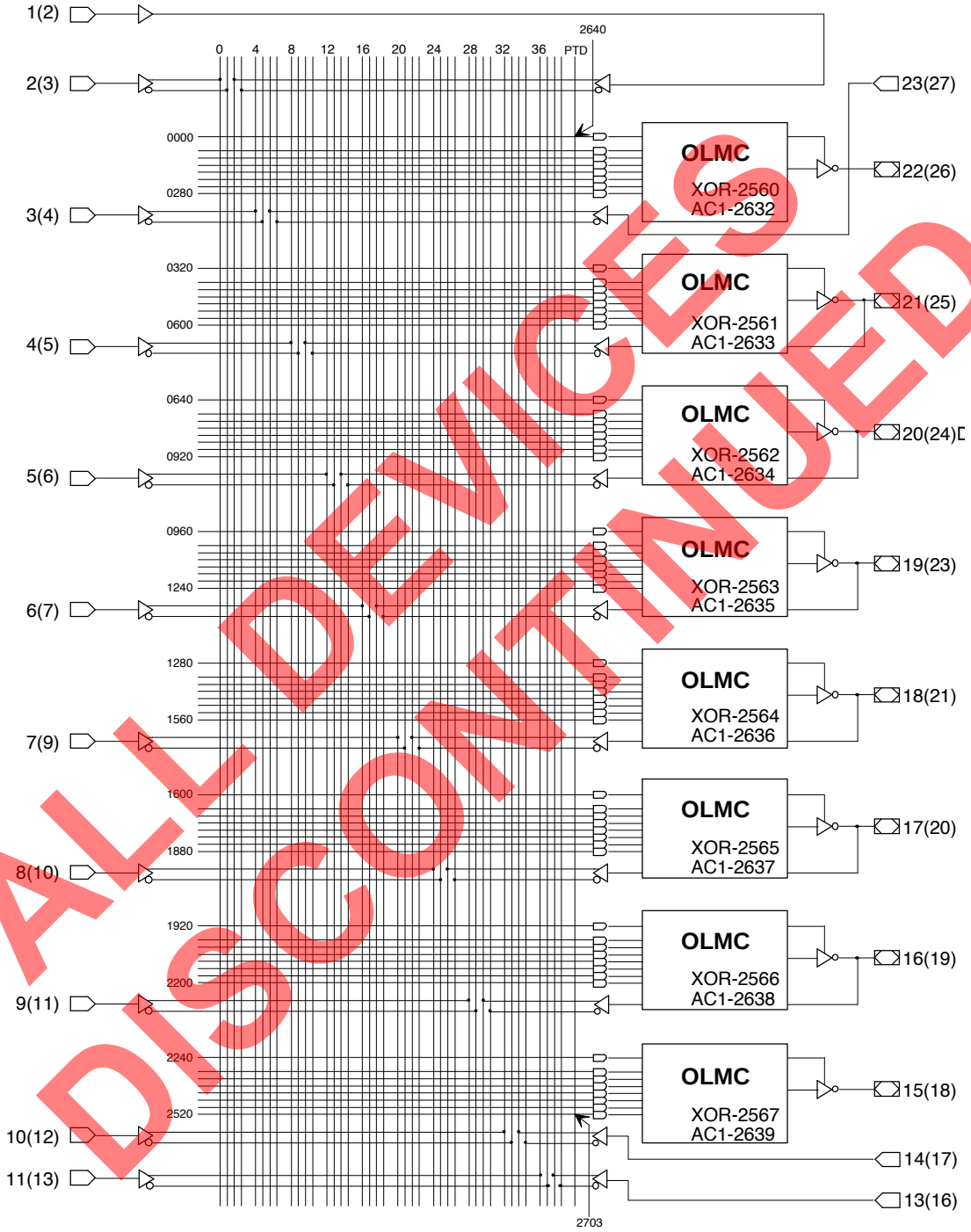
Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 15 and Pin 22 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Complex Mode Logic Diagram

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte 7 | Byte 6	.... Byte 1 | Byte 0

MSB LSB

SYN-2704
AC0-2705

Simple Mode

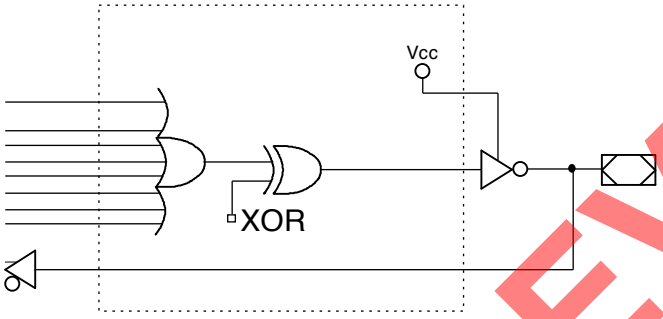
In the Simple mode, pins are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 14L8 and 16P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

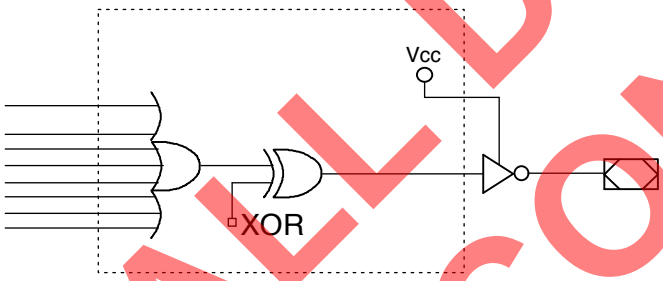
Pins 1 and 13 are always available as data inputs into the AND array. The "center" two macrocells (pins 18 and 19) cannot be used in the input configuration.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



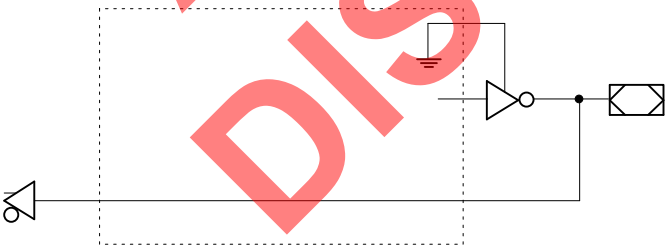
Combinatorial Output with Feedback Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- All OLMC **except** pins 18 & 19 can be configured to this function.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- Pins 18 & 19 are permanently configured to this function.



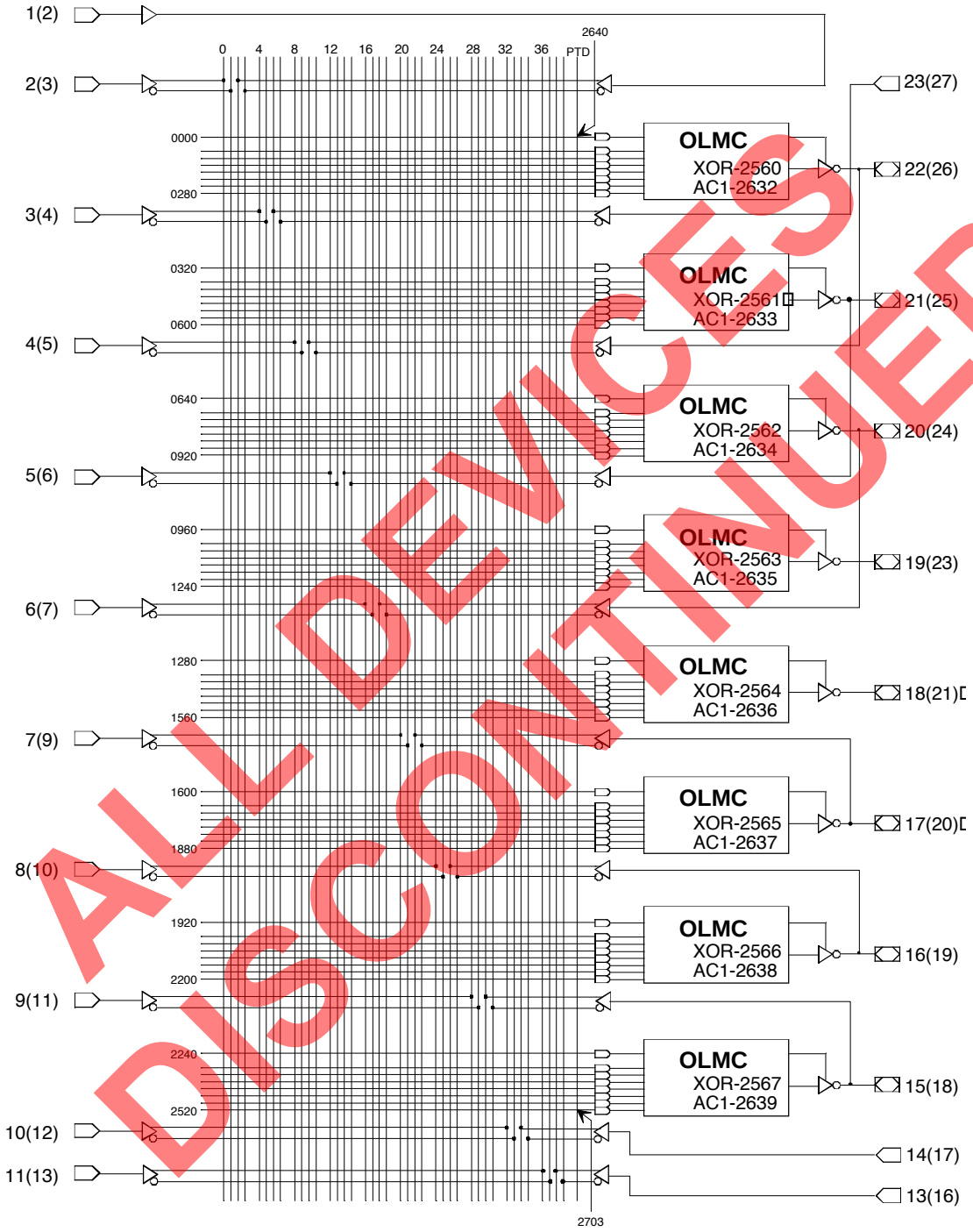
Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- All OLMC **except** pins 18 & 19 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Simple Mode Logic Diagram

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte 7 | Byte 6	.... Byte 1 | Byte 0

MSB LSB

SYN-2704
AC0-2705

AC Switching Characteristics

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION		COM -5 MIN.	COM -5 MAX.	COM -7 MIN.	COM -7 MAX.	COM/IND -10 MIN.	COM/IND -10 MAX.	UNITS
tpd	A	Input or I/O to Comb. Output	8 outputs switching	1	5	3	7.5	3	10	ns
			1 output switching	—	—	—	7	—	—	ns
tco	A	Clock to Output Delay		1	4	2	5	2	7	ns
tcf[2]	—	Clock to Feedback Delay		—	3	—	3	—	6	ns
tsu	—	Setup Time, Input or Feedback before Clock↑		3	—	5	—	7.5	—	ns
th	—	Hold Time, Input or Feedback after Clock↑		0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)		142.8	—	100	—	66.7	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)		166	—	125	—	71.4	—	MHz
	A	Maximum Clock Frequency with No Feedback		166	—	125	—	83.3	—	MHz
twh	—	Clock Pulse Duration, High		3	—	4	—	6	—	ns
twl	—	Clock Pulse Duration, Low		3	—	4	—	6	—	ns
ten	B	Input or I/O to Output Enabled		1	6	3	9	3	10	ns
	B	$\overline{OE}$ to Output Enabled		1	6	2	6	2	10	ns
tdis	C	Input or I/O to Output Disabled		1	5	2	9	2	10	ns
	C	$\overline{OE}$ to Output Disabled		1	5	1.5	6	1.5	10	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section. Characterized initially and after any design or process changes that may affect these parameters.

Capacitance (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested

Absolute Maximum Ratings(1)

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature (T_A) ..... –40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	24	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–150	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	**L** -7/-10	—	75	115	mA
			L -15/-25	—	75	90	mA
			Q -15/-25	—	45	55	mA

INDUSTRIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	**L** -10/-15/-25	—	75	130	mA
			Q -20/-25	—	45	65	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

AC Switching Characteristics

Over Recommended Operating Conditions

PARAM.	TEST COND[1].	DESCRIPTION		COM -7 MIN.	COM -7 MAX.	COM / IND -10 MIN.	COM / IND -10 MAX.	COM / IND -15 MIN.	COM / IND -15 MAX.	IND -20 MIN.	IND -20 MAX.	COM / IND -25 MIN.	COM / IND -25 MAX.	UNITS
t_{pd}	A	Input or I/O to	8 outputs switching	3	7.5	3	10	3	15	3	20	3	25	ns
		Comb. Output	1 output switching	—	7	—	—	—	—	—	—	—	—	ns
t_{co}	A	Clock to Output Delay		2	5	2	7	2	10	2	11	2	12	ns
t_{cf}[2]	—	Clock to Feedback Delay		—	3	—	6	—	8	—	9	—	10	ns
t_{su}	—	Setup Time, Input or Fdbk before Clk↑		7	—	10	—	12	—	13	—	15	—	ns
t_{h}	—	Hold Time, Input or Fdbk after Clk↑		0	—	0	—	0	—	0	—	0	—	ns
f_{max}[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)		83.3	—	58.8	—	45.5	—	41.6	—	37	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)		100	—	62.5	—	50	—	45.4	—	40	—	MHz
	A	Maximum Clock Frequency with No Feedback		100	—	62.5	—	62.5	—	50	—	41.7	—	MHz
t_{wh}	—	Clock Pulse Duration, High		5	—	8	—	8	—	10	—	12	—	ns
t_{wl}	—	Clock Pulse Duration, Low		5	—	8	—	8	—	10	—	12	—	ns
t_{en}	B	Input or I/O to Output Enabled		3	9	3	10	—	15	—	18	—	25	ns
	B	$\overline{OE}$ to Output Enabled		2	6	2	10	—	15	—	18	—	20	ns
t_{dis}	C	Input or I/O to Output Disabled		2	9	2	10	—	15	—	18	—	25	ns
	C	$\overline{OE}$ to Output Disabled		1.5	6	1.5	10	—	15	—	18	—	20	ns

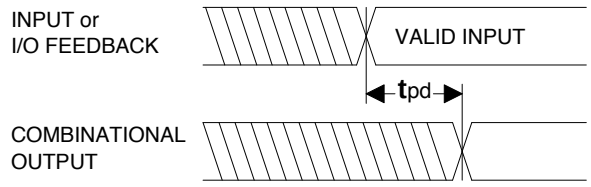
1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section.

Capacitance (TA = 25°C, f = 1.0 MHz)

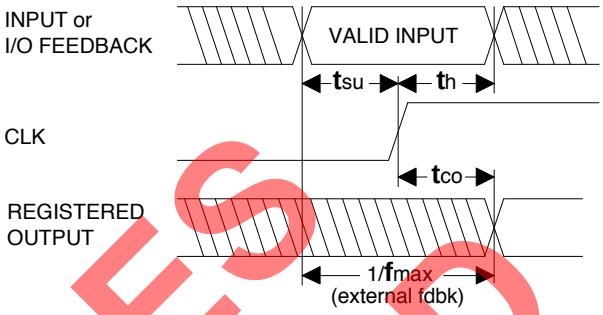
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested.

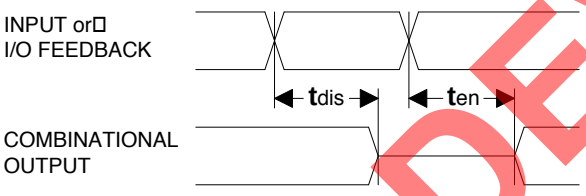
Switching Waveforms



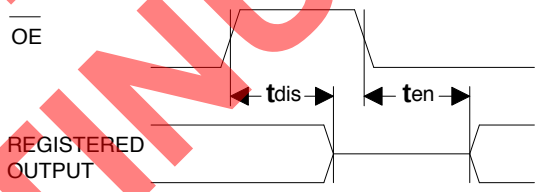
Combinatorial Output



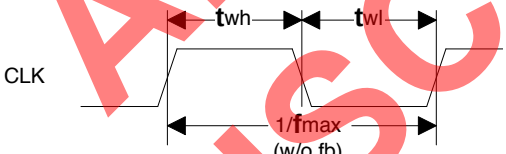
Registered Output



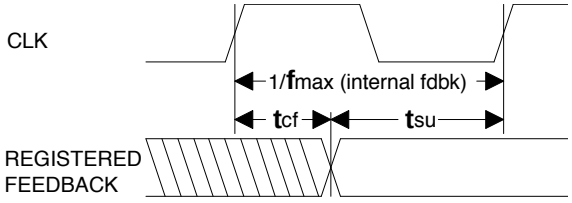
Input or I/O to Output Enable/Disable



$\overline{OE}$ to Output Enable/Disable

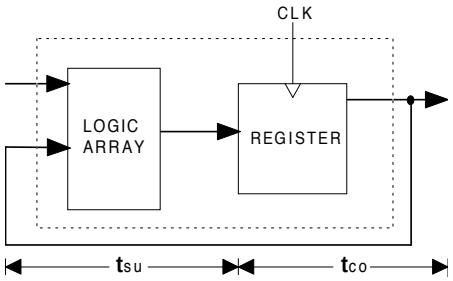


Clock Width



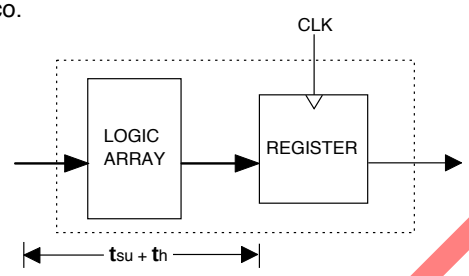
fmax with Feedback

fmax Descriptions



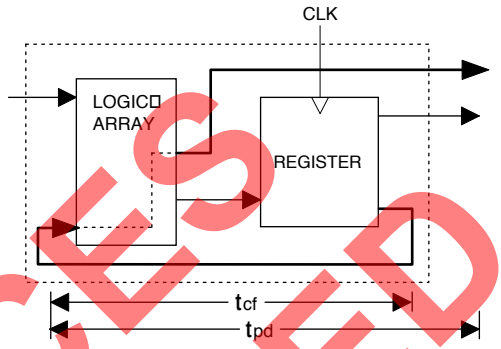
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.



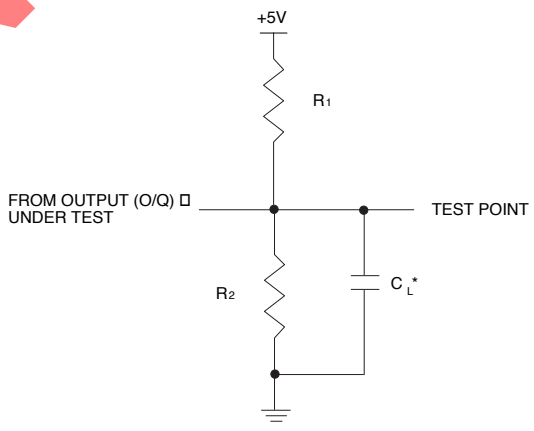
fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

Switching Test Conditions

Input Pulse Levels		GND to 3.0V
Input Rise and Fall Times	GAL20V8B	2 – 3ns 10% – 90%
	GAL20V8C	1.5ns 10% – 90%
Input Timing Reference Levels		1.5V
Output Timing Reference Levels		1.5V
Output Load		See Figure

3-state levels are measured 0.5V from steady-state active level.



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

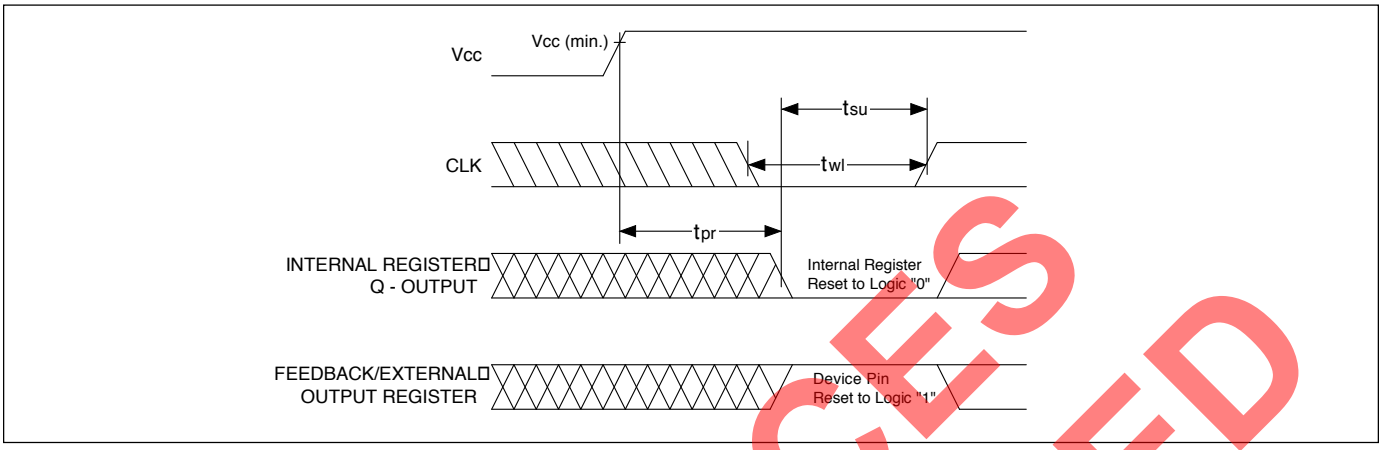
GAL20V8B Output Load Conditions (see figure)

Test Condition		R1	R2	CL
A		200Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	200Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	200Ω	390Ω	5pF

GAL20V8C Output Load Conditions (see figure)

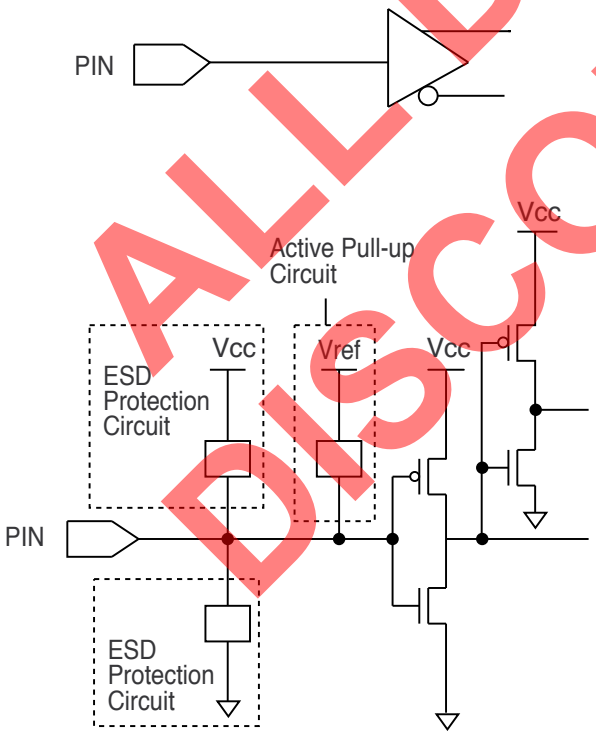
Test Condition		R1	R2	CL
A		200Ω	200Ω	50pF
B	Active High	∞	200Ω	50pF
	Active Low	200Ω	200Ω	50pF
C	Active High	∞	200Ω	5pF
	Active Low	200Ω	200Ω	5pF

Power-Up Reset



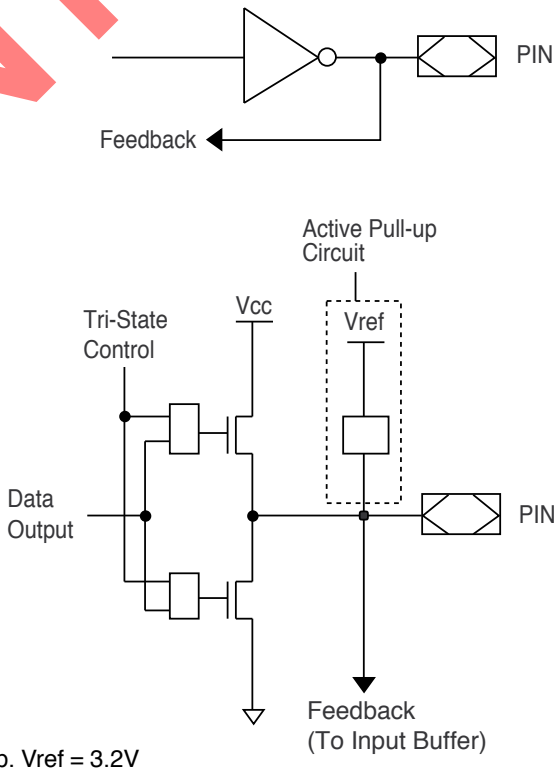
Circuitry within the GAL20V8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some conditions must be met to provide a valid power-up reset of the device. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

Input/Output Equivalent Schematics



Typ. Vref = 3.2V

Typical Input

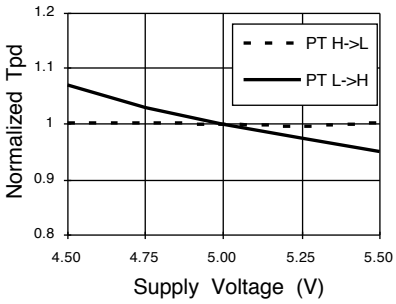


Typ. Vref = 3.2V

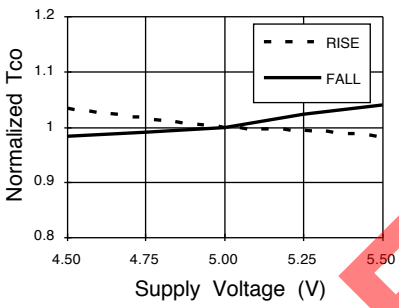
Typical Output

GAL20V8C: Typical AC and DC Characteristic Diagrams

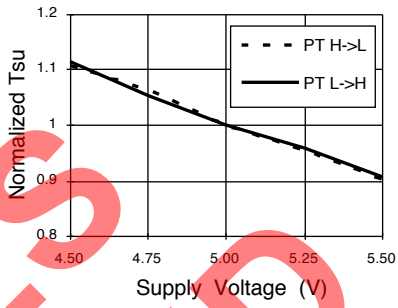
Normalized Tpd vs Vcc



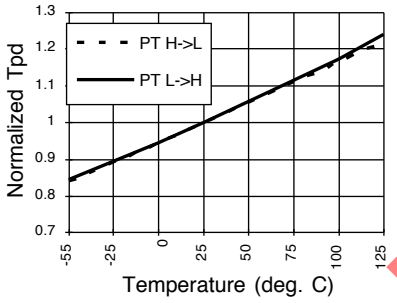
Normalized Tco vs Vcc



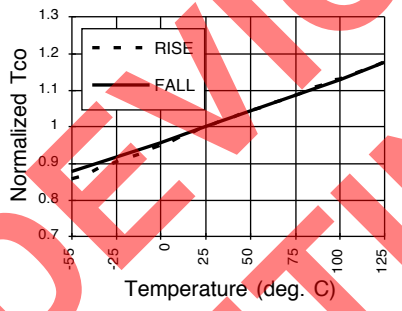
Normalized Tsu vs Vcc



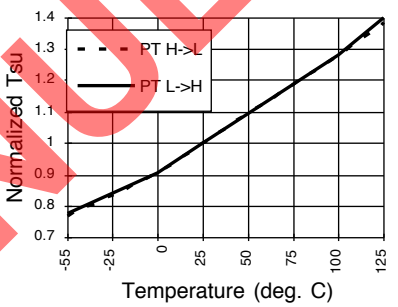
Normalized Tpd vs Temp



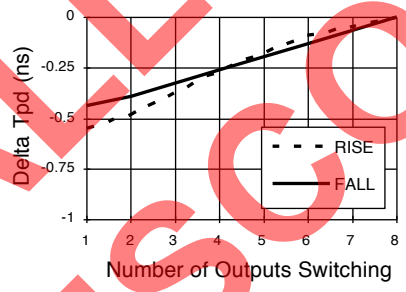
Normalized Tco vs Temp



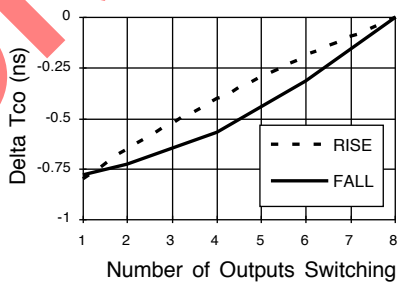
Normalized Tsu vs Temp



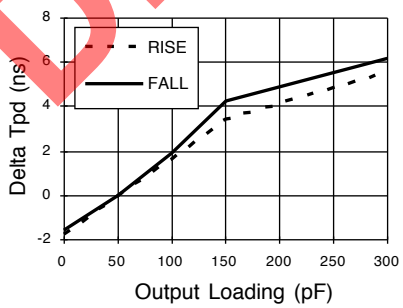
Delta Tpd vs # of Outputs Switching



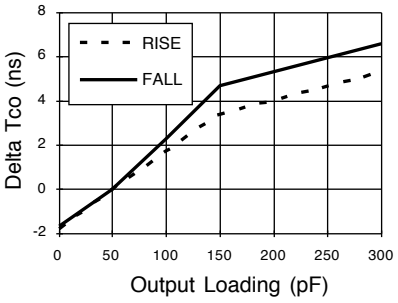
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

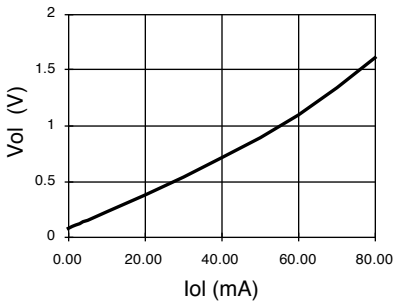


Delta Tco vs Output Loading

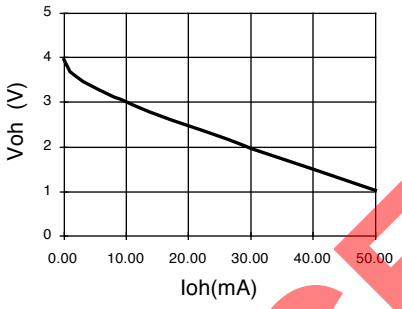


GAL20V8C: Typical AC and DC Characteristic Diagrams

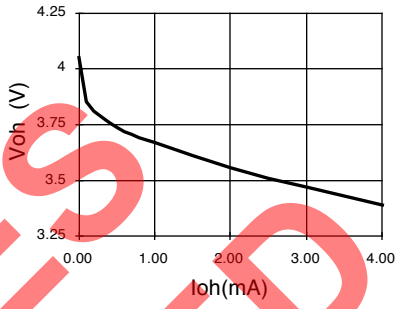
Vol vs Iol



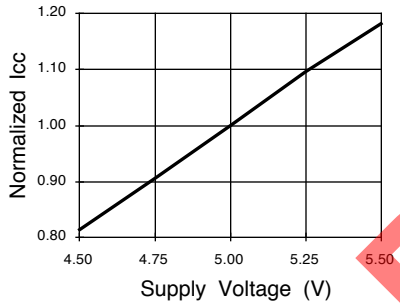
Voh vs Ioh



Voh vs Ioh

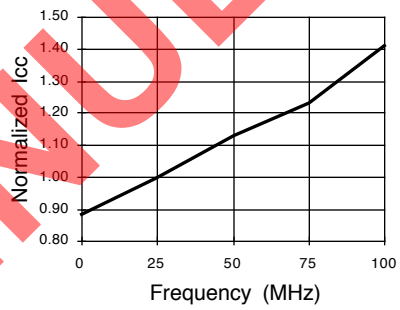


Normalized Icc vs Vcc

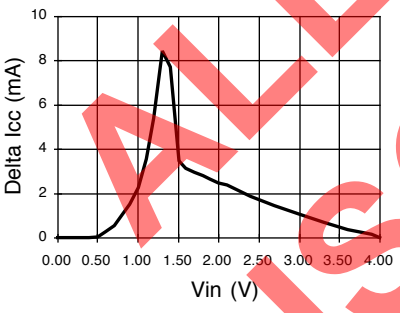


Normalized Icc vs Temp

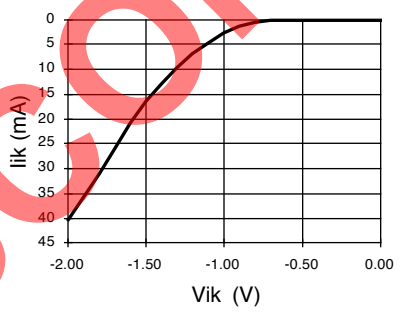
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

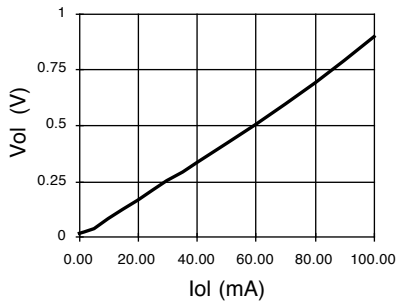


Input Clamp (Vik)

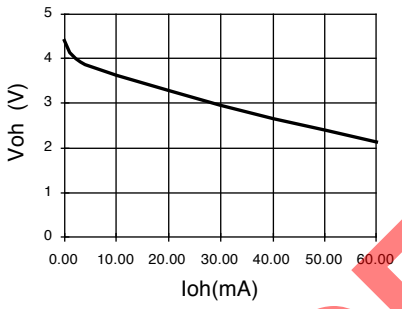


GAL20V8B-7/-10: Typical AC and DC Characteristic Diagrams

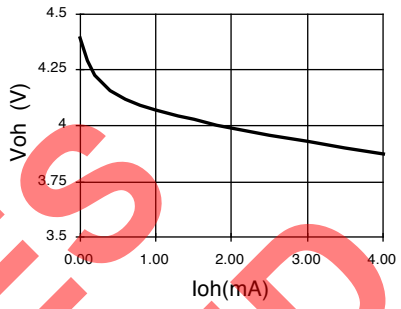
Vol vs Iol



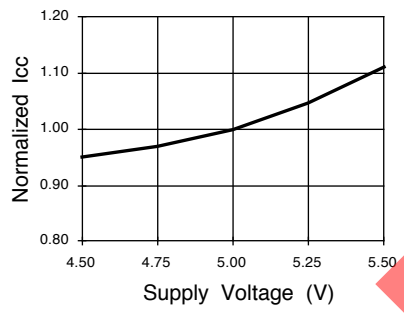
Voh vs Ioh



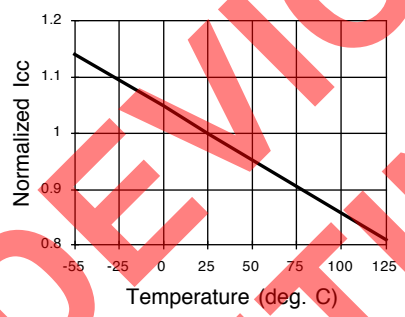
Voh vs Ioh



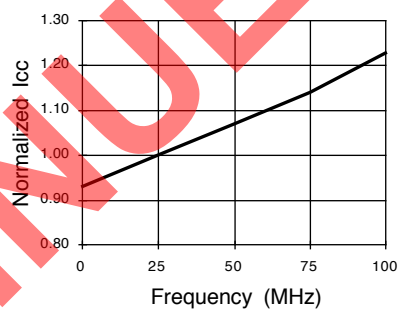
Normalized Icc vs Vcc



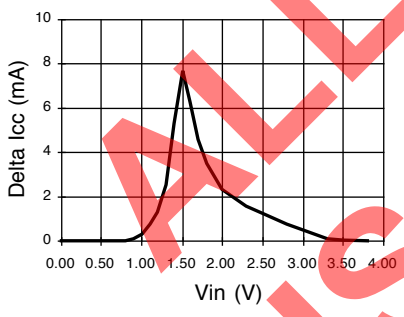
Normalized Icc vs Temp



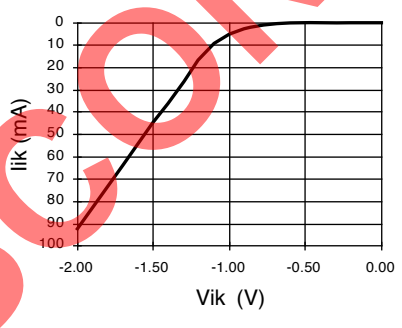
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

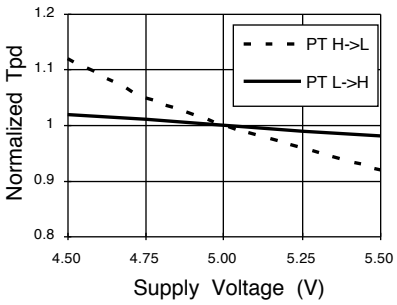


Input Clamp (Vik)

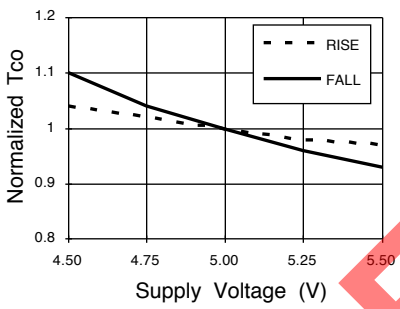


GAL20V8B-15/-25: Typical AC and DC Characteristic Diagrams

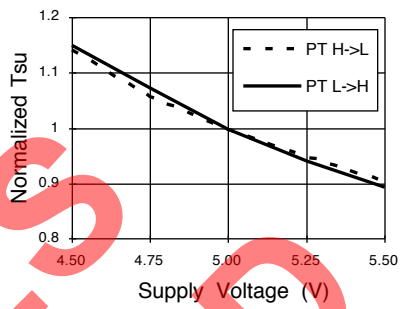
Normalized Tpd vs Vcc



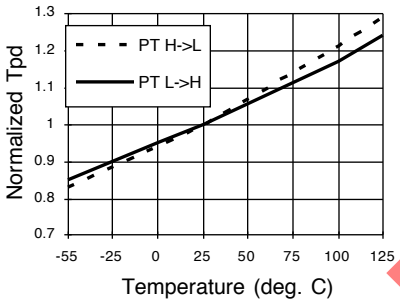
Normalized Tco vs Vcc



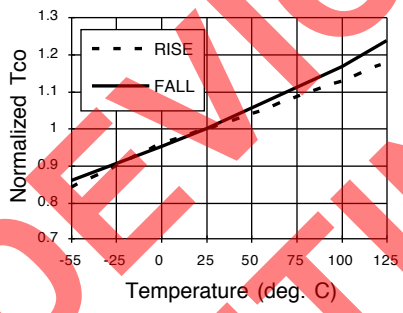
Normalized Tsu vs Vcc



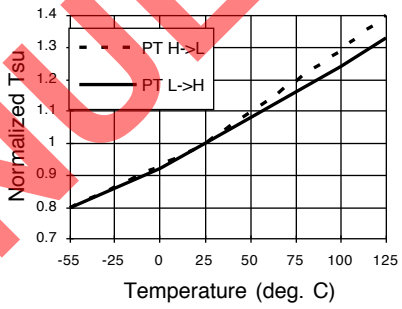
Normalized Tpd vs Temp



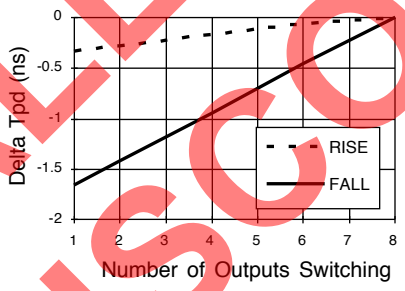
Normalized Tco vs Temp



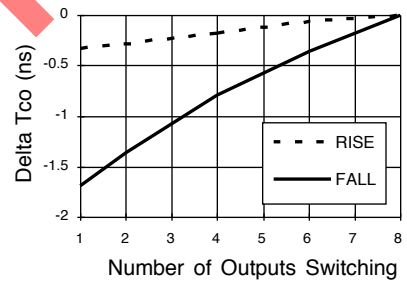
Normalized Tsu vs Temp



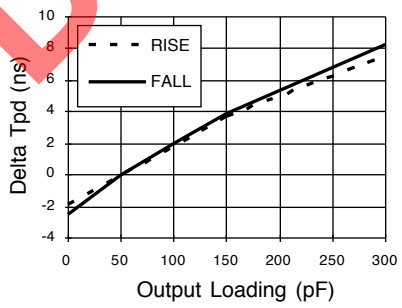
Delta Tpd vs # of Outputs Switching



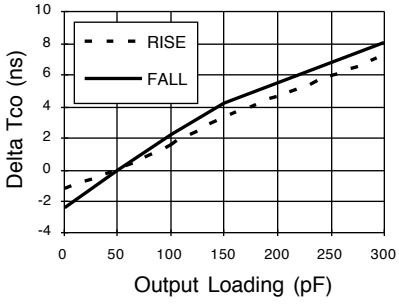
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading



Delta Tco vs Output Loading



Revision History

Date	Version	Change Summary
-	20v8_06	Previous Lattice release.
August 2006	20v8_07	Updated for lead-free package options.