Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	EE PLD
Delay Time tpd(1) Max	25 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	8
Number of Gates	-
Number of I/O	-
Operating Temperature	0°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	28-PLCC (11.51x11.51)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/gal20v8b-25ljn

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Product Line	Ordering Part Number	Product Status	Reference PCN
GAL20V8B (Cont'd)	GAL20V8B-25QJ	**Discontinued**	PCN#13-10
	GAL20V8B-25QJN		
	GAL20V8B-20QJI		PCN#09-10
	GAL20V8B-20QJNI		
	GAL20V8B-25QJI		PCN#13-10
	GAL20V8B-25QJNI		
GAL20V8C	GAL20V8C-5LJ		PCN#06-07
	GAL20V8C-5LJN		
	GAL20V8C-7LJ		PCN#13-10
	GAL20V8C-7LJN		
	GAL20V8C-10LJ		
	GAL20V8C-10LJN		
	GAL20V8C-10LJI		
	GAL20V8C-10LJNI		

Lead-Free Package Options Available!

GAL20V8

High Performance E²CMOS PLD Generic Array Logic™

Features

- HIGH PERFORMANCE E²CMOS® TECHNOLOGY
  - 5 ns Maximum Propagation Delay
  - Fmax = 166 MHz
  - 4 ns Maximum from Clock Input to Data Output
  - UltraMOS® Advanced CMOS Technology
- 50% to 75% REDUCTION IN POWER FROM BIPOLAR
  - 75mA Typ Icc on Low Power Device
  - 45mA Typ Icc on Quarter Power Device
- ACTIVE PULL-UPS ON ALL PINS
- E² CELL TECHNOLOGY
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention
- EIGHT OUTPUT LOGIC MACROCELLS
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity
  - Also Emulates 24-pin PAL® Devices with Full Function/ Fuse Map/Parametric Compatibility
- PRELOAD AND POWER-ON RESET OF ALL REGISTERS
  - 100% Functional Testability
- APPLICATIONS INCLUDE:
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- ELECTRONIC SIGNATURE FOR IDENTIFICATION
- LEAD-FREE PACKAGE OPTIONS

Functional Block Diagram

Description

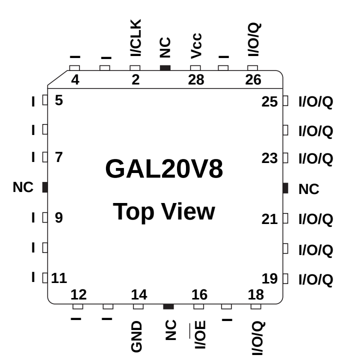
The GAL20V8C, at 5ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL20V8 are the PAL architectures listed in the table of the macrocell description section. GAL20V8 devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

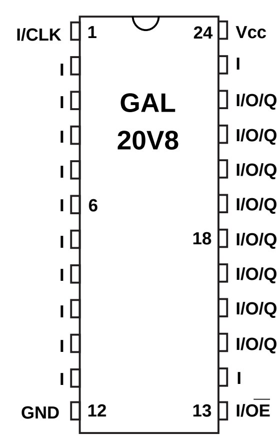
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Pin Configuration

PLCC



DIP



Lead-Free Packaging
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
5	3	4	115	GAL20V8C-5LJN[1]	Lead-Free 28-Lead PLCC
7.5	7	5	115	GAL20V8C-7LJN	Lead-Free 28-Lead PLCC
			115	GAL20V8B-7LPN[1]	Lead-Free 24-Pin Plastic DIP
10	10	7	115	GAL20V8C-10LJN	Lead-Free 28-Lead PLCC
			115	GAL20V8B-10LPN	Lead-Free 24-Pin Plastic DIP
15	12	10	55	GAL20V8B-15QJN	Lead-Free 28-Lead PLCC
			55	GAL20V8B-15QPN	Lead-Free 24-Pin Plastic DIP
			90	GAL20V8B-15LJN	Lead-Free 28-Lead PLCC
			90	GAL20V8B-15LPN	Lead-Free 24-Pin Plastic DIP
25	15	12	55	GAL20V8B-25QJN	Lead-Free 28-Lead PLCC
			55	GAL20V8B-25QPN	Lead-Free 24-Pin Plastic DIP
			90	GAL20V8B-25LJN	Lead-Free 28-Lead PLCC
			90	GAL20V8B-25LPN	Lead-Free 24-Pin Plastic DIP

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	10	7	130	GAL20V8C-10LJNI	Lead-Free 28-Pin Plastic DIP
			130	GAL20V8B-10LPNI[1]	Lead-Free 24-Pin Plastic DIP
15	12	10	130	GAL20V8B-15LJNI	Lead-Free 28-Lead PLCC
			130	GAL20V8B-15LPNI	Lead-Free 24-Pin Plastic DIP
20	13	11	65	GAL20V8B-20QJNI	Lead-Free 28-Lead PLCC
			65	GAL20V8B-20QPNI	Lead-Free 24-Pin Plastic DIP
25	15	12	65	GAL20V8B-25QJNI	Lead-Free 28-Lead PLCC
			65	GAL20V8B-25QPNI	Lead-Free 24-Pin Plastic DIP
			130	GAL20V8B-25LJNI	Lead-Free 28-Lead PLCC
			130	GAL20V8B-25LPNI	Lead-Free 24-Pin Plastic DIP

1. Discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

Part Number Description

XXXXXXXX – XX X XX X

Device Name: GAL20V8C, GAL20V8B

Speed (ns)

Power: L = Low Power, Q = Quarter Power

Package: P = Plastic DIP, PN = Lead-free Plastic DIP, J = PLCC, JN = Lead-free PLCC

Grade: Blank = Commercial, I = Industrial

Output Logic Macrocell (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL20V8 . The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL20V8 can emulate. It also shows the OLMC mode under which the devices emulate the PAL architecture.

PAL Architectures Emulated by GAL20V8	GAL20V8 Global OLMC Mode
20R8	Registered
20R6	Registered
20R4	Registered
20RP8	Registered
20RP6	Registered
20RP4	Registered
20L8	Complex
20H8	Complex
20P8	Complex
14L8	Simple
16L6	Simple
18L4	Simple
20L2	Simple
14H8	Simple
16H6	Simple
18H4	Simple
20H2	Simple
14P8	Simple
16P6	Simple
18P4	Simple
20P2	Simple

Compiler Support for OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode. In **registered mode** pin 1 and pin 13 (DIP pinout) are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 13 become dedicated inputs and use the feedback paths of pin 22 and pin 15 respectively. Because of this feedback path usage, pin 22 and pin 15 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 18 and 19) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P20V8R	P20V8C	P20V8AS	P20V8
CUPL	G20V8MS	G20V8MA	G20V8AS	G20V8
LOG/iC	GAL20V8_R	GAL20V8_C7	GAL20V8_C8	GAL20V8
OrCAD-PLD	"Registered"[1]	"Complex"[1]	"Simple"[1]	GAL20V8A
PLDesigner	P20V8R[2]	P20V8C[2]	P20V8C[2]	P20V8A
TANGO-PLD	G20V8R	G20V8C	G20V8AS[3]	G20V8

1) Used with **Configuration** keyword.
2) Prior to Version 2.0 support.
3) Supported on Version 1.20 or later.

Registered Mode

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

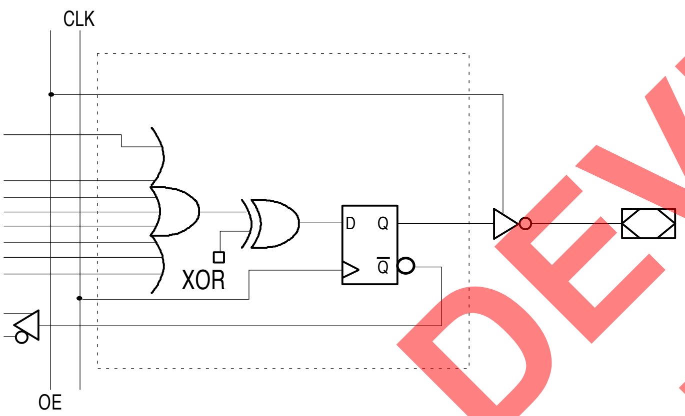
Architecture configurations available in this mode are similar to the common 20R8 and 20RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/Os are possible in this mode.

Dedicated input or output functions can be implemented as subsets of the I/O function.

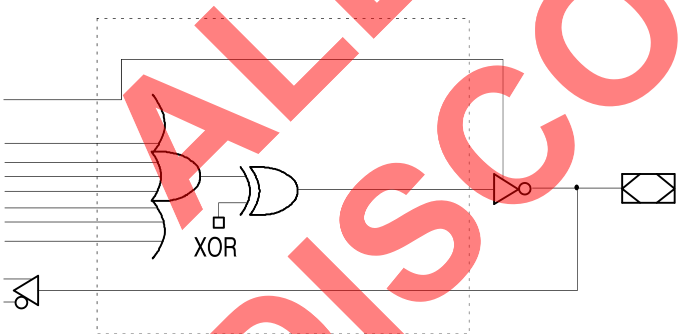
Registered outputs have eight product terms per output. I/Os have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 1 controls common CLK for the registered outputs.
- Pin 13 controls common $\overline{OE}$ for the registered outputs.
- Pin 1 & Pin 13 are permanently configured as CLK & $\overline{OE}$ for registered output configuration.



Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 1 & Pin 13 are permanently configured as CLK & $\overline{OE}$ for registered output configuration..

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Complex Mode

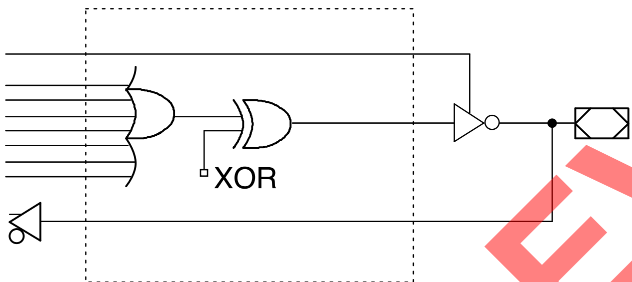
In the Complex mode, macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 20L8 and 20P8 devices with programmable polarity in each macrocell.

Up to six I/Os are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 15 & 22) do not have input capability. Designs requiring eight I/Os can be implemented in the Registered mode.

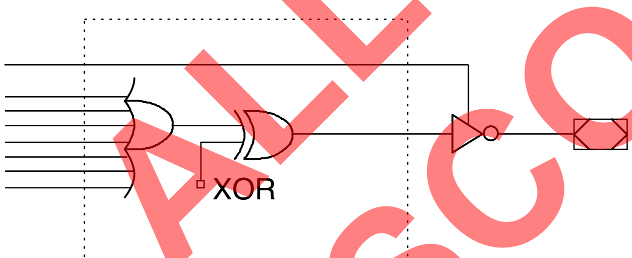
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 13 are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 16 through Pin 21 are configured to this function.



Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 15 and Pin 22 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Simple Mode

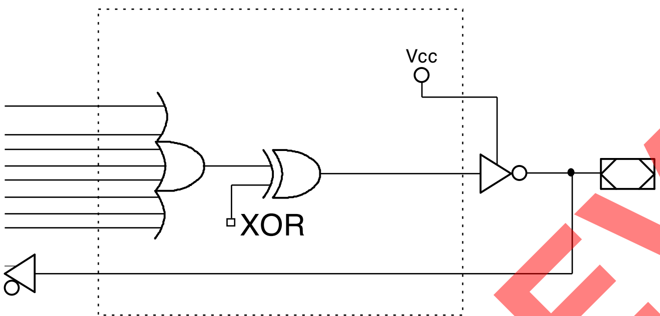
In the Simple mode, pins are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 14L8 and 16P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

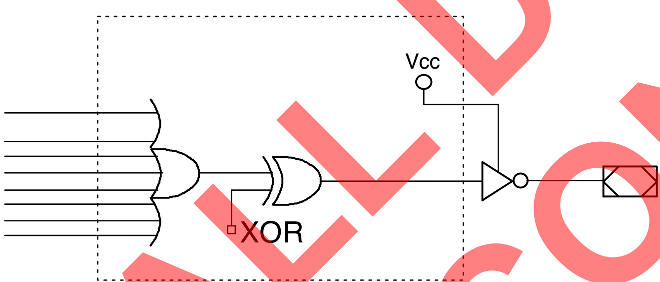
Pins 1 and 13 are always available as data inputs into the AND array. The "center" two macrocells (pins 18 and 19) cannot be used in the input configuration.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



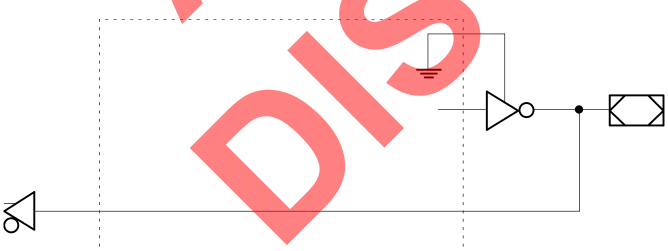
Combinatorial Output with Feedback Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- All OLMC **except** pins 18 & 19 can be configured to this function.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- Pins 18 & 19 are permanently configured to this function.

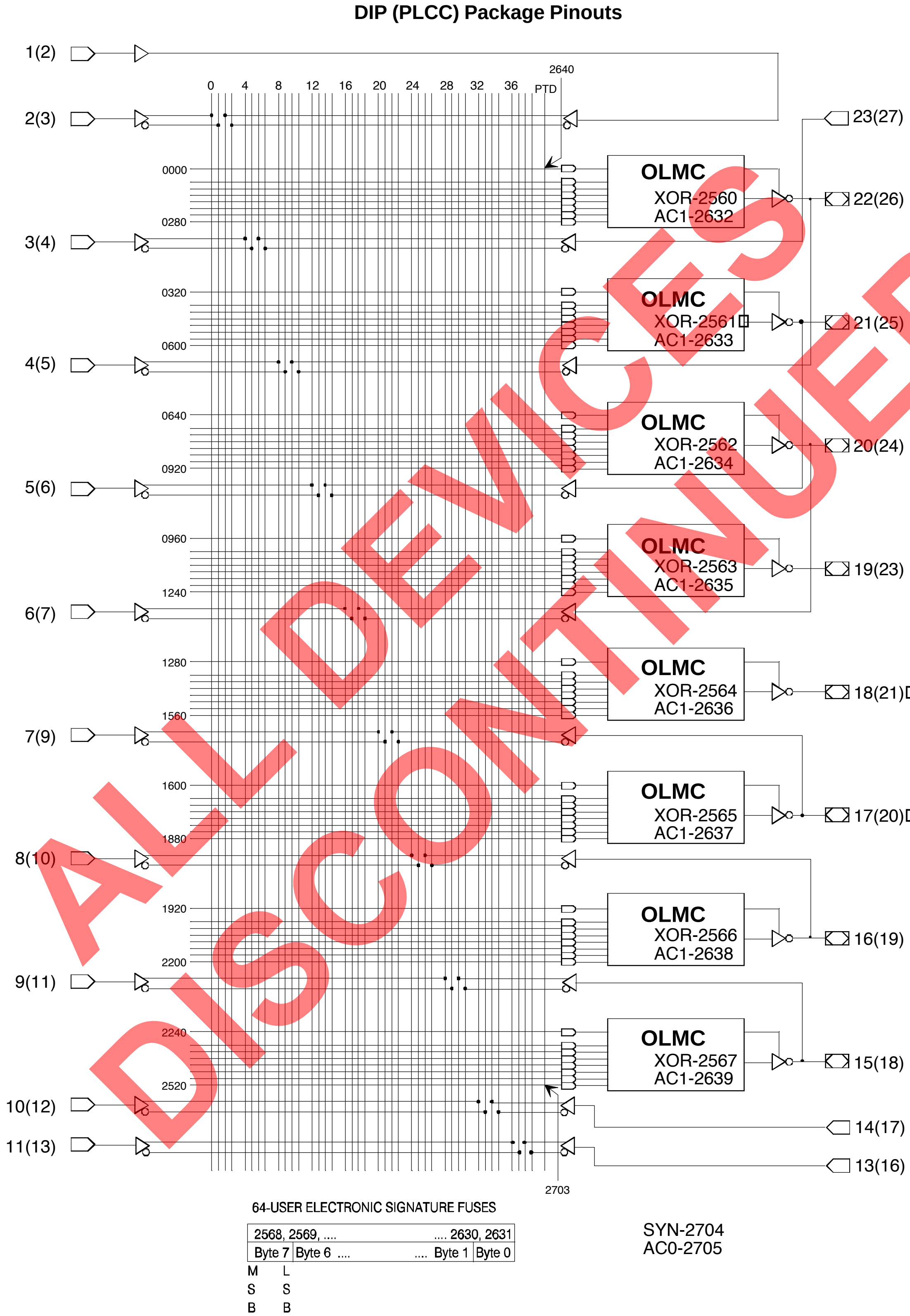


Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- All OLMC **except** pins 18 & 19 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Simple Mode Logic Diagram



Absolute Maximum Ratings(1)

Supply voltage V_{CC} .... –0.5 to +7V
Input voltage applied .... –2.5 to V_{CC} +1.0V
Off-state output voltage applied .... –2.5 to V_{CC} +1.0V
Storage Temperature .... –65 to 150°C
Ambient Temperature with
  Power Applied .... –55 to 125°C

1.Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Commercial Devices:
Ambient Temperature (T_A) .... 0 to 75°C
Supply voltage (V_{CC})
  with Respect to Ground .... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature (T_A) .... –40 to 85°C
Supply voltage (V_{CC})
  with Respect to Ground .... +4.50 to +5.50V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
VIL	Input Low Voltage		Vss – 0.5	—	0.8	V
VIH	Input High Voltage		2.0	—	Vcc+1	V
IIL[1]	Input or I/O Low Leakage Current	0V ≤ VIN ≤ VIL (MAX.)	—	—	–100	μA
IIH	Input or I/O High Leakage Current	3.5V ≤ VIN ≤ VCC	—	—	10	μA
VOL	Output Low Voltage	IOL = MAX. Vin = VIL or VIH	—	—	0.5	V
VOH	Output High Voltage	IOH = MAX. Vin = VIL or VIH	2.4	—	—	V
IOL	Low Level Output Current		—	—	16	mA
IOH	High Level Output Current		—	—	–3.2	mA
IOS[2]	Output Short Circuit Current	VCC = 5V VOUT = 0.5V T_A = 25°C	–30	—	–150	mA

COMMERCIAL

ICC	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 15MHz Outputs Open	L -5/-7/-10	—	75	115	mA

INDUSTRIAL

ICC	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 15MHz Outputs Open	L-10	—	75	130	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

AC Switching Characteristics

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION		COM -5 MIN.	COM -5 MAX.	COM -7 MIN.	COM -7 MAX.	COM/IND -10 MIN.	COM/IND -10 MAX.	UNITS
tpd	A	Input or I/O to Comb. Output	8 outputs switching	1	5	3	7.5	3	10	ns
			1 output switching	—	—	—	7	—	—	ns
tco	A	Clock to Output Delay		1	4	2	5	2	7	ns
tcf[2]	—	Clock to Feedback Delay		—	3	—	3	—	6	ns
tsu	—	Setup Time, Input or Feedback before Clock↑		3	—	5	—	7.5	—	ns
th	—	Hold Time, Input or Feedback after Clock↑		0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)		142.8	—	100	—	66.7	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)		166	—	125	—	71.4	—	MHz
	A	Maximum Clock Frequency with No Feedback		166	—	125	—	83.3	—	MHz
twh	—	Clock Pulse Duration, High		3	—	4	—	6	—	ns
twl	—	Clock Pulse Duration, Low		3	—	4	—	6	—	ns
ten	B	Input or I/O to Output Enabled		1	6	3	9	3	10	ns
	B	$\overline{OE}$ to Output Enabled		1	6	2	6	2	10	ns
tdis	C	Input or I/O to Output Disabled		1	5	2	9	2	10	ns
	C	$\overline{OE}$ to Output Disabled		1	5	1.5	6	1.5	10	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section. Characterized initially and after any design or process changes that may affect these parameters.

Capacitance (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested

Absolute Maximum Ratings(1)

Supply voltage V_{CC} .... –0.5 to +7V
Input voltage applied .... –2.5 to V_{CC} +1.0V
Off-state output voltage applied .... –2.5 to V_{CC} +1.0V
Storage Temperature .... –65 to 150°C
Ambient Temperature with
 Power Applied .... –55 to 125°C

1.Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Commercial Devices:
Ambient Temperature (T_A) .... 0 to 75°C
Supply voltage (V_{CC})
 with Respect to Ground .... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature (T_A) .... –40 to 85°C
Supply voltage (V_{CC})
 with Respect to Ground .... +4.50 to +5.50V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	24	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–150	mA

COMMERCIAL

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	**L** -7/-10	—	75	115	mA
			L -15/-25	—	75	90	mA
			Q -15/-25	—	45	55	mA

INDUSTRIAL

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	**L** -10/-15/-25	—	75	130	mA
			Q -20/-25	—	45	65	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

AC Switching Characteristics

Over Recommended Operating Conditions

PARAM.	TEST COND[1].	DESCRIPTION		COM -7 MIN.	COM -7 MAX.	COM / IND -10 MIN.	COM / IND -10 MAX.	COM / IND -15 MIN.	COM / IND -15 MAX.	IND -20 MIN.	IND -20 MAX.	COM / IND -25 MIN.	COM / IND -25 MAX.	UNITS
tpd	A	Input or I/O to Comb. Output	8 outputs switching	3	7.5	3	10	3	15	3	20	3	25	ns
			1 output switching	—	7	—	—	—	—	—	—	—	—	ns
tco	A	Clock to Output Delay		2	5	2	7	2	10	2	11	2	12	ns
tcf[2]	—	Clock to Feedback Delay		—	3	—	6	—	8	—	9	—	10	ns
tsu	—	Setup Time, Input or Fdbk before Clk↑		7	—	10	—	12	—	13	—	15	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑		0	—	0	—	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)		83.3	—	58.8	—	45.5	—	41.6	—	37	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)		100	—	62.5	—	50	—	45.4	—	40	—	MHz
	A	Maximum Clock Frequency with No Feedback		100	—	62.5	—	62.5	—	50	—	41.7	—	MHz
twh	—	Clock Pulse Duration, High		5	—	8	—	8	—	10	—	12	—	ns
twl	—	Clock Pulse Duration, Low		5	—	8	—	8	—	10	—	12	—	ns
ten	B	Input or I/O to Output Enabled		3	9	3	10	—	15	—	18	—	25	ns
	B	$\overline{OE}$ to Output Enabled		2	6	2	10	—	15	—	18	—	20	ns
tdis	C	Input or I/O to Output Disabled		2	9	2	10	—	15	—	18	—	25	ns
	C	$\overline{OE}$ to Output Disabled		1.5	6	1.5	10	—	15	—	18	—	20	ns

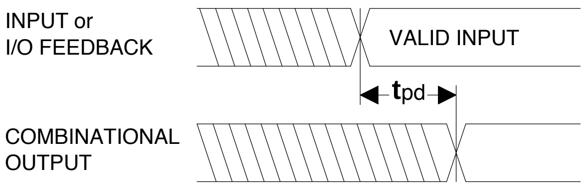
1) Refer to **Switching Test Conditions** section.
2) Calculated from **f**max with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section.

Capacitance (TA = 25°C, f = 1.0 MHz)

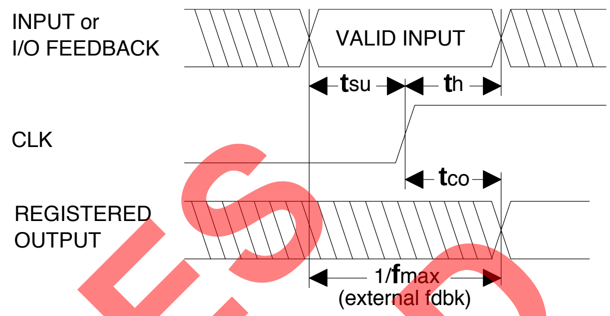
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested.

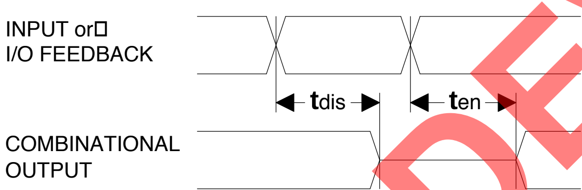
Switching Waveforms



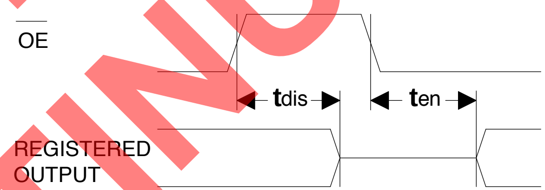
Combinatorial Output



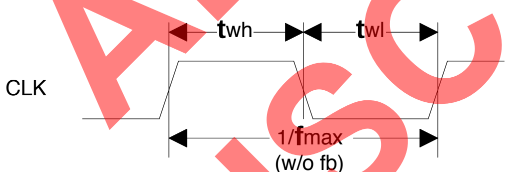
Registered Output



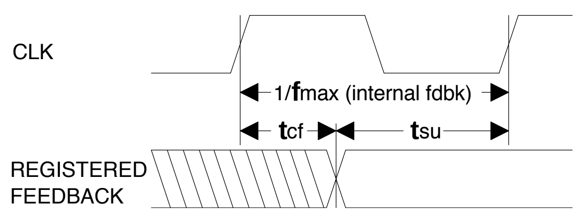
Input or I/O to Output Enable/Disable



OE to Output Enable/Disable

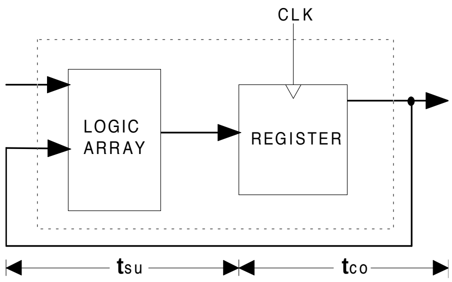


Clock Width



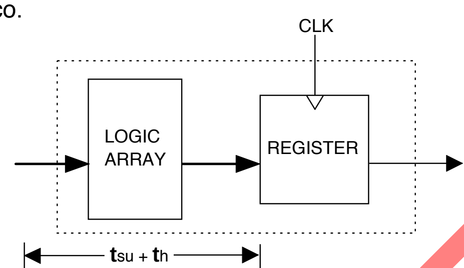
fmax with Feedback

fmax Descriptions



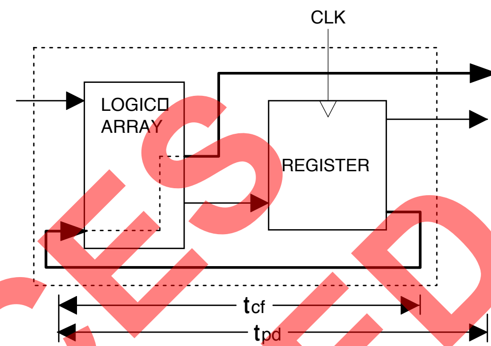
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.



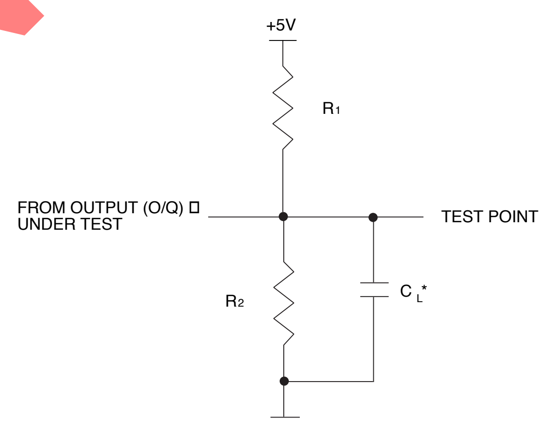
fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

Switching Test Conditions

Input Pulse Levels		GND to 3.0V
Input Rise and Fall Times	GAL20V8B	2 – 3ns 10% – 90%
	GAL20V8C	1.5ns 10% – 90%
Input Timing Reference Levels		1.5V
Output Timing Reference Levels		1.5V
Output Load		See Figure

3-state levels are measured 0.5V from steady-state active level.



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

GAL20V8B Output Load Conditions (see figure)

Test Condition		R1	R2	CL
A		200Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	200Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	200Ω	390Ω	5pF

GAL20V8C Output Load Conditions (see figure)

Test Condition		R1	R2	CL
A		200Ω	200Ω	50pF
B	Active High	∞	200Ω	50pF
	Active Low	200Ω	200Ω	50pF
C	Active High	∞	200Ω	5pF
	Active Low	200Ω	200Ω	5pF

Electronic Signature

An electronic signature is provided in every GAL20V8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the checksum.

Security Cell

A security cell is provided in the GAL20V8 devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

Latch-Up Protection

GAL20V8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias minimizes the potential of latch-up caused by negative input undershoots. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups in order to eliminate latch-up due to output overshoots.

Device Programming

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

Output Register Preload

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

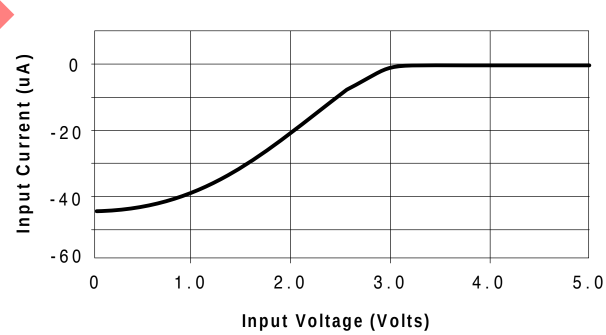
GAL20V8 devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing text vectors perform output register preload automatically.

Input Buffers

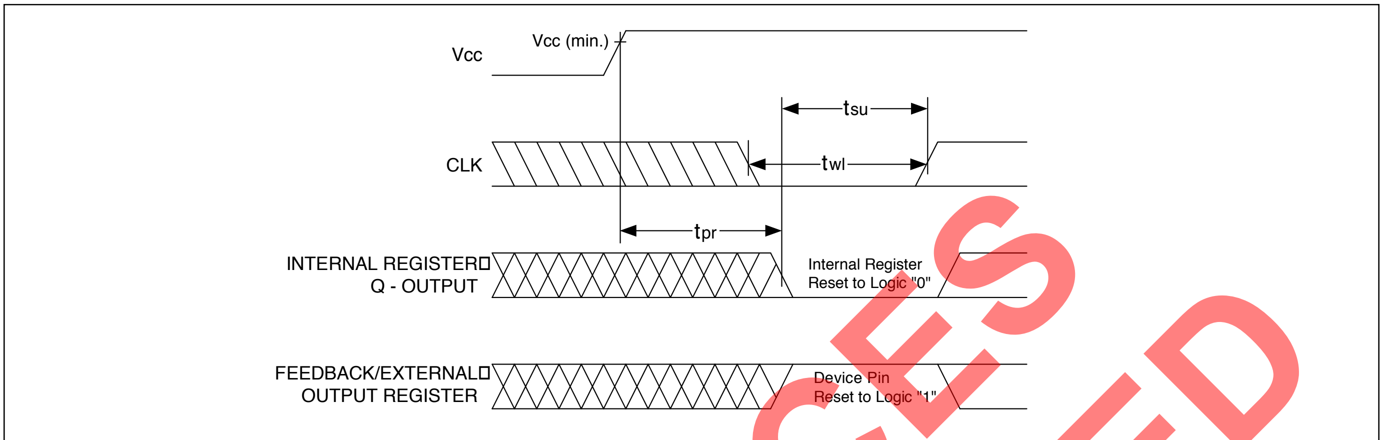
GAL20V8 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The GAL20V8 input and I/O pins have built-in active pull-ups. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC}, or Ground. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

Typical Input Pull-up Characteristic

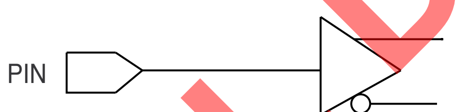


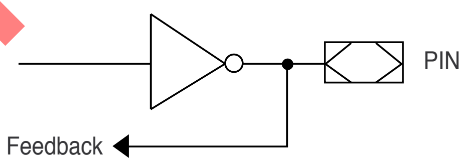
Power-Up Reset

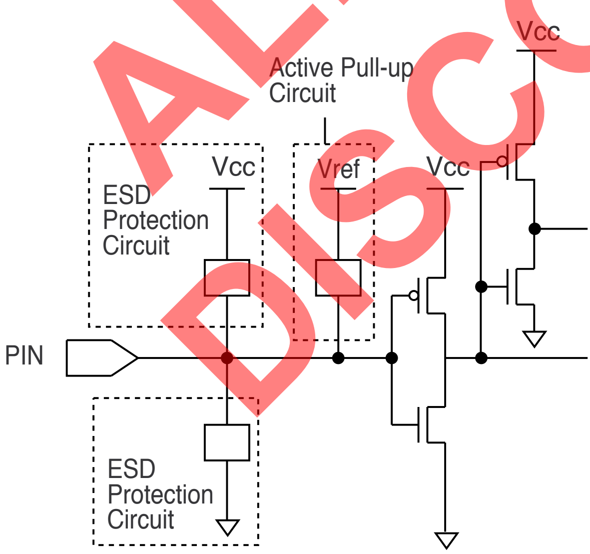


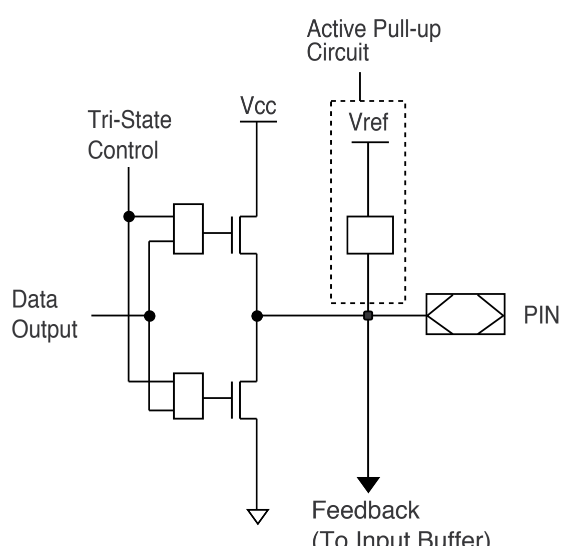
Circuitry within the GAL20V8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr}, 1μs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some conditions must be met to provide a valid power-up reset of the device. First, the V_{CC} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

Input/Output Equivalent Schematics









Typ. Vref = 3.2V

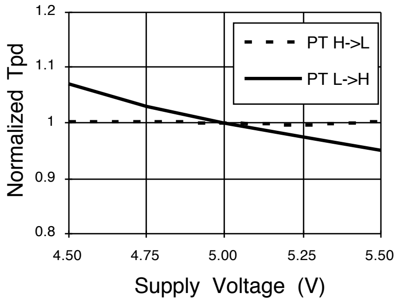
Typical Input

Typ. Vref = 3.2V

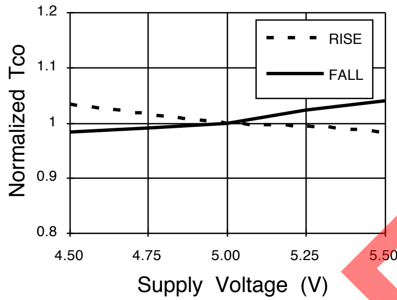
Typical Output

GAL20V8C: Typical AC and DC Characteristic Diagrams

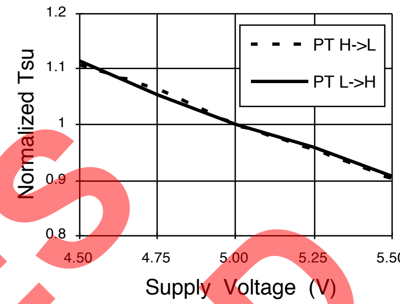
Normalized Tpd vs Vcc



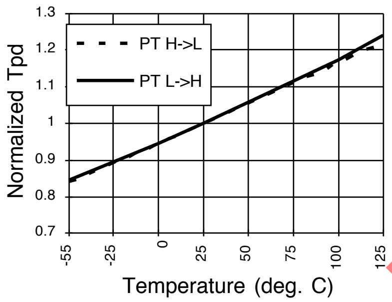
Normalized Tco vs Vcc



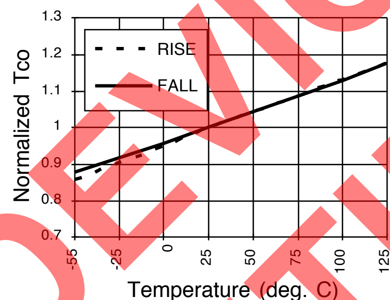
Normalized Tsu vs Vcc



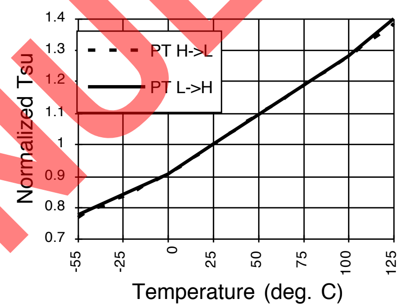
Normalized Tpd vs Temp



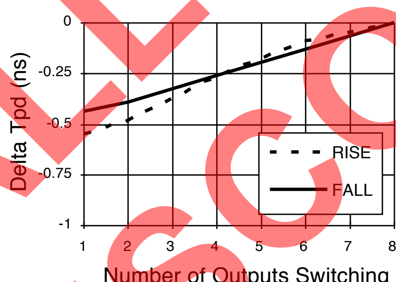
Normalized Tco vs Temp



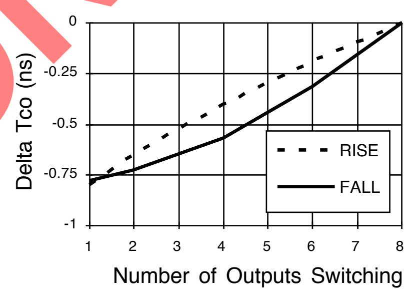
Normalized Tsu vs Temp



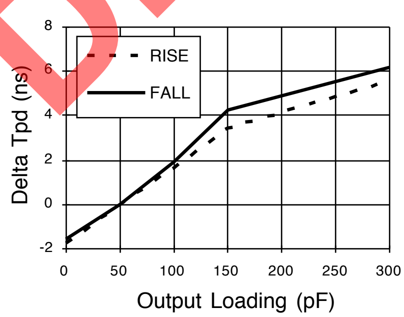
Delta Tpd vs # of Outputs Switching



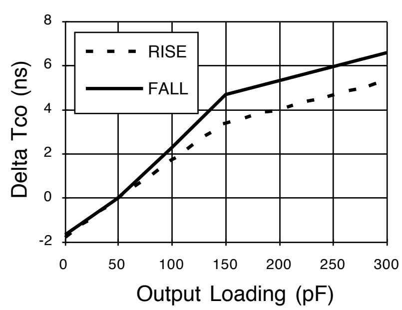
Delta Tco vs # of Outputs Switching



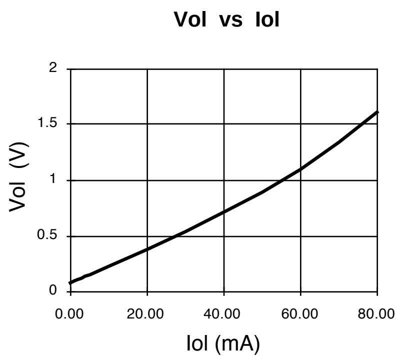
Delta Tpd vs Output Loading

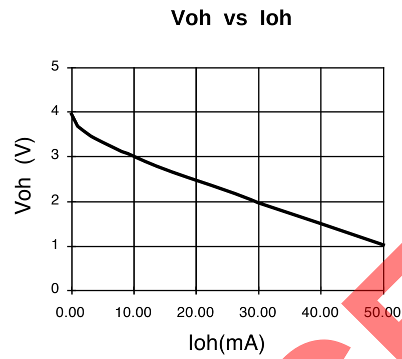


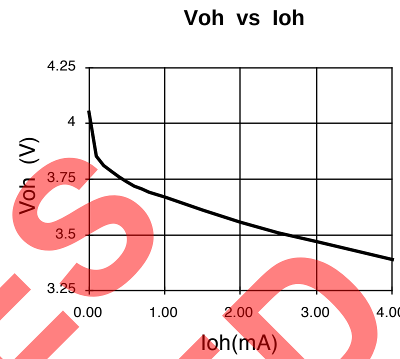
Delta Tco vs Output Loading

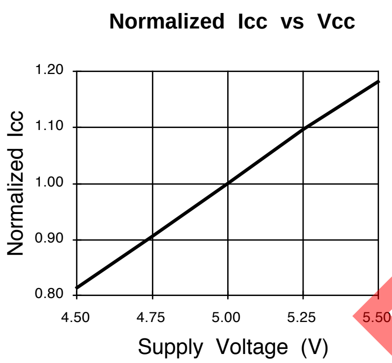


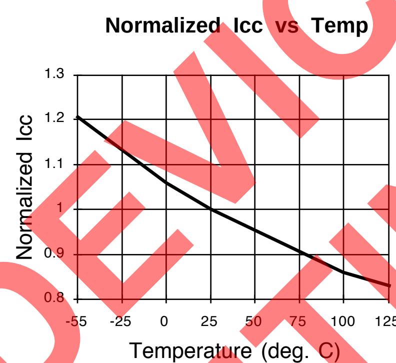
GAL20V8C: Typical AC and DC Characteristic Diagrams

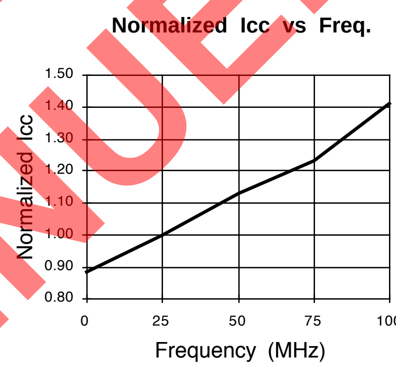


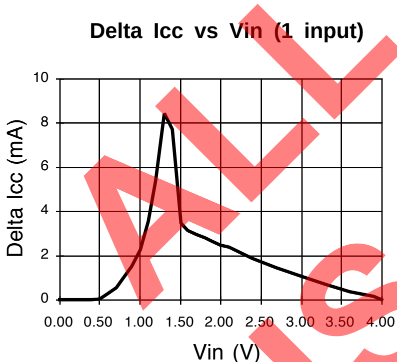


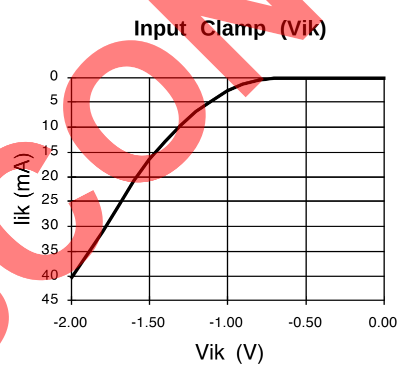






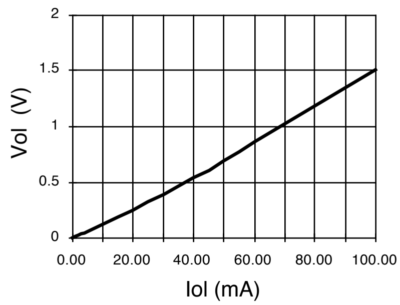




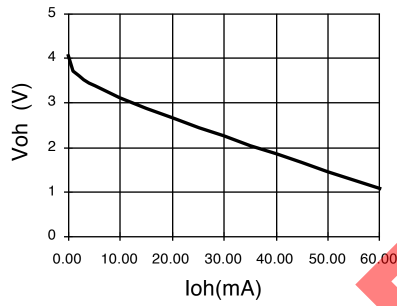


GAL20V8B-15/-25: Typical AC and DC Characteristic Diagrams

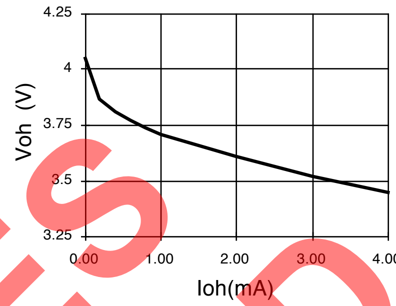
Vol vs Iol



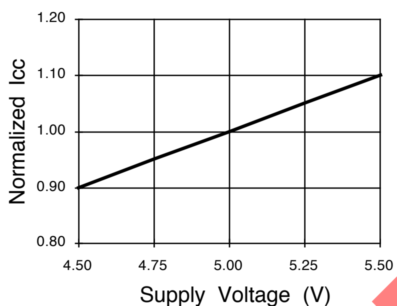
Voh vs Ioh



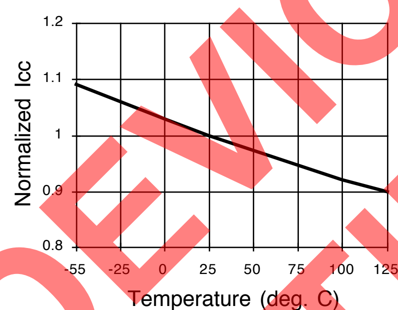
Voh vs Ioh



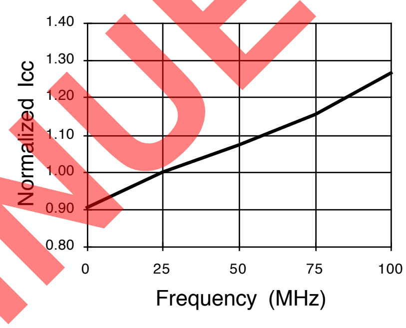
Normalized Icc vs Vcc



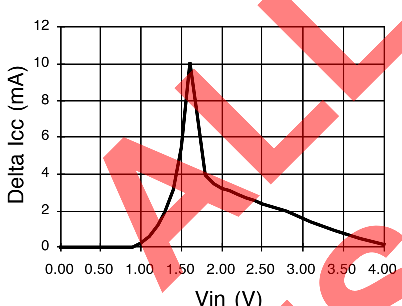
Normalized Icc vs Temp



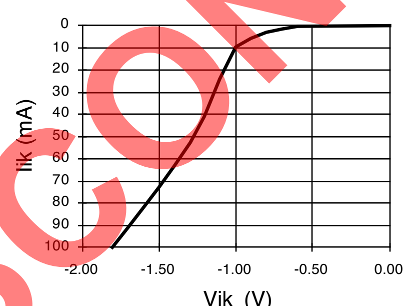
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



Revision History

Date	Version	Change Summary
-	20v8_06	Previous Lattice release.
August 2006	20v8_07	Updated for lead-free package options.